N-Channel Enhancement-Mode Vertical DMOS FETs

Features

- Low threshold (2.0V max.)
- High input impedance
- Low input capacitance (50pF typ.)
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

This low threshold enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Ordering Information

Device	Order Number / Die*	BV_{DSS}/ BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$V_{GS(th)}$ (max) (V)	$I_{D(ON)}$ (min) (A)
TN1504	TN1504NW	40	3.0	2.0	2.0

** Die in wafer form.*

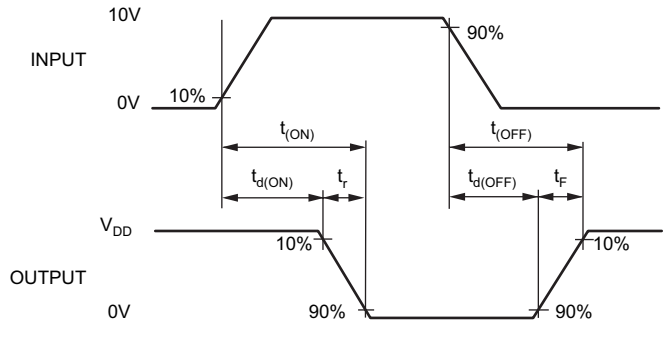
Electrical Characteristics (T_A = 25°C unless otherwise specified)

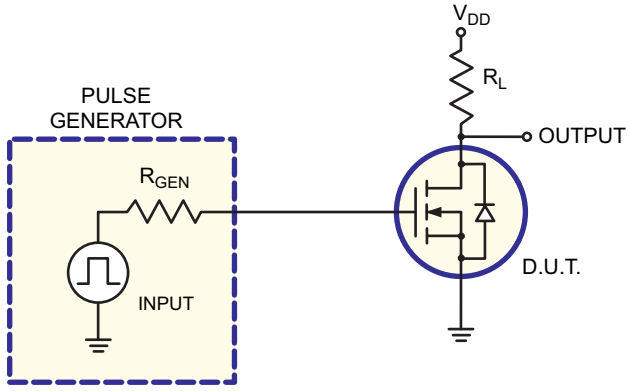
Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	40	-	-	V	V_{GS}= 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	V_{GS} = V_{DS}, I_D = 0.5mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage	-	0.1	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} =0V, V_{DS} = Max Rating
				500		V_{DS} = 0.8 Max Rating V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-	1.4	-	A	V_{GS} = 5V, V_{DS} = 25V
		-	3.4	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	4.5	Ω	V_{GS} = 4.5V, I_D = 250mA
		-	1.6	3.0		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.6	1.1	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward transconductance	225	400	-	mmho	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input capacitance	-	50	60	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	25	35		
C_{RSS}	Reverse transfer capacitance	-	4.0	8.05		
$t_{d(ON)}$	Turn-on delay time	-	2.0	5.0	ns	V_{DD} = 25V, I_D = 1.0A R_{GEN} = 25Ω
t_r	Rise time	-	3.0	5.0		
$t_{d(OFF)}$	Turn-off delay time	-	6.0	7.0		
t_f	Fall time	-	3.0	6.0		
V_{SD}	Diode forward voltage drop	-	1.0	1.5	V	V_{GS} = 0V, I_{SD} = 0.5A
t_{rr}	Reverse recovery time	-	400	-	ns	V_{GS} = 0V, I_{SD} = 0.5A

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit





Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com