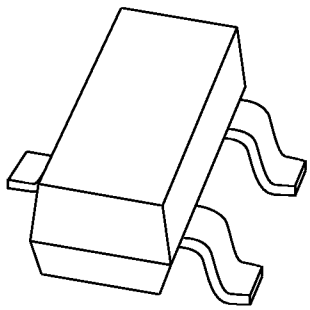
DATA SHEET



PMBF107
N-channel enhancement mode vertical D-MOS transistor

Product specification
1998 Mar 06
Supersedes data of April 1995
File under Discrete Semiconductors, SC13b

Philips Semiconductors

PHILIPS

N-channel enhancement mode vertical D-MOS transistor

PMBF107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Relay, high-speed and line transformer drivers.

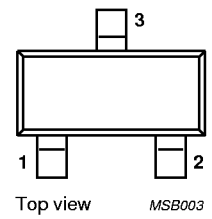
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 package, intended for use as a line current interruptor in telephone sets.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



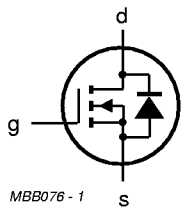


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.6 V	28	Ω
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	2.4	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
V_{GSO}	gate-source voltage	open drain	–	±20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 130 V	–	–	30	nA
I_{DSX}	drain cut-off current	V_{GS} = 0.2 V; V_{DS} = 70 V	–	–	1	μA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0;	–	–	±10	nA
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.8	–	2.4	V
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.6 V; I_D = 20 mA	–	20	28	Ω
		V_{GS} = 10 V; I_D = 150 mA	–	14	–	Ω
$\lvert y_{fs} \rvert$	transfer admittance	V_{DS} = 15 V; I_D = 250 mA	75	170	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 250 mA	–	2	10	ns
t_{off}	turn-off time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 200 mA	–	5	20	ns

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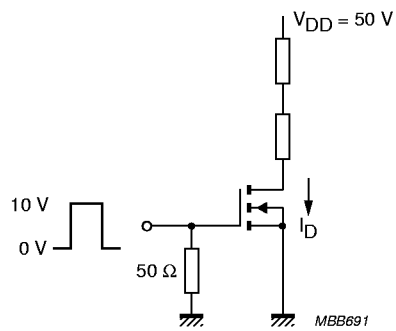


Fig.2 Switching time test circuit.

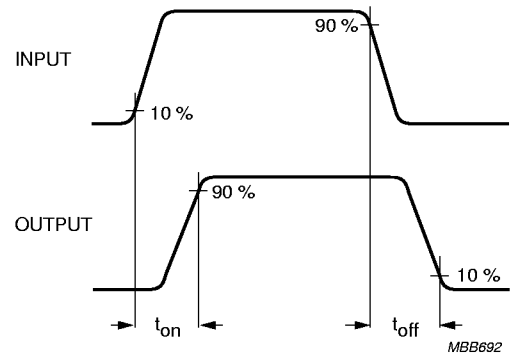


Fig.3 Input and output waveforms.

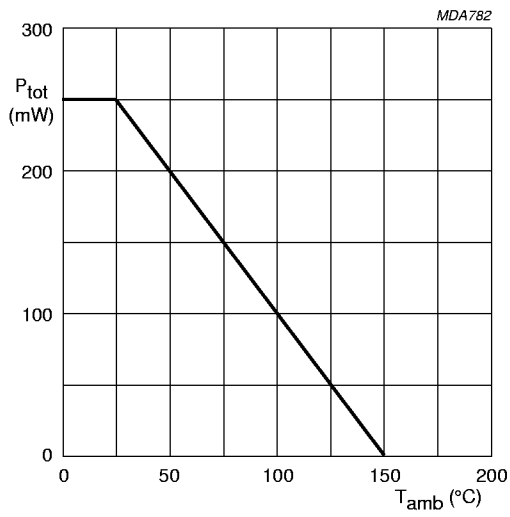


Fig.4 Power derating curve.

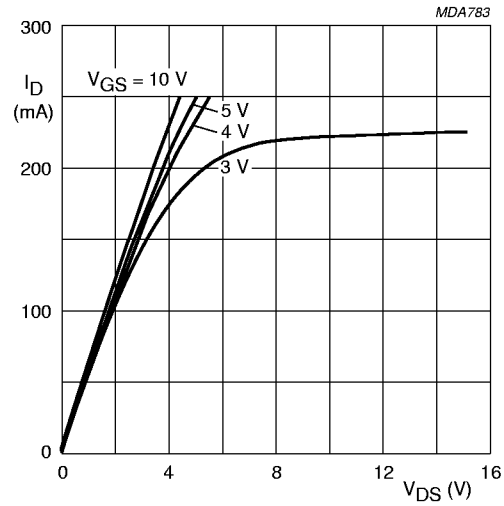


Fig.5 Typical output characteristics; T_j = 25 °C.

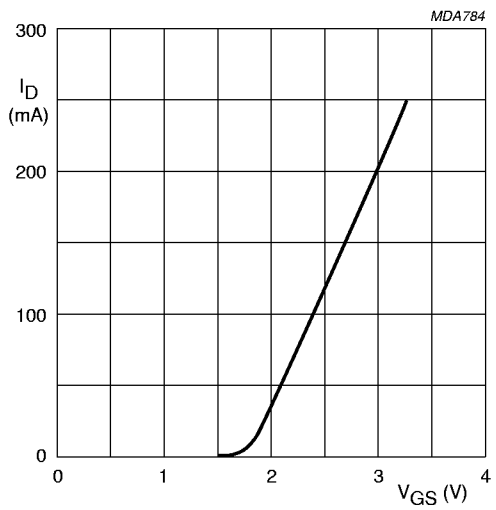


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

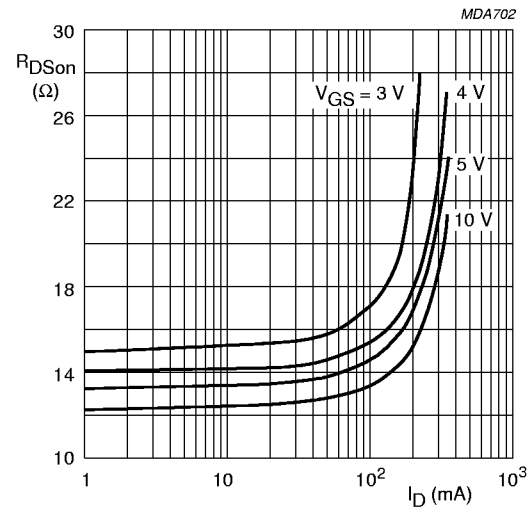


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

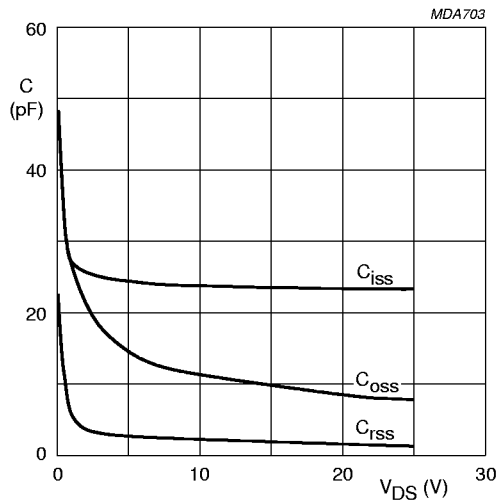
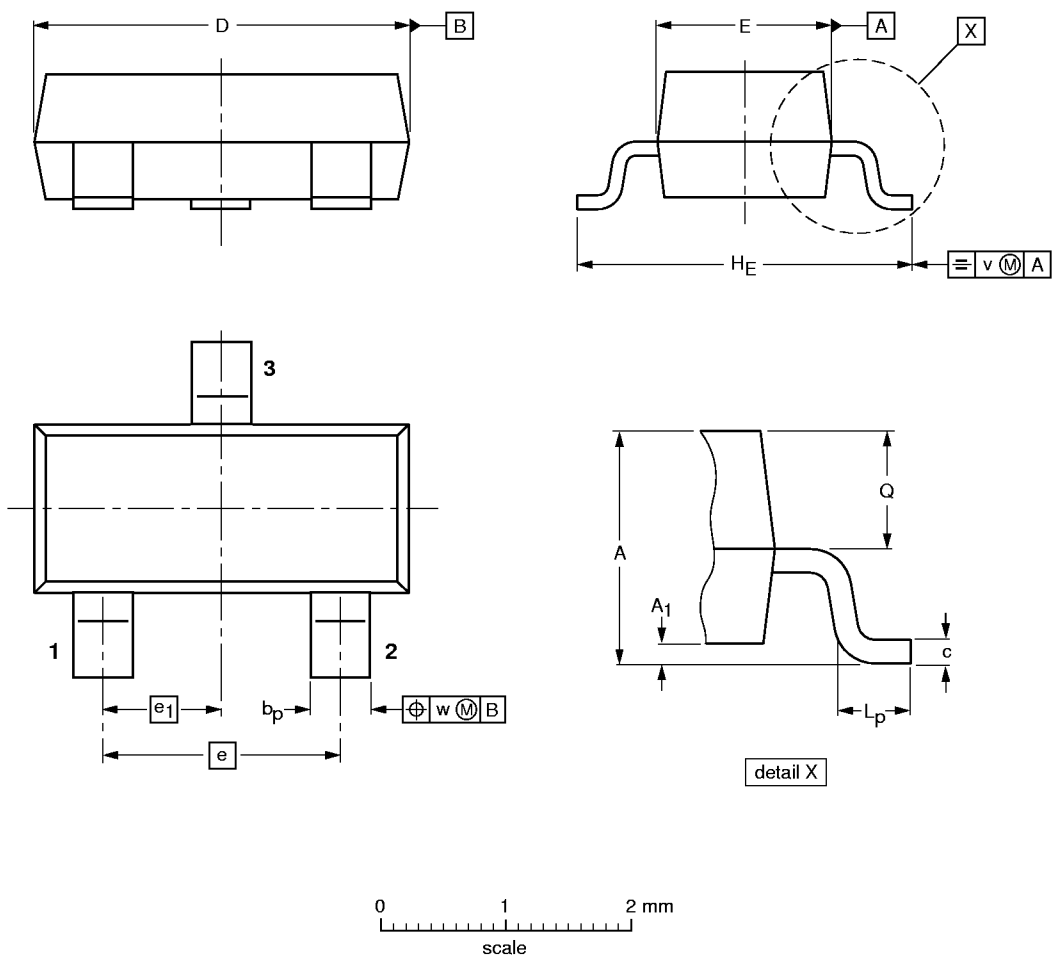


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28