8-INPUT NAND GATE

The HEF4068B provides the 8-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

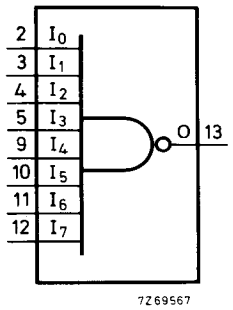

Fig. 1 Functional diagram.

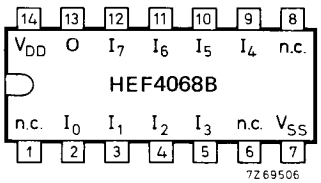

Fig. 2 Pinning diagram.

HEF4068BP : 14-lead DIL; plastic (SOT-27).
HEF4068BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4068BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

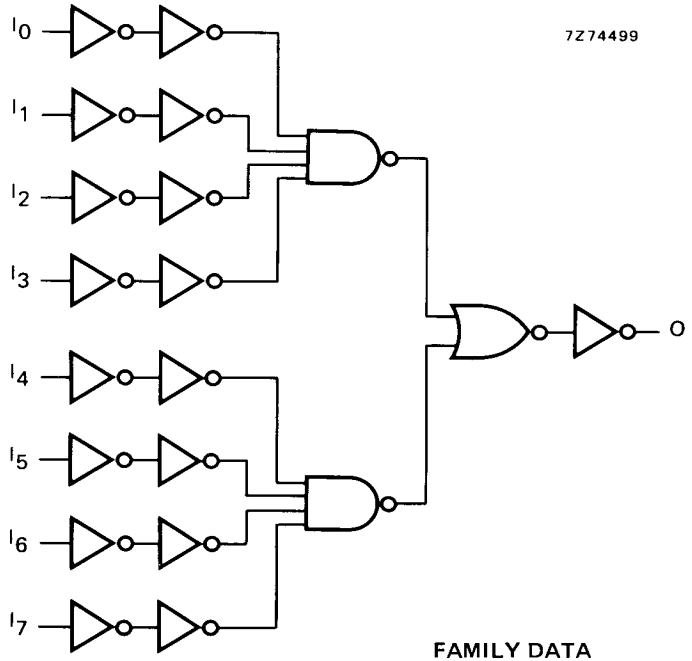

Fig. 3 Logic diagram.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O$	5		95	195	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	85	ns	29 ns + (0,23 ns/pF) C_L
	15		30	65	ns	22 ns + (0,16 ns/pF) C_L
	5		80	165	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times						
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	