GENERAL INSTRUMENT

ER5901
ER5901IR
ER5901HR

PRELIMINARY INFORMATION

1K N-Channel EEPROM

FEATURES

- 128 x 8 bit organization, fully decoded
- SNOS si-gate technology
- Single +5V power supply
- 100ns access time
- TTL compatible
- Word alterable
- Reprogramming time-user determined
- Automatic erase/write cycle

DESCRIPTION

The ER5901 is intended for microcomputer applications which require a small non-volatile memory capable of fast operation with a minimum of processor intervention. The fast access time, coupled with the ability to multiplex the address and data lines, through the Address Latch Enable (ALE) and $\overline{WE}$ inputs, will make it readily adaptable for use in most systems.

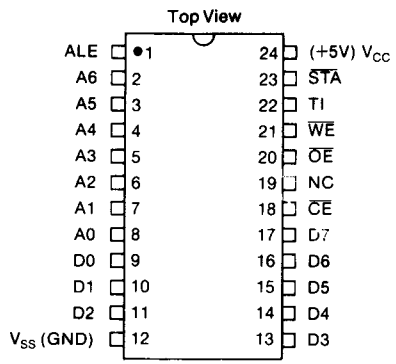
A single pulse on the $\overline{WE}$ input will cause the device to perform a complete erase/write cycle without any further processor intervention. The duration of this reprogramming cycle can be determined by means of an external RC time constant connected to the TI input. During the reprogramming cycle a busy status is made available on the status line $\overline{STA}$.

The combining of all these features on a single device has been achieved through innovative circuit design and N-channel Si-gate technology.

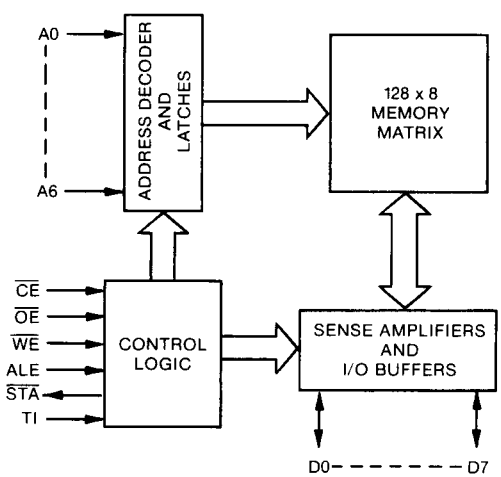
ELEC. ALTERABLE NON-VOLATILE MEMORY

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering temperature of leads (10 secs.) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±5% Volts
Operating Temperature Ranges T_A: 0°C to + 70°C (Commercial)
−40°C to +85°C (Industrial)
−55°C to +125°C (Military)

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	**	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	**	μA	V_{OUT} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	35	54	mA	V_{CC} = +5.5V
Chip Deselected	I_{CC}	—	12	18	mA	V_{CC}= +5.5V
Power Dissipation:						
Chip Selected	P_D	—	195	300	mW	V_{CC} = +5.5V
Chip Deselected	P_D	—	66	100	mW	V_{CC} = +5.5V

** To be announced at a later date.

NOTE: 1. T_A = −40°C to + 85°C, V_{CC} = 5±5% Volts, unless otherwise specified.

PIN FUNCTIONS

Name	Function
A0-A6	7 bit binary word address.
D0-D7	8 bit data I/O.
V_{CC}	Power supply +5V ± 5%.
GND	Chip Ground connection.
$\overline{CE}$	Chip Enable input — used for chip selection.
$\overline{OE}$	Output Enable input — gates data to output pins during Read.
$\overline{WE}$	Write Enable input — enables a reprogramming cycle, input data latched on a positive edge.
ALE	Address Latch Enable input — address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
$\overline{STA}$	Status output pin — low when chip is in reprogramming mode and cannot be accessed.
TI	Timing input — defines clock frequency for reprogramming; May be RC or other external clock.