AS8221

FlexRay Standard Transceiver

1 General Description

This document is subject to change without notice.

The AS8221 is a high speed automotive bus driver fully conforming to the FlexRay Electrical Physical Layer Specification V2.1 Rev B. The AS8221 operates as a bi-directional interface between the FlexRay Communication Controller and the twisted-pair copper wiring.

The AS8221 provides an optimized host controller interface consisting of three low-active pins. The Enable (EN) and Standby (STBN) input pins for mode handling by the microcontroller and the Error (ERRN) out pin where system, chip failures or status information are signalled to the microcontroller. Signalling logic high on the Enable and Standby pin the device will enter NORMAL mode in case no fault condition is given and in this mode the device is fully operational meaning FlexRay communication is possible. Additionally, a RECEIVE-ONLY mode is implemented, which can be accessed by the microcontroller where only FlexRay streams can be received in order to avoid unwanted disturbances on the FlexRay bus while listening to the bus traffic. In the low-power modes (STANDBY and SLEEP mode) very low power consumption is achieved.

In case of undervoltage at one of the supply voltages (V_{BAT}, V_{CC}, and V_{IO}) the device will change its mode to a low-power mode (either STANDBY or SLEEP mode) and the device will signal an error accordingly. In case of low voltage is detected on both V_{BAT} and V_{CC} the device will enter the POWER-OFF mode, where no operation is possible. A safe mechanism from the low-power modes to POWER-OFF mode and vice versa is implemented ensuring that no deadlock can happen during the startup phase.

Ensuring application in safety critical environments a two wire bus-guardian interface is implemented where additional monitoring circuitries on the electronic-control-unit can activate and deactivate the transmitter and additionally on the receive enable output (RxEN) in low-power modes the wake conditions and in normal power modes the received FlexRay streams can be monitored.

A thermal sensor circuit with an integral shutdown mechanism prevents damage to the device in extreme temperature conditions. The symmetrical transient control for the high- and low-side driver for both the bus-minus (BM) and bus-plus (BP) line allows an ideal balance of communications over different network topologies, with excellent EMC performance.

2 Key Features

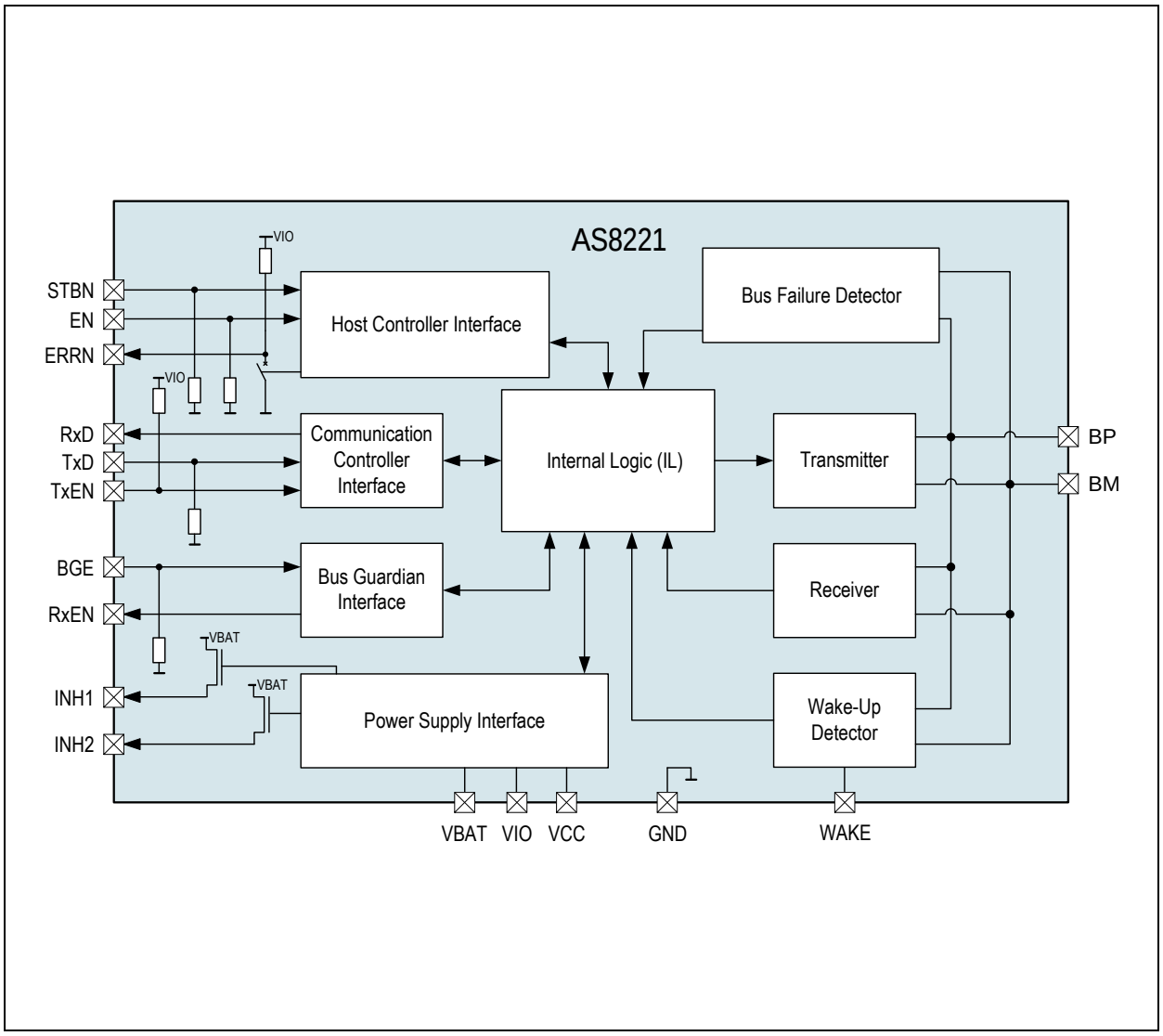
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev. B
- Data transfer up to 10 Mbps
- Excellent EMC performance. High common mode range ensure excellent EMI
- Interface for Bus Guardian or supervision circuits
- Automatic thermal shutdown protection
- Supports 12V and 24V systems with very low sleep current
- Integrated power management system
  - Two inhibit pins for external voltage supply control
  - Local wake-up input
  - Remote wake-up capability via FlexRay bus in low-power modes
- Supports 2.5V, 3V, 3.3V, 5V microcontrollers, automatic adaptation to digital interface levels
- Protection against damage due to short circuit conditions on the bus (positive and negative battery voltage)
- Operating temperature range -40ºC to +125ºC
- Lead-free SSOP20 package

3 Applications

The AS8221 FlexRay Standard Transceiver is best fitting for automotive FlexRay nodes where bus wake-up and voltage regulator control for voltage supplies is needed.

The device addresses all ECUs connected to the permanent battery supply (clamp 30). The AS8221 can be used as only ECU wake-up component with very low power consumption in SLEEP mode.

Figure 1. AS8221 FlexRay Standard Transceiver Block Diagram



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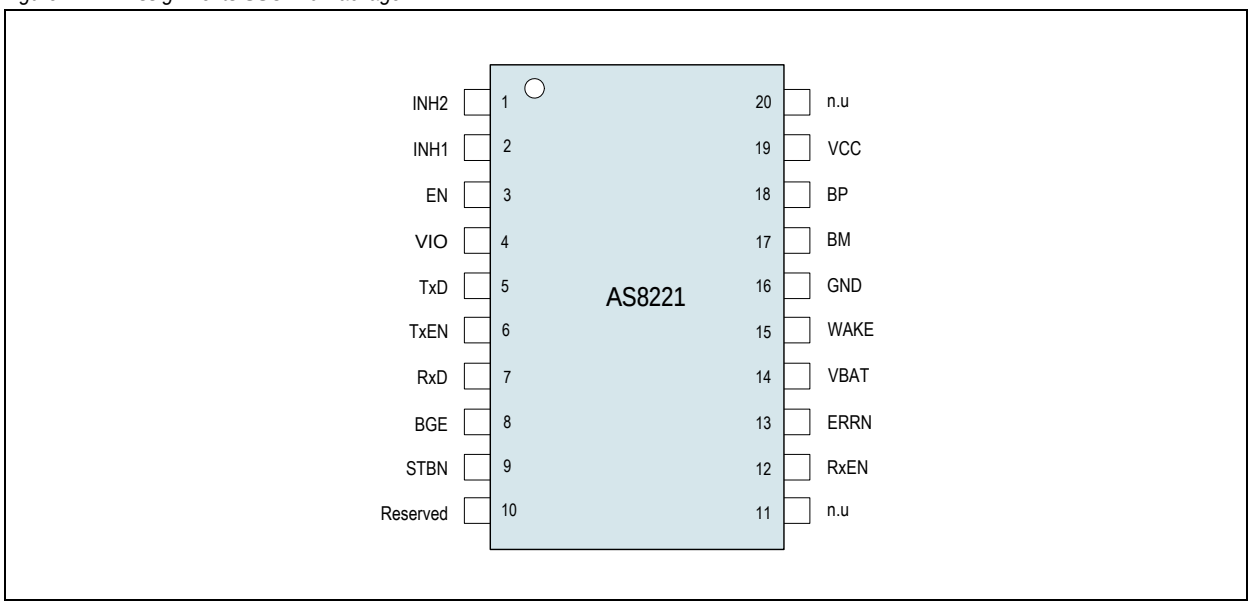
4 Pin Assignments

Figure 2. Pin Assignments SSOP20 Package



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
INH2	1	Analog I/O	**Analog Output.** Inhibit 2 output for switching external voltage regulator
INH1	2		**Analog Output.** Inhibit 1 output for switching external voltage regulator
EN	3	Digital input with pull-down	**Digital Input.** Enable input
VIO	4	Supply pad	**Supply Voltage.** I/O supply voltage
TxD	5	Digital input with pull-down	**Digital Input.** Transmit data input
TxEN	6	Digital input with pull-up	**Digital Input.** Transmitter enable input
RxD	7	Digital output	**Digital Output.** Receive data output
BGE	8	Digital input with pull-down	**Digital Input.** Bus guardian enable input
STBN	9		**Digital Input.** Standby input
Reserved	10	Analog/digital input/output with pull-down	To be connected to GND or to be unconnected
Not used	11	-	
RxEN	12	Digital output	**Digital Output.** Receive data enable output
ERRN	13		**Digital Output.** Error diagnosis output and wake status output
VBAT	14	Supply pad	**Supply Voltage.** Battery supply voltage
WAKE	15	Analog I/O	**Analog Input.** Local wake-up input
GND	16	Supply pad	**Ground**
BM	17	Analog I/O	**Analog Input/Output.** Bus line Minus
BP	18		**Analog Input/Output.** Bus line Plus
VCC	19	Supply pad	**Supply voltage**
Not used	20	-	

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Battery Supply Voltage (V_{BAT})	-0.3	+50	V	
Supply Voltage (V_{CC})	-0.3	+7.0	V	
Supply Voltage (V_{IO})	-0.3	+7.0	V	
DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-0.3	V_{IO} + 0.3	V	$V_{IO} < V_{CC}$
DC Voltage on pin WAKE, INH1, INH2	-0.3	V_{BAT} + 0.3		
DC Voltage at BP and BM	-40	+50	V	
Input current (latchup immunity)	-100	100	mA	According to JEDEC 78
Electrostatic discharge (V_{ESD})	±4		kV	BP, BM, V_{BAT} and Wake pin according AEC-Q100-002 (HBM)
	±2		kV	All other pins according to AEC-Q100-002 (HBM)
	±3		kV	BP and BM according to FlexRay Physical Layer EMC Measurement Specification Version 3.0
	±500		V	On all pins AEC-Q100-011 (Charge Device Model)
	±750		V	Corner pins AEC-Q100-011 (Charge Device Model)
	±100		V	AEC-Q100-003 (Machine Model)
Transient voltage on BP, BM	-200	+200	V	According to ISO7637 part3 test pulses a and b; class C; RL=45 Ω, CL= 100 pF; (see Figure 18 on page 30).
Transient voltage on V_{BAT}	-200	+200	V	According to ISO7637 part2 test pulses 1, 2, 3a and 3b; class C; RL=45Ω, CL= 100pF; (see Figure 18 on page 30).
	+6.5	+50	V	According to ISO7637 part2 test pulse 4; class C; RL=45Ω, CL= 100pF; (see Figure 18 on page 30).
		+50		According to ISO7637 part2 test pulse 5b; class C; RL=45Ω, CL= 100pF; (see Figure 18 on page 30).
Total power dissipation (all supplies and outputs)		150	mW	
Storage temperature	-55	+150	°C	
Junction temperature	-40	+150	°C	
Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

6 Electrical Characteristics

T_{vj} = -40 to +150 ºC, V_{CC}= +4.75V to +5.25V, V_{BAT}= 5.5V to +50V, V_{IO} = +2.2 to V_{CC}, R_L= 45Ω, C_L= 100 pF, unless otherwise specified.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage						
T_{AMB}	Ambient temperature		-40	+25	+125	ºC
V_{CC}-V_{IO}	Difference of supplies		-0.1		3.05	V
I_{BAT}	V_{BAT} current consumption	V_{BAT}=12V; low-power modes T_{vj} < 125ºC (see footnote 1)	0	26	50	µA
		V_{BAT}=12V; low-power modes T_{vj} < 150ºC	0		100	µA
		Non-low-power modes	0	0.15	1	mA
I_{CC}	V_{CC} current consumption	Low-power Modes V_{CC} = 0V to +5.25V (see footnote 1)	-5	8	20	µA
		Non-low-power modes: NORMAL, driver enabled;	0	29	45	mA
		Non-low-power modes: NORMAL, driver enabled; R_{BUS} = ∞Ω	0	7	15	mA
		Non-low-power modes: RECEIVE-ONLY	0	2.0	10	mA
I_{IO}	V_{IO} current consumption	Low-power modes V_{IO} = 0V to +5.25V	-5	1	5	µA
		Non-low power modes	0	15	1000	µA
State Transitions						
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set		1	9	50	µs
t_{STBN_RxEN}	Delay STBN high to RxEN high with wake flag set		1	9	50	µs
t_{SLEEP_INH1}	Delay STBN high to INH1 high	INH1 high = 80% V_{BAT}	1	11	50	µs
$t_{STANDBY\_INH2}$	Delay STBN high to INH2 high	INH2 high = 80% V_{BAT}	1	11	50	µs
t_{SLEEP}	GO-TO-SLEEP hold time	INH1 low = 20% V_{BAT}	10	26	70	µs
Transmitter						
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in NORMAL mode (Data0)	$V_{BPdata0}$ - $V_{BMdata0}$; 40 ≤ R_L ≤ 55Ω	-2	-1	-0.6	V
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in NORMAL mode (Data1)	$V_{BPdata1}$ - $V_{BMdata1}$; 40 ≤ R_L ≤ 55Ω	0.6	1	2	V
ΔV_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	$V_{BUS\_DIFF\_D0}$ - $V_{BUS\_DIFF\_D1}$ 40 ≤ R_L ≤ 55Ω	-200	0	200	mV
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data0 in non-low-power modes	$V_{BPdata0}$/2 + $V_{BMdata0}$/2 40 ≤ R_L ≤ 55Ω	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data1 in non-low-power modes	$V_{BPdata1}$/2 + $V_{BMdata1}$/2 40 ≤ R_L ≤ 55Ω	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	$V_{BUS\_COM\_D0}$ - $V_{BUS\_COM\_D1}$ $40 \leq R_L \leq 55\Omega$	-200	0	200	mV
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in bus idle mode	Load on BM/BM: 40Ω || 100pF		0	30	mV
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute max current when BP is shorted to BM	V_{BP}=V_{BM}		35	+100	mA
$IBP_{GNDShortMax}$	Absolute max current when BP is shorted to GND	V_{BP}= 0V		48	+100	mA
$IBM_{GNDShortMax}$	Absolute max current when BM is shorted to GND	V_{BM}= 0V		48	+100	mA
$IBP_{-5VShortMax}$	Absolute max current when BP is shorted to -5 V	V_{BP}= -5V		48	+100	mA
$IBM_{-5VShortMax}$	Absolute max current when BM is shorted to -5 V	V_{BM}= -5V		48	+100	mA
$IBP_{27VShortMax}$	Absolute max current when BP is shorted to 27 V	V_{BP}= 27V		71	+100	mA
$IBM_{27VShortMax}$	Absolute max current when BM is shorted to 27 V	V_{BM}= 27V		71	+100	mA
$IBP_{48VShortMax}$	Absolute max current when BP is shorted to 48 V	V_{BP}= 48V		72	+100	mA
$IBM_{48VShortMax}$	Absolute max current when BM is shorted to 48 V	V_{BM}= 48V		72	+100	mA
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	t_{TxD_RISE} = 5ns		22	50	ns
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	t_{TxD_FALL} = 5ns		22	50	ns
$t_{TxD\_MISMATCH}$	Delay time from TxD to BUS mismatch	t_{TxD_BUS10} - t_{TxD_BUS01}	-4	0	4	ns
t_{BUS10}	Fall time differential bus voltage	80% - 20% of V_{BUS}	3.75	12	18.75	ns
t_{BUS01}	Rise time differential bus voltage	20% - 80% of V_{BUS}	3.75	12	18.75	ns
$t_{TxEN\_BUS\_Idle\_Active}$	Delay time from TxEN to bus active			14	50	ns
$t_{TxEN\_BUS\_Active\_Idle}$	Delay time from TxEN to bus idle			10	50	ns
$t_{TxEN\_MISMATCH}$	Delay time from TxEN to bus mismatch	$\lvert t_{TxEN\_BUS\_Idle\_Active}$ - $t_{TxEN\_BUS\_Active\_Idle} \rvert$		4	50	ns
$t_{BGE\_BUS\_Idle\_Active}$	Delay time from BGE to bus active			15	50	ns
$t_{BGE\_BUS\_Active\_Idle}$	Delay time from BGE to bus idle			11	50	ns
$t_{BUS\_Idle\_Active}$	Differential bus voltage transition time: idle to active			5	30	ns
$t_{BUS\_Active\_Idle}$	Differential bus voltage transition time: active to idle			2	30	ns
$t_{TxEN\_timeout}$	TxEN timeout		1.5	4.9	15	ms

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Receiver						
R_{BP}, R_{BM}	BP, BM input resistance	Idle mode; R_{BUS}=∞	10	25	40	KΩ
R_{DIFF}	BP, BM differential input resistance	Idle mode; R_{BUS}=∞	20	50	80	KΩ
V_{BPidle}, V_{BMidle}	Idle voltage in non-low-power modes on pin BP, BM	Non-low-power modes; V_{TxEN} = V_{IO} Load on BM/BM: 40Ω || 100pF	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in low-power modes on pin BP, BM	Low-power modes Load on BM/BM: 40Ω || 100pF	-0.2	0	+0.2	V
I_{BPidle}	Absolute idle output current on pin BP	-40V < V_{BP} < 50V	0	2	7.5	mA
I_{BMidle}	Absolute idle output current on pin BM	-40V < V_{BM} < 50V	0	2	7.5	mA
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	V_{BP} = V_{BM} = 5V, V_{CC} = 0V, V_{BAT} = 0V; V_{IO} = 0V	0	7	+25	µA
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	Non-low-power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM}) < 15V	150	225	400	mV
$V_{BUSActiveLow}$	Activity detection differential input voltage low	Non-low-power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	-400	-225	-150	mV
V_{Data1}	Data1 detection differential input voltage	Pre-condition: activity already detected. Non-low-power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	150	225	300	mV
V_{Data0}	Data0 detection differential input voltage	Pre-condition: activity already detected. Non-low-power modes; $V_{RECEIVE\_COM}$: -10V < (V_{BP}, V_{BM})< 15V	-300	-225	-150	mV
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	2 x (| | V_{Data0}| - | V_{Data1}| |) / (| V_{Data0}| +| V_{Data1}|) (see footnote 2)			10	%
$V_{RECEIVE\_COM}$	Max. common mode voltage range when receiving	Non-low-power modes	-10		+15	V
t_{BUS_RxD10}	Delay from BUS to RxD negative edge	C_{RxD} = 15 pF (see footnote 3)		36	80	ns
t_{BUS_RxD01}	Delay from BUS to RxD positive edge	C_{RxD} = 15 pF (see footnote 3)		36	80	ns
t_{BIT}	Bit time	C_{RxD} = 15 pF (see footnote 3)	54			ns
t_{RxD_ASYM}	Delay time from BUS to RxD mismatch	C_{RXD}=15 pF; |t_{BUS_RxD10}- t_{BUS_RxD01}| (see footnote 3) (see footnote 4)		0	5	ns
t_{RxD_FALL}	Fall time RxD voltage	80% - 20% of V_{RxD}; C_{RxD}=15 pF (see footnote 3)		2	5	ns

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RxD_RISE}	Rise time RxD voltage	20% - 80% of VRxD; CRxD=15 pF (see footnote 3)		2	5	ns
$t_{BUSIdleDetection}$	Idle detection time	V_{BUS}: 400mV → 0V	50	173	200	ns
$t_{BUSActivityDetection}$	Activity detection time	V_{BUS}: 0V → 400mV	100	173	250	ns
$t_{BUSIdleReaction}$	Idle reaction time	V_{BUS}: 400mV → 0V	50	192	300	ns
$t_{BUSActivityReaction}$	Activity reaction time	V_{BUS}: 0V → 400mV	100	200	350	ns
Wake-Up Detector						
t_{BWU_D0}	Data0 detection time in remote wake-up pattern	-10V < (V_{BP}, V_{BM}) < 15V	1	2	4	µs
t_{BWU_Idle}	Idle or Data1 detection time in remote wake-up pattern	-10V < (V_{BP}, V_{BM}) < 15V	1	2	4	µs
t_{BWU_Detect}	Total remote wake-up detection time	-10V < (V_{BP}, V_{BM}) < 15V	48	73	140	µs
V_{BWUTH}	Bus wake-up detection threshold	-10V < (V_{BP}, V_{BM}) < 15V	-300	-250	-150	mV
V_{LWUTH}	Local wake-up detection threshold		2	2.8	4	V
I_{LWUL}	Low level input current on local WAKE pin	V_{BAT} = 12V; V_{LWAKE} = 2V for t < $t_{LWUFilter}$	-20	-10	-5	µA
I_{LWUH}	High level input current on local WAKE pin	V_{BAT} = 12V; V_{LWAKE} = 4V for t < $t_{LWUFilter}$	5	11	20	µA
$t_{LWUFilter}$	Local wake filter time		1	20	40	µs
Supply Voltage Monitor						
V_{BATTHH}	V_{BAT} undervoltage recovery threshold		3.5	4	4.5	V
V_{BATTHL}	V_{BAT} undervoltage detection threshold		2.5	3	3.5	V
V_{CCTHH}	V_{CC} under-voltage recovery threshold		3.5	4	4.5	V
V_{CCTHL}	V_{CC} undervoltage detection threshold		2.5	3	3.5	V
V_{IOTHH}	V_{IO} undervoltage recovery threshold		1.25	1.6	2.0	V
V_{IOTHL}	V_{IO} undervoltage detection threshold		0.75	1.1	1.5	V
t_{UV_DETECT}	Detection time for undervoltage at V_{BAT}, V_{CC}, V_{IO}		100	300	700	ms
t_{UV_REC}	Detection time for undervoltage recovery at V_{BAT}, V_{CC}, V_{IO}		0.7	2	5	ms
Bus Error Detection						
I_{THL}	Absolute bus current for low current detection	NORMAL mode, Transmitter enabled		5		mA
I_{THH}	Absolute bus current for high current detection	NORMAL mode, Transmitter enabled		40		mA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	NORMAL mode, Transmitter enabled		225		mV
t_{BUS_ERROR}	Bus error detection time	NORMAL mode, Transmitter enabled		20		µs
Over Temperature						
OT_{TH}	Over temperature threshold		150	171	180	°C
OT_{TL}	Over temperature hysteresis		10	13	20	°C
Power Supply Interface						
ΔV_{OINH}	High level voltage drop on INH1, INH2	I_{INH} = 0.2mA, V_{BAT} = 5.5V	0	0.15	0.8	V
$\lvert I_{IL} \rvert$	Leakage current	SLEEP mode, V_{INH} = 0V		0	5	µA
Communication Controller Interface						
V_{TxDIH}	Threshold for detecting TxD as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
V_{TxDIL}	Threshold for detecting TxD as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
I_{TxDIH}	TxD high level input current		30	52	100	µA
I_{TxDIL}	TxD low level input current		-5	0	5	µA
V_{TxENIH}	Threshold for detecting TxEN as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
V_{TXENIL}	Threshold for detecting TxEN as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
I_{TxENIH}	TxEN high level input current		-5	0	5	µA
I_{TxENIL}	TxEN low level input current		-100	-50	-30	µA
V_{RxDOH}	RxD high level output voltage	I_{RxD} = -4mA, V_{IO} = 5V	0.8 * V_{IO}	0.9 * V_{IO}	1.0 * V_{IO}	V
V_{RxDOL}	RxD low level output voltage	I_{RxD} = 4mA, V_{IO} = 5V	0	0.1 * V_{IO}	0.2 * V_{IO}	V
Host Interface						
V_{STBNIH}	Threshold for detecting STBN as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
V_{STBNIL}	Threshold for detecting STBN as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
I_{STBNIH}	STBN high level input current		30	52	100	µA
I_{STBNIL}	STBN low level input current		-5	0	5	µA
$t_{STBN\_DEB\_LP}$	STBN de-bouncing time low-power modes		0.1	1	40	µs
$t_{STBN\_DEB\_NLP}$	STBN de-bouncing time non-low-power modes		0.1	1	2	µs
V_{ENIH}	Threshold for detecting EN as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
V_{ENIL}	Threshold for detecting EN as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
I_{ENIH}	EN high level input current		30	50	100	µA
I_{ENIL}	EN low level input current		-5	0	5	µA

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{EN\_DEB\_LP}$	EN de-bouncing time low-power modes		0.1	1	40	µs
$t_{EN\_DEB\_NLP}$	EN de-bouncing time non-low-power modes		0.1	1	2	µs
V_{ERRNOH}	ERRN high level output voltage	I_{ERRN} = -4mA, V_{IO} = 5V	0.8 * V_{IO}	0.9 * V_{IO}	1.0 * V_{IO}	V
V_{ERRNOL}	ERRN low level output voltage	I_{ERRN} = 4mA, V_{IO} = 5V	0	0.1 * V_{IO}	0.2 * V_{IO}	V
Bus Guardian Interface						
V_{BGEIH}	Threshold for detecting BGE as on logical high			0.48 * V_{IO}	0.7 * V_{IO}	V
V_{BGEIL}	Threshold for detecting BGE as on logical low		0.3 * V_{IO}	0.48 * V_{IO}		V
I_{BGEIH}	BGE high level input current		30	51	100	µA
I_{BGEIL}	BGE low level input current		-5	0	5	µA
V_{RxENOH}	RxEN high level output voltage	I_{RxEN} = -4mA, V_{IO} = 5V	0.8 * V_{IO}	0.9 * V_{IO}	1.0 * V_{IO}	V
V_{RxENOL}	RxEN low level output voltage	I_{RxEN} = 4mA, V_{IO} = 5V	0	0.1 * V_{IO}	0.2 * V_{IO}	V
Read Out Interface						
$t_{RO\_EN\_ERRN}$	Propagation delay falling edge EN to ERRN			2	4.5	µs
$t_{RO\_EN\_TIMEOUT}$	error-read-out timeout		25	50	100	µs

1. EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN, LWAKE, INH1, INH2: open
2. Test condition: (VBP + VBM) / 2 = 2,5V) ± 5%
3. For test signal (see Figure 17)
4. Guaranteed at specified bit time t_{BIT}

7 Typical Operating Characteristics

Figure 3. Bus Differential Voltage

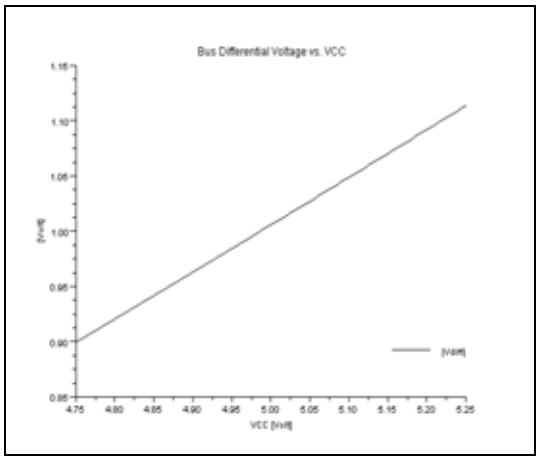


Figure 4. Bus Absolute Voltage

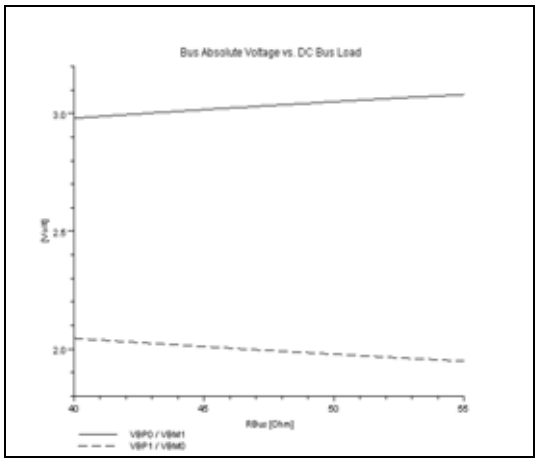


Figure 5. Bus Differential Voltage

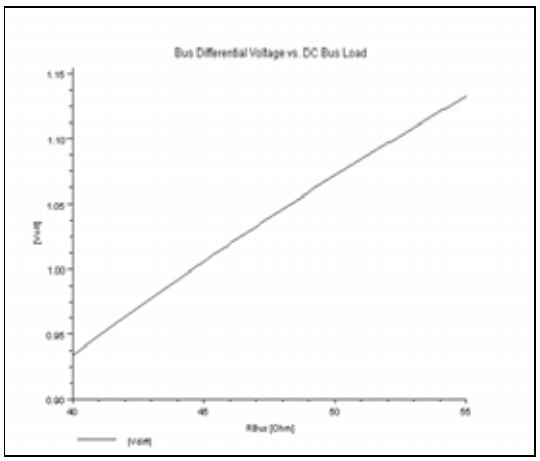
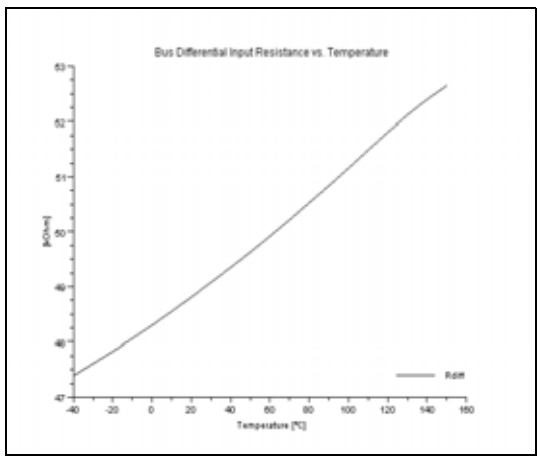


Figure 6. Bus Differential Input Resistance



8 Detailed Description

The AS8221 is a FlexRay Transceiver operating as an interface between the Communication Controller and the wired bus lines. The AS8221 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The drivers are short circuit protected against the positive and negative supply voltage to increase the robustness and reliability of automotive systems. The AS8221 operates at baudrates up to 10 Mbps.

8.1 Block Description

The AS8221 consists of 9 functional blocks (see Figure 1):

Table 4. Functional Blocks

Functional Block	Short Description
Host Controller Interface (HCI)	Digital interface between the Transceiver and the host controller (HC) The host interface comprises the read-out handler, which delivers failure and status information via the ERRN pin to the host controller.
Communication Controller Interface (CCI)	Digital interface between the Transceiver and the FlexRay communication controller (CC)
Bus Guarding Interface (BGI)	Digital interface between the Transceiver and the FlexRay bus guardian (BG) or monitoring circuitry.
Power Supply Interface (PSI)	The power supply interface consists of the voltage monitor (VM) with two analog inhibit outputs switching external voltage supplies.
Internal Logic (IL)	The digital signals from the functional blocks of the device are fed into the internal logic where the forwarding of FlexRay messages from analog side to digital interfaces and vice versa is done. The state machine is embedded in the Internal Logic and the handling of error, wake, and power-on flags is executed herein.
Bus Failure Detector (BFD) Temperature Protection (TP)	The bus failure detector is directly connected to the bus pins, in order to detect several external failure conditions which may occur on the bus. The temperature protection turns off the output driver when reaching the specified internal temperature in order to protect the device.
Transmitter	The transmitter provides the differential signalling according the FlexRay standard on the bus pins.
Receiver	The Receiver captures FlexRay valid signals at the bus pins and provides the received data streams to the Internal Logic.
Wake-Up Detector (WUD)	The wake-up detector recognizes valid wake-up frames on the bus, recognizes a wake signal on the local WAKE pin and signals valid wake-up events to the Internal Logic.

8.2 Events

Transitions in order to change between the operation modes are possible only if events are detected. The device supports three type of events, events on the host controller interface (STBN, EN), detection of undervoltage or supply voltage recovery and wake events. Mode changes are only performed upon detected events.

8.3 Operating Modes

The AS8221 provides the following operating modes:

- NORMAL: non-low-power mode
- RECEIVE-ONLY: non-low-power mode
- STANDBY: low-power mode
- GO-TO-SLEEP: low-power mode
- SLEEP: low-power mode

8.3.1 NORMAL Mode

In this mode the Transceiver is able to send and receive data signals on the bus. TxEN and BGE enables and disables the transmission of data streams. INH1 and INH2 outputs are set high. RxD reflects bus data and bus state. The error-read-out-mechanism is enabled. In NORMAL mode, the transmitter state can be selected as shown in the Table 5. In case the over-temperature flag is set the Transmitter will be disabled. The bus wires are terminated to VCC/2 via Receiver input resistances.

Table 5. Transmitter State

BGE	TxEN	TxD	Transmitter state	Bus State
H	L	H	Enabled	Data1 (BP is driven high, BM is driven low)
H	L	L	Enabled	Data0 (BP is driven low, BM is driven High)
X	H	X	Disabled	Idle (BP and BM are not driven)
L	X	X	Disabled	Idle (BP and BM are not driven)

- If the differential bus voltage is higher than $V_{BUSActiveHigh}$ or lower than $V_{BUSActiveLow}$ for a time longer than $t_{BUSActivityDetection}$, then activity is detected on the bus (Bus = active), RxEN is switched to logical “low” and RxD is released.
- If, after the activity detection, the differential bus voltage is higher than V_{Data1}, RxD is high.
- If, after the activity detection, the differential bus voltage is lover than V_{Data0}, RxD is low.
- If the absolute differential bus voltage is lower than $V_{BUSActiveHigh}$ and higher than $V_{BUSActiveLow}$ for a time longer than $t_{BUSIdleDetection}$, then idle is detected on the bus (Bus = idle), RxEN and RxD are switched to logical “high”

8.3.2 RECEIVE-ONLY Mode

In RECEIVE-ONLY mode the Transmitter is disabled but the Receiver is active.

8.3.3 STANDBY Mode

In this mode the Transceiver is not able to send and receive data signals from the bus, but the wake-up detector is active. The power consumption is significantly reduced with respect to the non-low-power operation modes. RxD and RxEN, reflects the negation of the wake-up flag. INH1 is set to high. If wake-up flag is set then INH2 is high, otherwise it is floating. The error-read-out-mechanism is not enabled. The bus wires are terminated to GND (bus state: Idle_LP).

8.3.4 GO-TO-SLEEP Mode

In this mode the Transceiver has the same behavior as in STANDBY mode but if this mode is selected for a time longer than t_{SLEEP} and the wake flag is cleared the device enters into the SLEEP mode.

8.3.5 SLEEP Mode

In SLEEP mode only the bus wake and local wake detection is enabled. IN1 and INH2 are floating.

8.4 Non Operating Mode

The AS8221 provides the following non operating mode:

8.4.1 POWER-OFF

In this mode the Transceiver is not able to operate. RxD, RxEN are set to high and ERRN is set to low. INH1 and INH2 are floating. The bus wires are not connected to GND (bus state: Idle_HZ).

8.5 Undervoltage Events

The device monitors the following three voltage supplies:

- V_{BAT}: Battery supply voltage
- V_{IO}: Supply voltage for I/O digital level adaptation
- V_{CC}: Supply voltage (+5V)

8.5.1 Undervoltage/Voltage Recovery V_{BAT}

If V_{BAT} voltage falls below V_{BATTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{BAT} flag is set and it is reset if V_{BAT} exceeds the voltage threshold V_{BATTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all the modes.

8.5.2 Undervoltage/Voltage Recovery V_{IO}

If V_{IO} voltage falls below V_{IOTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{IO} flag is set and it is reset if V_{IO} exceeds the voltage threshold V_{IOTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all the operation modes. The flag is automatically reset at POWER-OFF.

8.5.3 Undervoltage/Voltage Recovery V_{CC}

If V_{CC} voltage falls below V_{CCTHL} for a time longer than t_{UV_DETECT} then the undervoltage V_{CC} flag is set and it is reset if V_{CC} exceeds the voltage threshold V_{CCTHH} for a time longer than t_{UV_REC} or in case a wake-up event has been detected. The flag can be set or reset in all operation modes. The flag is automatically reset at POWER-OFF.

8.6 Power On/Off Events

- Starting from POWER-OFF mode a power on event occurs in case V_{BAT} undervoltage flag is reset.
- Starting from every operation mode a POWER-OFF event occurs in case V_{BAT} and V_{CC} undervoltage flags are set.

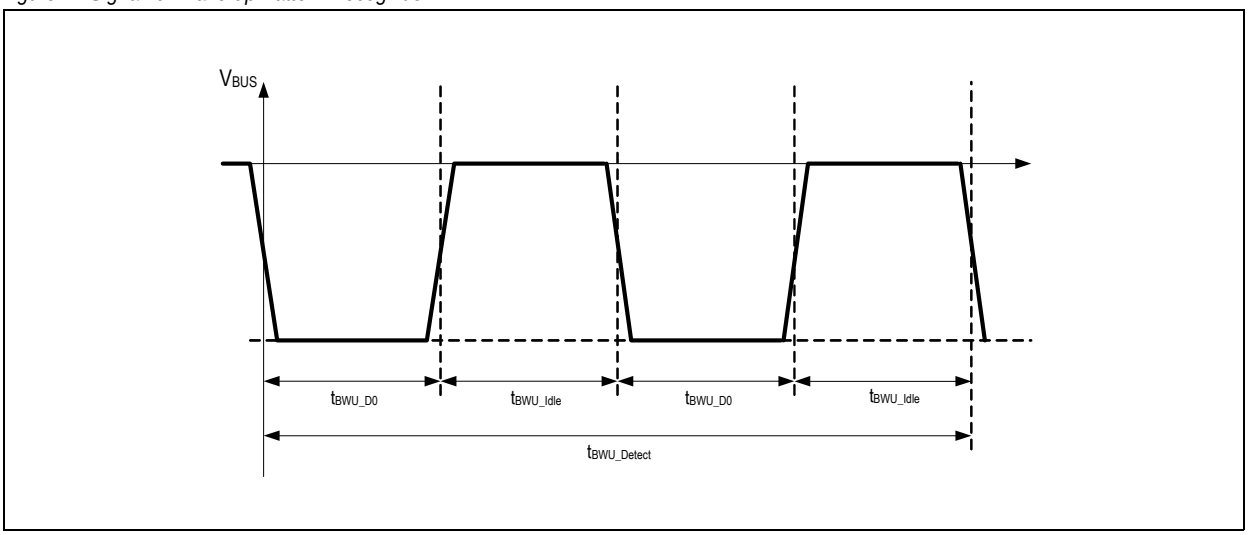
8.7 Wake-Up Events

A wake-up event can be detected only in low-power modes. The wake-up flag is set if the remote or local wake flag is set. The wake-up flag is reset if both the remote and local wake-up flags are reset. The remote wake-up flag is set if a remote wake-up event occurs. The local wake-up flag is set if a local wake-up event occurs. The remote and local wake-up flags are reset entering a low-power mode from a non-low-power mode, entering NORMAL mode, whenever an undervoltage event occurs and at POWER-OFF.

8.7.1 Remote Wake-Up Event

A remote wake-up event, only possible in low-power mode, consists in the reception of at least two consecutive wake-up symbols via the bus within t_{BWU_Detect}. The wake-up symbol is defined as Data0 longer than t_{BWU_D0} followed by idle or Data1 longer than t_{BWU_Idle} as in Figure 7 unless an undervoltage or wake-up event is present.

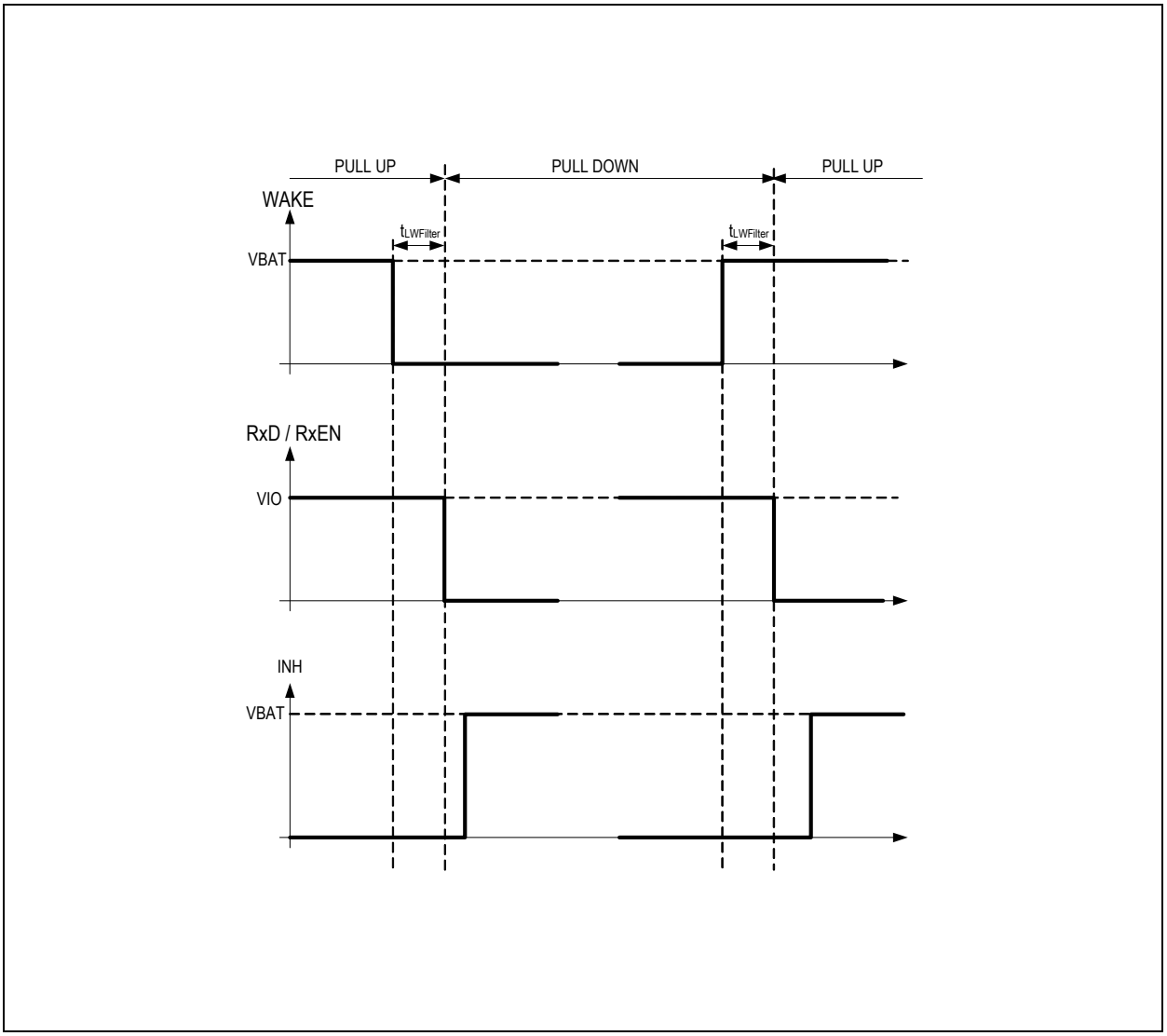
Figure 7. Signal for Wake-up Pattern Recognition



8.7.2 Local Wake-Up Event

In all low-power modes, if the voltage on the WAKE pin falls below V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-down. If the voltage on the WAKE pin rises above V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-up. The pull up and down mechanism is active in low-power and non-low-power modes.

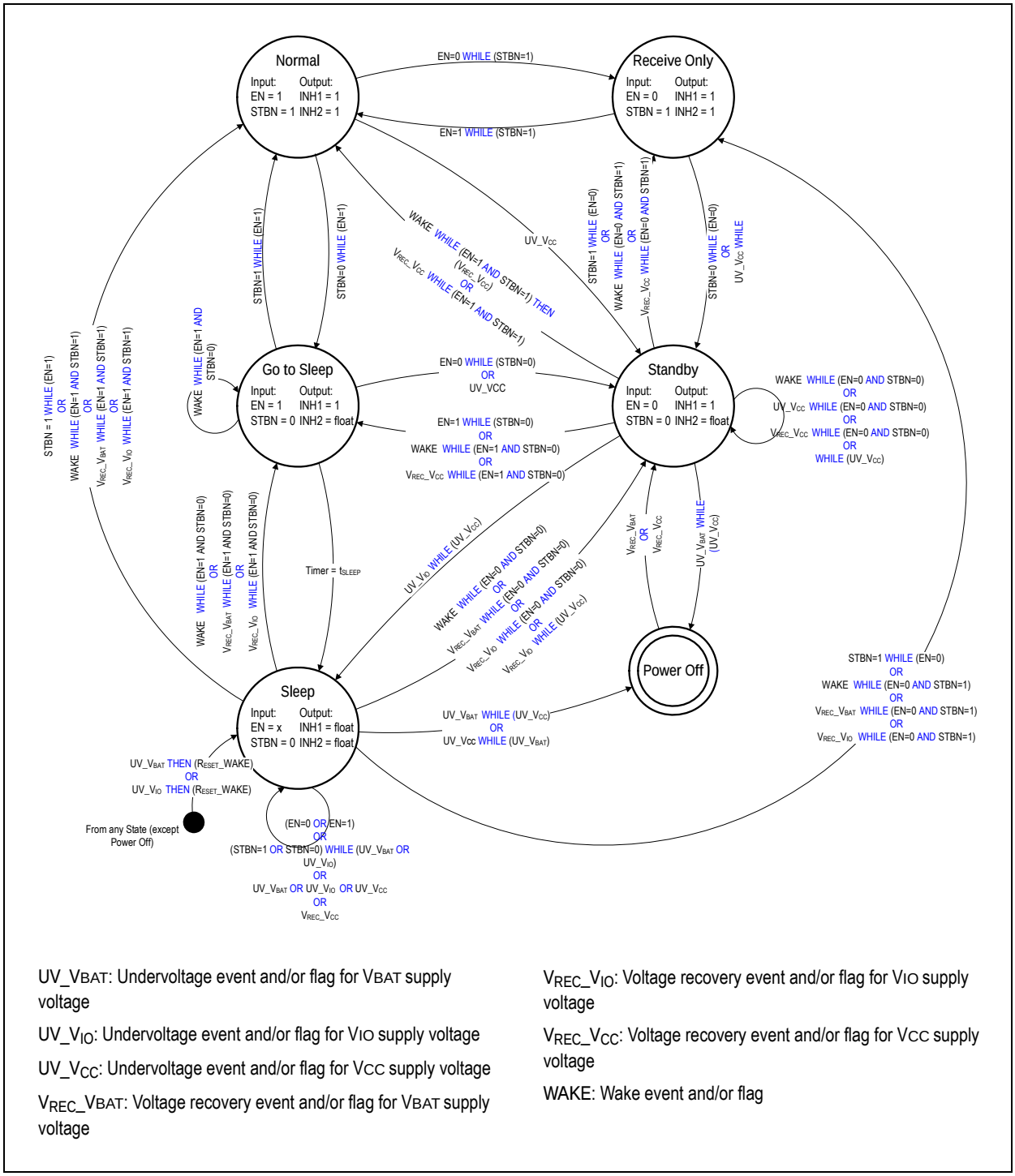
Figure 8. WAKE Input Pin Behavior



9 Application Information

System Description. Note that the state diagram does not include all the transitions described in Table 7.

Figure 9. State Diagram



UV_VBAT: Undervoltage event and/or flag for VBAT supply voltage

UV_VIO: Undervoltage event and/or flag for VIO supply voltage

UV_VCC: Undervoltage event and/or flag for VCC supply voltage

VREC_VBAT: Voltage recovery event and/or flag for VBAT supply voltage

VREC_VIO: Voltage recovery event and/or flag for VIO supply voltage

VREC_VCC: Voltage recovery event and/or flag for VCC supply voltage

WAKE: Wake event and/or flag

Prefix of "WHILE" is an event and suffix in brackets checks the flags or in case of EN and STBN the input condition. For example: VREC_VBAT WHILE (EN=0 AND STBN=0).

After the event VBAT supply voltage recovery is detected, the transition is performed if EN and STBN are "low".

9.1 Fail Silent Behavior

9.1.1 RxEN / BGE timeout

In case no edges on RxEN and BGE within $t_{TxEN\_timeout}$ are detected, the transmitter will stop transmitting the signals on RxD to the bus pins.

9.1.2 State Transitions due to Undervoltage Detection

- In case of V_{BAT} or V_{IO} undervoltage is detected, SLEEP mode will be entered regardless the status of EN and STBN.
- In case V_{CC} undervoltage is detected, STANDBY mode will be entered regardless the status of EN and STBN.
- V_{BAT} and V_{IO} undervoltage detection have higher priority than V_{CC} undervoltage detection.
- In case undervoltage at V_{BAT} and V_{CC} is detected, POWER-OFF mode is entered (bus state: Idle_HZ).

9.1.3 State Transitions due to Voltage Recovery Detection

- If the voltage recovers the device will enter the mode selected by the EN and STBN pins, in case no undervoltage is present at the other supply pins.
- Starting from the POWER-OFF, the device enters the state selected by the host input pins (EN, STBN) only if V_{BAT} or V_{CC} recovers ($V_{BAT} \geq V_{BATTHH}$ or $V_{CC} \geq V_{CCTHH}$) while V_{IO} is available (undervoltage flag of V_{IO} flag not set). If the V_{IO} undervoltage flag is set, the STANDBY mode will be entered. In both cases the Power-On flag is set.
- If $V_{BAT} \leq V_{BATTHL}$ and $V_{CC} \leq V_{CCTHL}$ the device will be in POWER-OFF state, thus the bus wires are not terminated (bus state: Idle_HZ).

9.2 Mode Transitions

In case of power-off event, the device enters POWER-OFF regardless VIO undervoltage flag, wake-up flags and regardless the selection at the host input pins.

Starting from the POWER-OFF the device enters STANDBY only in case a power on event occurs.

Starting from every operating mode the device enters SLEEP in case V_{BAT} or V_{IO} undervoltage flag is set regardless the V_{CC} undervoltage flag, the wake-up flag and the state of the host input pins.

Starting from every operating mode except SLEEP the device enters STANDBY in case V_{CC} undervoltage flag is set and V_{BAT} and V_{IO} undervoltage flags are not set, regardless the wake-up flag indication and the host input pins state.

Starting from a low-power mode the device enters the operation mode indicated by the host input pins if a wake-up event occurs.

In case all the undervoltage flags are reset the operation mode is selected by the wake-up flag and the host pins according to Table 6.

Table 6. Pin Signalling and Operating Modes

Inputs		Operation Mode	OutPut				
STBN	EN		RxD	ERRN	RxEN	INH1	INH2
H	H	NORMAL	L Bus = Data_0	NOT [Error flag]	L Bus = Active	H	H
			H Bus = Idle or Data_1		H Bus = Idle		
H	L	RECEIVE-ONLY	L Bus = Data_0	NOT [Error flag]	L Bus = Active	H	H
			H Bus = Idle or Data_1		H Bus = Idle		
L	H	GO-TO-SLEEP	NOT [Wake-up flag]	NOT [Wake-up flag]	NOT [Wake-up flag]	H	Floating
L	L	STANDBY	NOT [Wake-up flag]	NOT [Wake-up flag]	NOT [Wake-up flag]	H	Floating
L	X	SLEEP	NOT [Wake-up flag]	NOT [Wake-up flag]	NOT [Wake-up flag]	Floating	Floating
X	X	POWER-OFF	H	L	H	Floating	Floating

Where: H = Digital level high, L = Digital level low, X = Do not care!, Floating = The analog output is not driven.

Notes:

1. If GO-TO-SLEEP is selected for more than t_{SLEEP} then the device will enter SLEEP only if the wake-up flag is not set otherwise it will remain in GO-TO-SLEEP.
2. If wake-up flag is set INH2=H otherwise INH2=floating.
3. Starting from SLEEP, if the wake-up flag is set, the device enters STANDBY regardless the host pins state and UV flags. Starting from SLEEP, if the wake-up flag is not set, the only operating mode that can be entered through host pins are the non-low-power modes.

9.2.1 Operating Mode Transitions

Table 7. Transition Table

Transition		Event	Under Voltage Flag			Wake Flag	Host Input		Remarks
Start Point	Destination		VIO	VBAT	VCC		STBN	EN	
NORMAL	RECEIVE-ONLY	S	L	L	L	X	H	(1) H→L	
	STANDBY	U	L	L	(1) L→H	(2) X→L	H	H	
	GO-TO-SLEEP	S	L	L	L	(2) X→L	(1) H→L	H	sleep timer enabled
	SLEEP	U	(1) L→H	L	L	(2) X→L	H	H	
		U	L	(1) L→H		(2) X→L	H	H	
RECEIVE-ONLY	NORMAL	S	L	L	L	X	H	(1) L→H	
	STANDBY	S	L	L	L	(2) X→L	(1) H→L	L	
		U	L	L	(1) L→H	(2) X→L	H	L	
	SLEEP	U	(1) L→H	L	L	(2) X→L	H	L	
		U	L	(1) L→H	L	(2) X→L	H	L	
STANDBY	NORMAL	U	L	L	(1) H→L	L	H	H	
		W	L	L	(2) H→L	(1) L→H	H	H	
	RECEIVE-ONLY	S	L	L	L	X	(1) L→H	L	
		U	L	L	(1) H→L	L	H	L	
		W	L	L	(2) H→L	(1) L→H	H	L	
	GO-TO-SLEEP	S	L	L	L	L	L	(1) L→H	sleep timer enabled
		S	L	L	L	H	L	(1) L→H	sleep timer disabled
		U	L	L	(1) H→L	L	L	H	sleep timer enabled
		W	L	L	(2) H→L	(1) L→H	L	H	sleep timer disabled
	SLEEP	U	(1) L→H	L	L	(2) X→L	L	L	
		U	(1) L→H	L	H	L	X	X	
		U	L	(1) L→H	L	(2) X→L	L	L	
	STANDBY	W	L	L	(2) X→L	(1) L→H	L	L	
		U	L	L	(1) L→H	(2) X→L	L	L	
		U	L	L	(1) H→L	L	L	L	
		S	L	L	H	L	(1) L↔H	X	
		S	L	L	H	L	X	(1) L↔H	

Table 7. Transition Table

Transition		Event	Under Voltage Flag			Wake Flag	Host Input		Remarks
Start Point	Destination		V_{IO}	V_{BAT}	V_{CC}		STBN	EN	
GO-TO-SLEEP	NORMAL	S	L	L	L	X	(1) L→H	H	
	STANDBY	S	L	L	L	X	L	(1) H→L	
		U	L	L	(1) L→H	(2) X→L	L	H	
	SLEEP	S	L	L	L	L	L	H	$t \geq t_{SLEEP}$
		U	(1) L→H	L	L	(2) X→L	L	H	
		U	L	(1) L→H	L	(2) X→L	L	H	
	GO-TO-SLEEP	W	L	L	L	(1) L→H	L	H	sleep timer disabled
SLEEP	NORMAL	S	L	L	L	L	(1) L→H	H	
		W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	H	H	
		U	L	(1) H→L	L	L	H	H	
		U	(1) H→L	L	L	L	H	H	
	RECEIVE-ONLY	S	L	L	L	L	(1) L→H	L	
		W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	H	H	
		U	L	(1) H→L	L	L	H	L	
		U	(1) H→L	L	L	L	H	L	
	STANDBY	W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	L	L	
		U	L	(1) H→L	L	L	L	L	
		U	(1) H→L	L	L	L	L	L	
		U	(1) H→L	L	H	L	X	X	
	GO-TO-SLEEP	W	(2) X→L	(2) X→L	(2) X→L	(1) L→H	L	H	sleep timer disabled
		U	L	(1) H→L	L	L	L	H	sleep timer disabled
		U	(1) H→L	L	L	L	L	H	sleep timer disabled
	SLEEP	S	X	X	X	L	X	(1) L↔H	
		S	H	L	X	L	(1) L↔H	X	
		S	L	H	L	L	(1) L↔H	X	
		S	H	H	L	L	(1) L↔H	X	
		U	X	(1) L→H	L	L	X	X	
		U	(1) L→H	X	X	L	X	X	
		U	L	L	(1) L↔H	L	X	X	

Note: S = transition forced via EN, STBN; U = transition forced via undervoltage or voltage recovery; W = transition forced via WAKE

(1) Indicates the action, that initiates the transition

(2) Indicates the consequence after performed transition

(3) In case the wake flag is set, it is not possible to enter SLEEP mode through a Sleep command, requested by the host.

(4) In case an undervoltage on V_{BAT} and V_{CC} is detected, the device enters the POWER-OFF state.

9.2.2 ERRN Signalling

The ERRN signalling is shown in Table 8.

Table 8. ERRN Signalling

Supply Voltage Flag Event V_{IO}	RWAKE Flag	LWAKE Flag	Host Command		ERRN
			STBN	EN	
L	X	X	H	H	NOT [error flag]
L	H	X	H	L	If rising edge at EN, then NOT [error flag] else L
L	L	X	H	L	If rising edge at EN, then NOT [error flag] else H
L	L	L	L	X	H
L	L	L→H	L	X	H→L
L	L→H	L	L	X	H→L
L	H	L→H	L	X	L
L	L→H	H	L	X	L
H	X	X	X	X	L

9.3 Loss of Ground

Whenever a loss of ground is detected, the bus lines are switched Idle_HZ with the precondition that the host pins are open. Either error or no error can be indicated on the ERRN pin.

9.4 Error Flags

9.4.1 Undervoltage

- UVV_{BAT}_DET: The V_{BAT} undervoltage flag is set if the V_{BAT} voltage falls below V_{BATTHL} for longer than t_{UV_DETECT} and is reset if the V_{BAT} voltage reaches a voltage level higher than V_{BATTHH} for longer than t_{UV_DETECT}.
- UVV_{IO}_DET: The V_{IO} undervoltage flag is set if the V_{CC} voltage falls below V_{CCTHL} for longer than t_{UV_DETECT} and is reset if the V_{CC} voltage reaches a voltage level for longer than V_{CCTHH} after t_{UV_DETECT}.
- UVV_{CC}_DET: The V_{CC} undervoltage flag is set if the V_{IO} voltage falls below V_{IOTHL} for longer than t_{UV_DETECT} and is reset if the V_{IO} voltage reaches a voltage level higher than V_{IOTHH} for longer than t_{UV_DETECT}.

9.4.2 Bus Error (BUSERR)

The bus error flag is set if 2 consecutive rising edges on the TxD pin without any rising edge on the RxD pin are detected or if 2 consecutive falling edges on the TxD pin without any falling edge on the RxD pin are detected. This flag is reset if a rising edge on the TxD pin is followed by a rising edge on RxD pin before the next TxD rising edge or if a falling edge on the TxD pin is followed by a falling edge on RxD pin before the next TxD falling edge. This flag can be set or reset only in NORMAL mode when the transmitter is enabled. The flag is reset at POWER-OFF.

9.4.3 Short Circuit between BP and BM (BP_BM)

The BP_BM can only be set or reset in NORMAL mode while the driver is active (edge at TxEN) for a time longer than t_{BUS_ERROR}.

The flag is set if the absolute value of the differential voltage is lower than V_{SHORT} for a time t_{BUS_ERROR}.

The flag is reset in POWER-OFF mode and if the set condition is not fulfilled.

9.4.4 Over Temperature (OT)

This flag can only be set or reset in the non-low-power modes. The flag is set if the junction temperature exceeds OT_{TH} and it is reset if the junction temperature falls below OT_{TL}.

9.4.5 TxEN_BGE Timeout (TxEN_TO)

This flag can only be set in NORMAL mode if the driver is enabled (TxEN is low and BGE is high) for a time longer than t_{TxEN_max}. It is reset during transition on TxEN or BGE or if the device exits NORMAL mode. If the flag is set the driver is disabled.

9.4.6 Error Flag (ERROR)

The ERROR is signalled on the ERRN pin according to Table 6 and Table 8.

The flag is set if at least one of the error flags in chapters 9.4.2 to 9.4.5 is set. The flag will be reset if none of the flags in chapters 9.4.2 to 9.4.5 is set.

9.5 Status Flags

9.5.1 Local Wake Flag (LWAKE)

See chapter 8.7 Wake-Up Events on page 16

9.5.2 Remote Wake Flag (RWAKE)

see chapter 8.7 Wake-Up Events on page 16

9.5.3 Power on Flag (PWON)

The PWON is set leaving the POWER-OFF state and it is reset entering a low-power mode after a non-low-power mode.

9.6 Error Flags and Status Flags Read-Out

The readout mechanism consists of two information groups:

1. Error read-out
2. Status information read-out

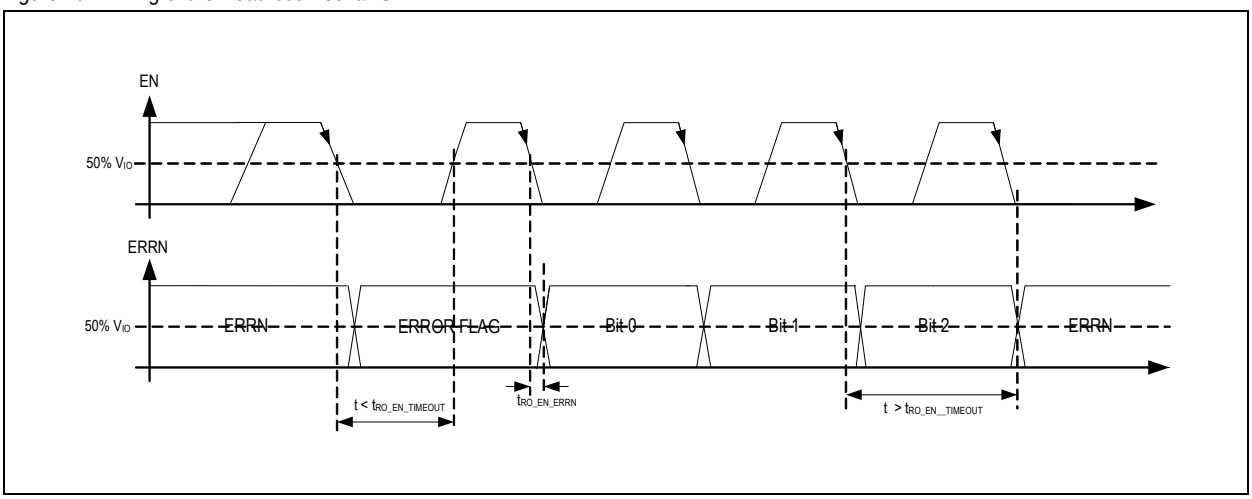
The read-out mechanism as serial transmission on Pin EN and ERRN:

Table 9. Read-out Mechanism and Transceiver States

State	Enabled / Disabled
NORMAL mode	Enabled
RECEIVE-ONLY mode	Enabled
STANDBY mode	Disabled
GO-TO-SLEEP mode	Disabled
SLEEP mode	Disabled

The error flags and the status flags can be read-out by applying a clock signal to pin EN in a non-low-power mode. A falling edge on pin EN starts the read-out loading the content of the error/status flag into the shift register and signaling the error flag on the ERRN pin. On the second falling edge the first flag (Bit 0) will be shifted out. The ERRN data is valid after $t_{RO\_EN\_ERRN}$. If EN pin keeps on toggling after the last flag (Bit 15) the next flag again is Bit 0. The complete list of bits is shown in Table 10. If no transition is detected on pin EN for longer than $t_{RO\_EN\_TIMEOUT}$ the device enters the operation mode selected by the host pins.

Figure 10. Timing of the Read-out Mechanism



9.6.1 Error and Status Flag Bit Order

Table 10. Bit Order for the Read-out Sequence

Bit	Description	Symbol
Bit 0	Undervoltage V_{BAT} detected	UVV_{BAT}_DET
Bit 1	Undervoltage V_{IO} detected	UVV_{IO}_DET
Bit 2	Undervoltage V_{CC} detected	UVV_{CC}_DET
Bit 3	Bus error	BUSERR
Bit 4	Reserved	Reserved
Bit 5		
Bit 6		
Bit 7		
Bit 8		
Bit 9		
Bit 10	Short circuit between BP and BM	BP_BM
Bit 11	Over temperature	OT
Bit 12	TxEN_BGE timeout	TxEN_TO
Bit 13	Local wake flag	LWAKE
Bit 14	Remote wake flag	RWAKE
Bit 15	Power on flag	PWON

When the read-out mechanism is started, the first data information is the Bit 0 until Bit 15 is transmitted. Any re-initiation or repetitions is started with the first data Bit 0.

9.7 Bus Driver

9.7.1 Bus States

Activity: The bus wires reflects the differential signal specified in chapter 9.9 Transmitter on page 26.

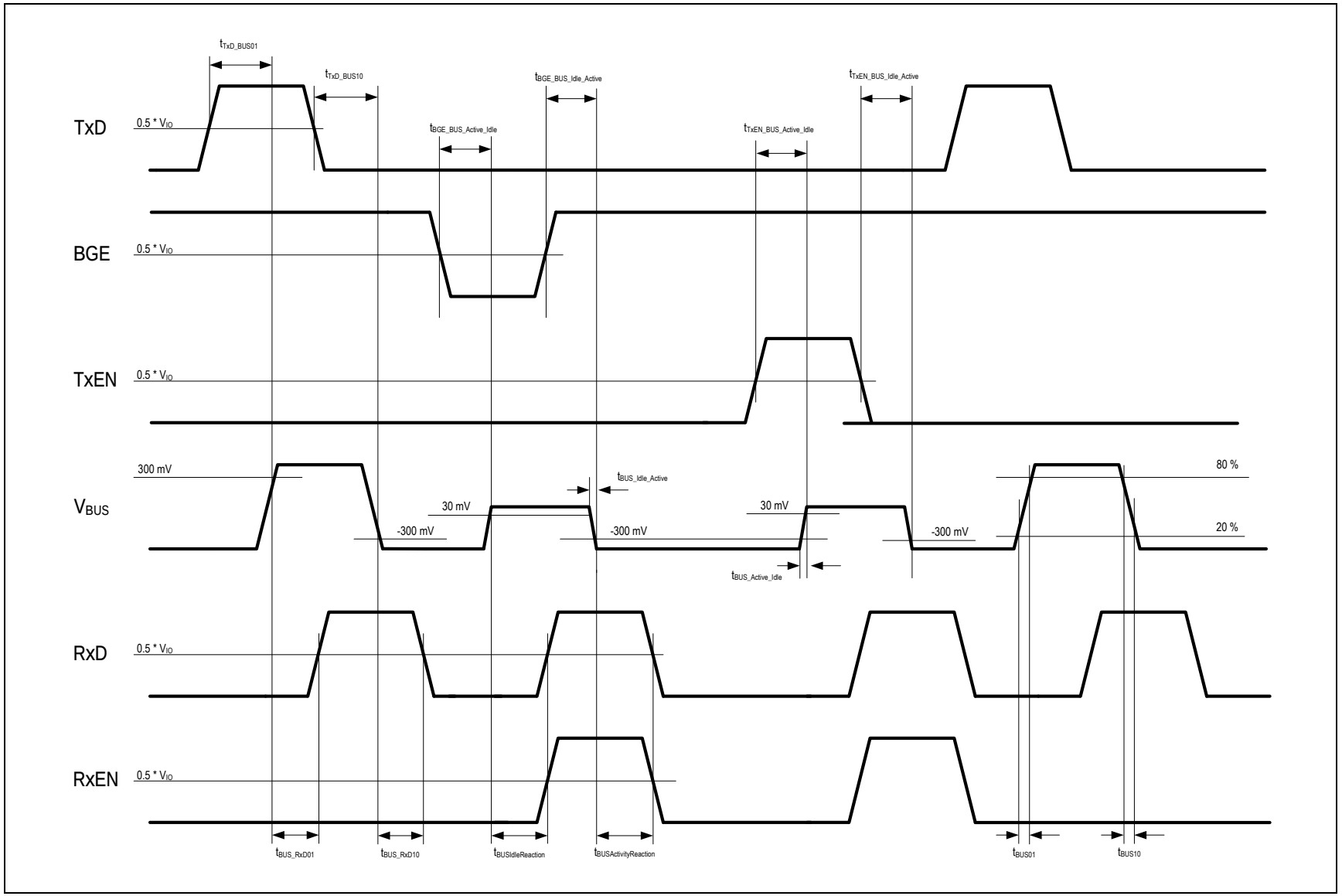
Idle: The bus wires are terminated to $V_{CC}/2$ via. receiver input resistances.

Idle_LP: The bus wires are terminated to GND via receiver input resistances.

Idle_HZ: The bus wires are not terminated to $V_{CC}/2$ via. 1MΩ

9.8 Transceiver Timing

Figure 11. Timing Diagram



9.9 Transmitter

The transmitter generates out of a digital input signal on TxD the FlexRay differential bus voltage. The transmitter is only active in NORMAL mode if BGE is on logical high and TxEN is on logical low.

Figure 12. Transmitter Characteristics (TxD → BUS)

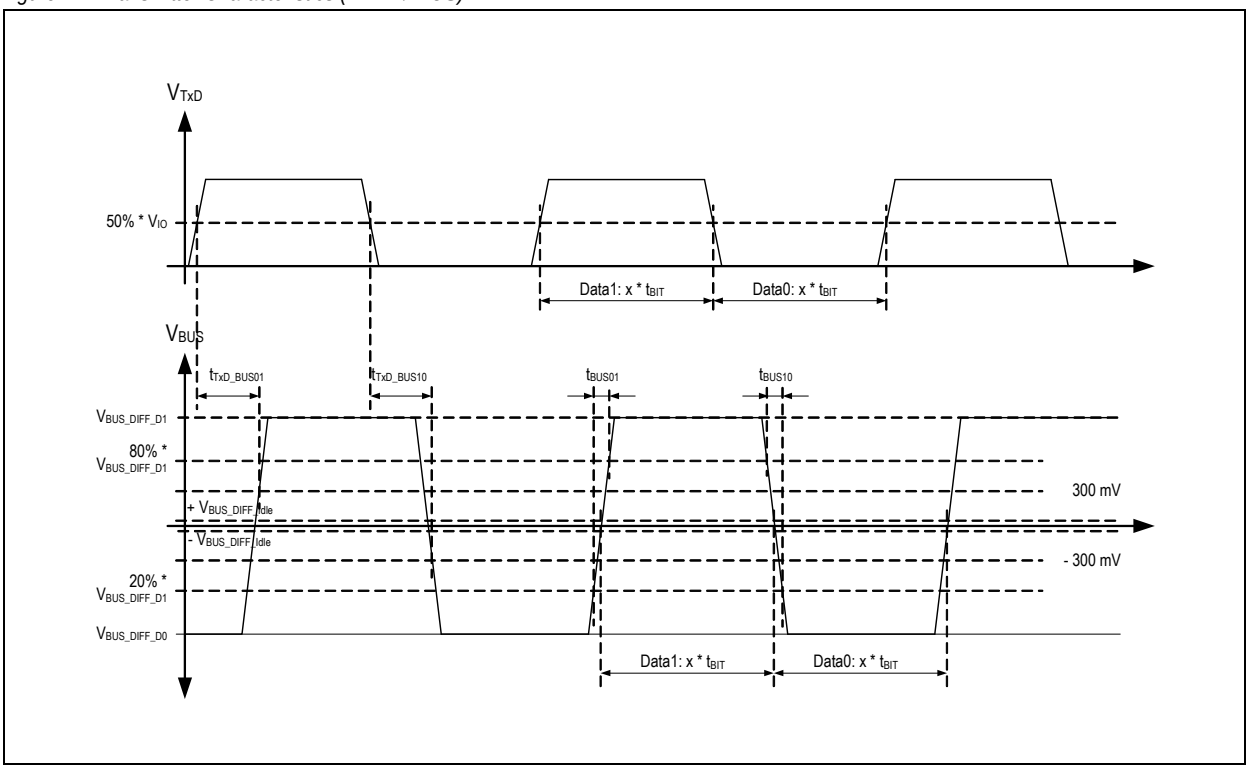


Figure 13. Transmitter Characteristics (TxEN → BUS)

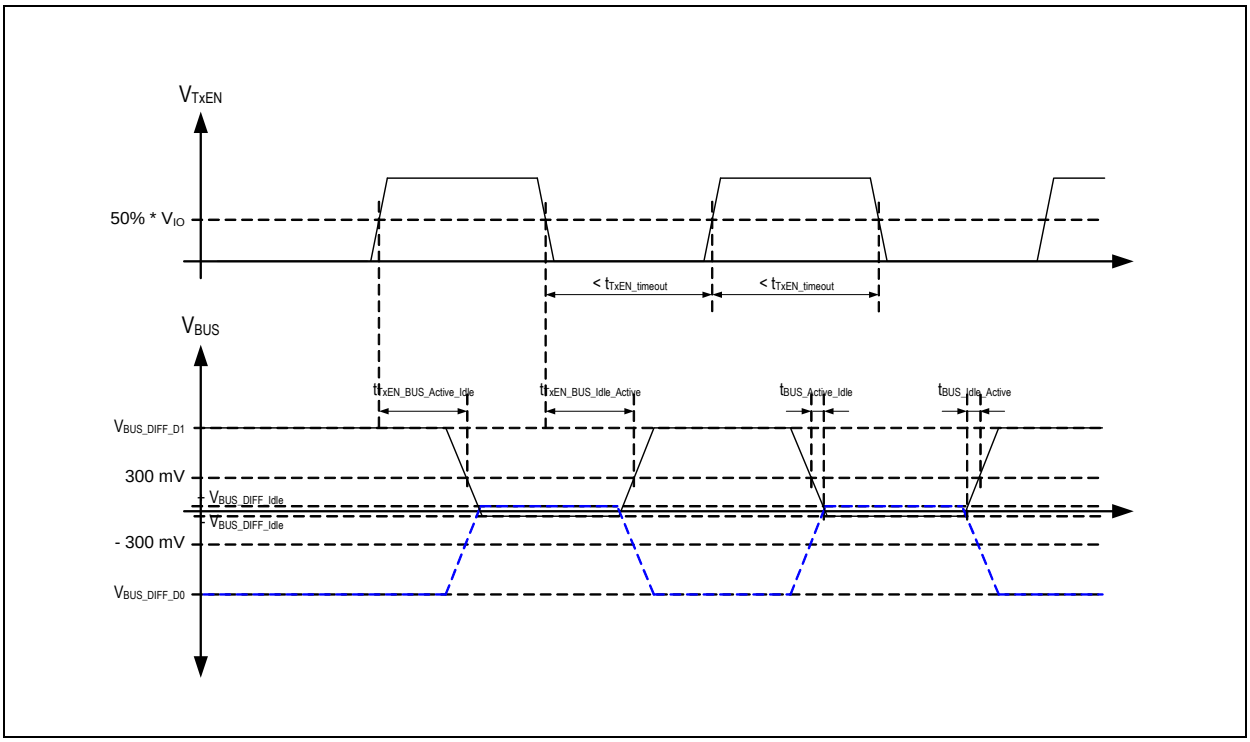
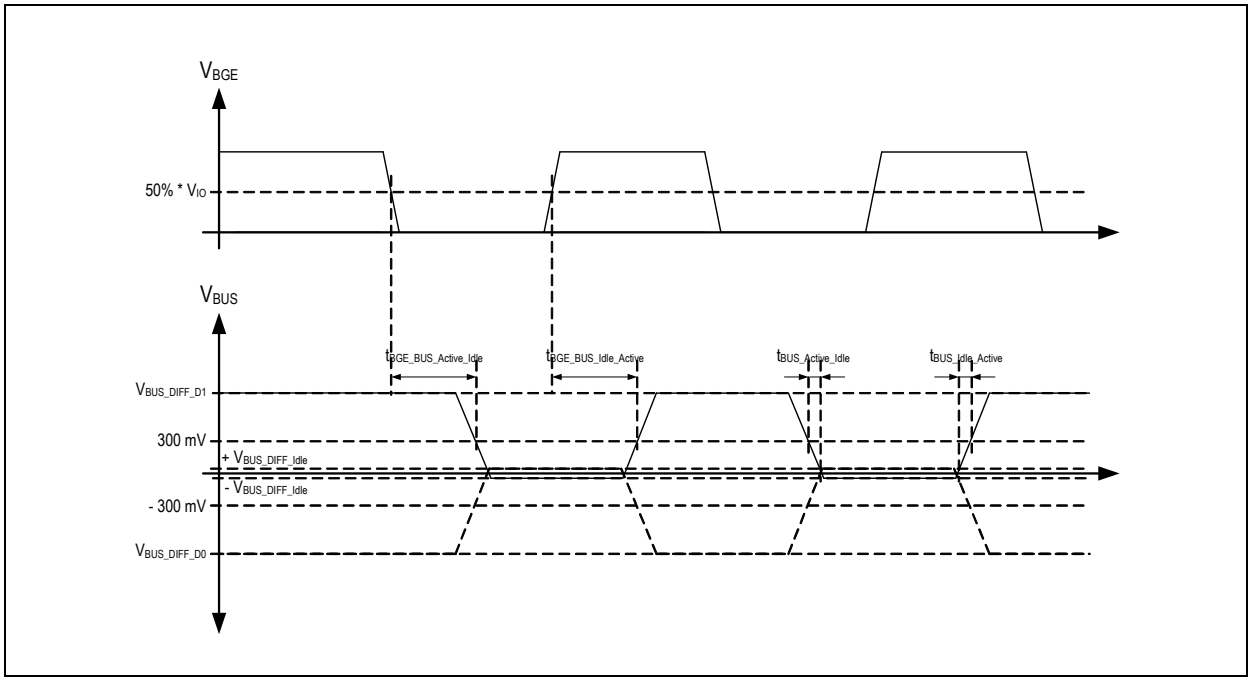


Figure 14. Timing Characteristics (BGE → BUS)

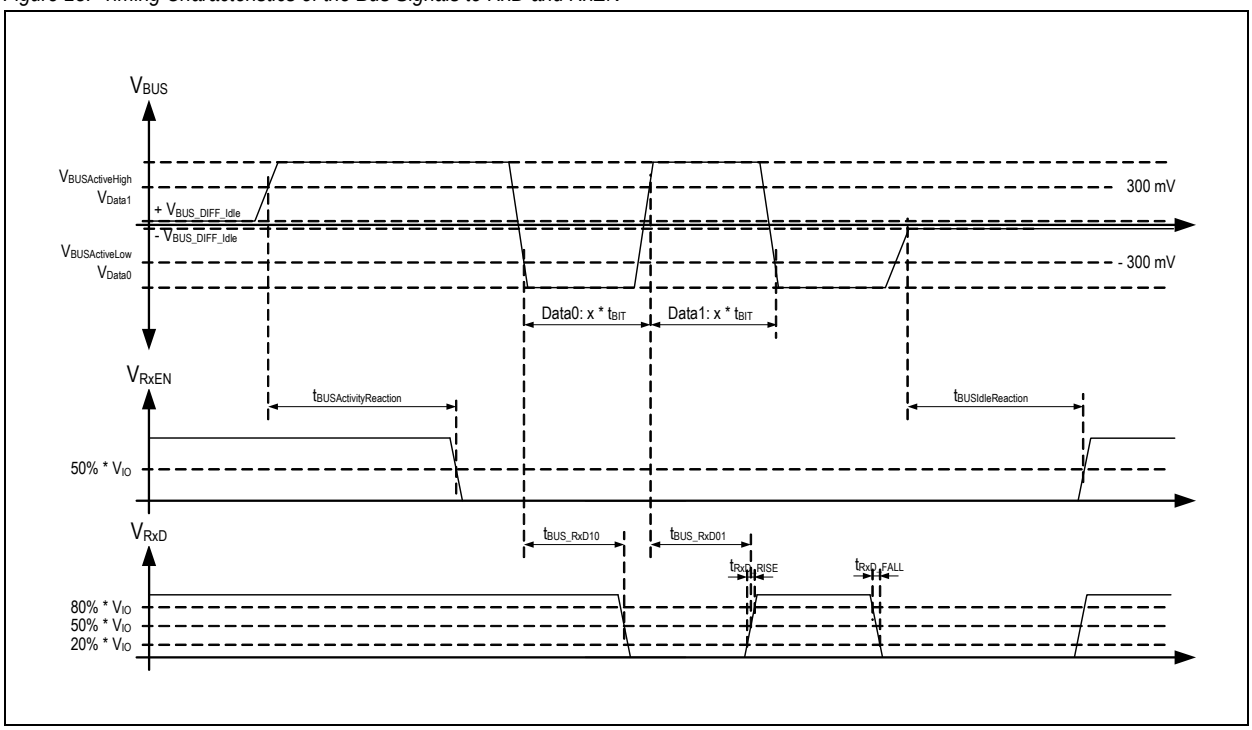


In NORMAL and RECEIVE-ONLY mode, the transmitter drives on the bus Idle in case no data are transmitted. In STANDBY, GO-TO-SLEEP and SLEEP mode the transmitter drives Idle_LP on the bus pins. In POWER-OFF mode the bus pins shows Idle_HZ.

9.10 Receiver

The Receiver generates from the FlexRay differential bus voltage a digital signal on the RxD and RxEN pins. RxD shows the data (Data0 and Data1) and RxEN shows the bus idle and activity status received on the bus pins. The Receiver is only active in NORMAL and RECEIVE-ONLY mode.

Figure 15. Timing Characteristics of the Bus Signals to RxD and RxEN



9.10.1 Bus Activity and Idle Detection (only in NORMAL and RECEIVE-ONLY mode)

If the absolute differential bus voltage is higher than $V_{BUSActiveLow}$ and less than $V_{BUSActiveHigh}$ for a time longer than $t_{BUSIdleDetection}$, bus Idle is detected, RxEN and RxD are switched to logical high after a time $t_{BUSIdleReaction}$.

If the absolute differential bus voltage is higher than $V_{BUSActiveHigh}$ or lower than $V_{BUSActiveLow}$ for a time loner than $t_{BUSActivitiyDetection}$, bus Activity is detected, RxEN is switched to logical low and RxD shows the detected bus data according to Table 11 after the time $t_{BUSActivityReaction}$.

Table 11. Logic Table for Receiver Bus Signal Detection

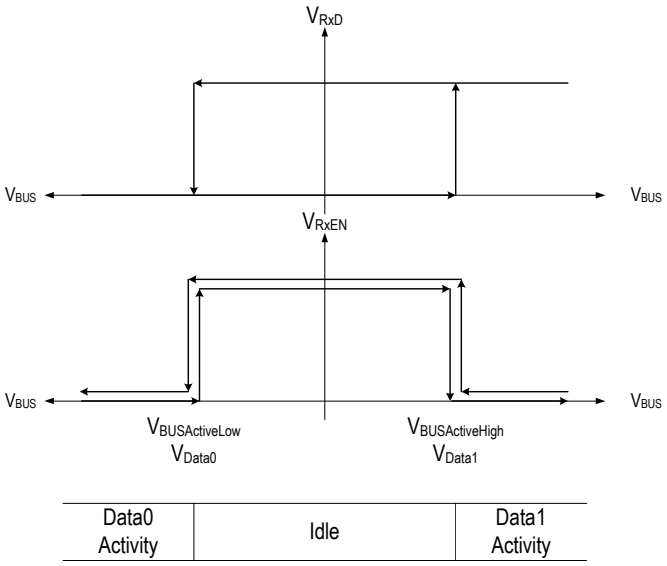
Receiver Operation Mode	Bus Signals	RxEN	RxD
Normal power modes (NORMAL and RECEIVE-ONLY mode)	Idle	H	H
	Data0	L	L
	Data1	L	H

9.10.2 Bus Data Detection (only in NORMAL and RECEIVE-ONLY mode)

If, after activity detection the differential bus voltage is higher than V_{Data1}, RxD will be high after a time t_{BUS_RxD01}.

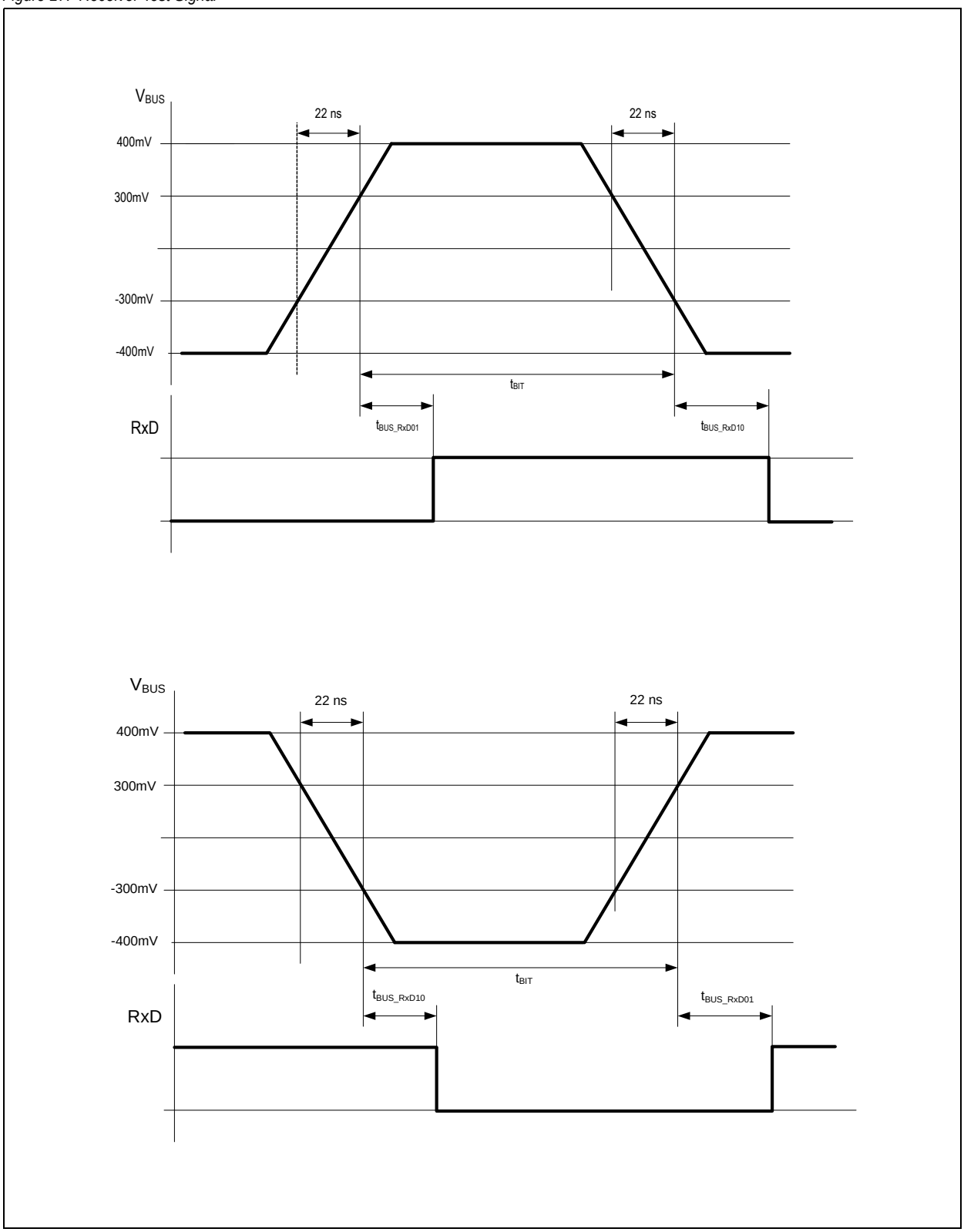
If, after activity detection the differential bus voltage is lower than V_{Data0}, RxD will be low after a time t_{BUS_RxD10}.

Figure 16. Receiver Characteristics (BUS → RxD, RxEN)



9.10.3 Receiver Test Signal

Figure 17. Receiver Test Signal



9.11 Test Circuits

Figure 18. Test Circuit for Automotive Transients

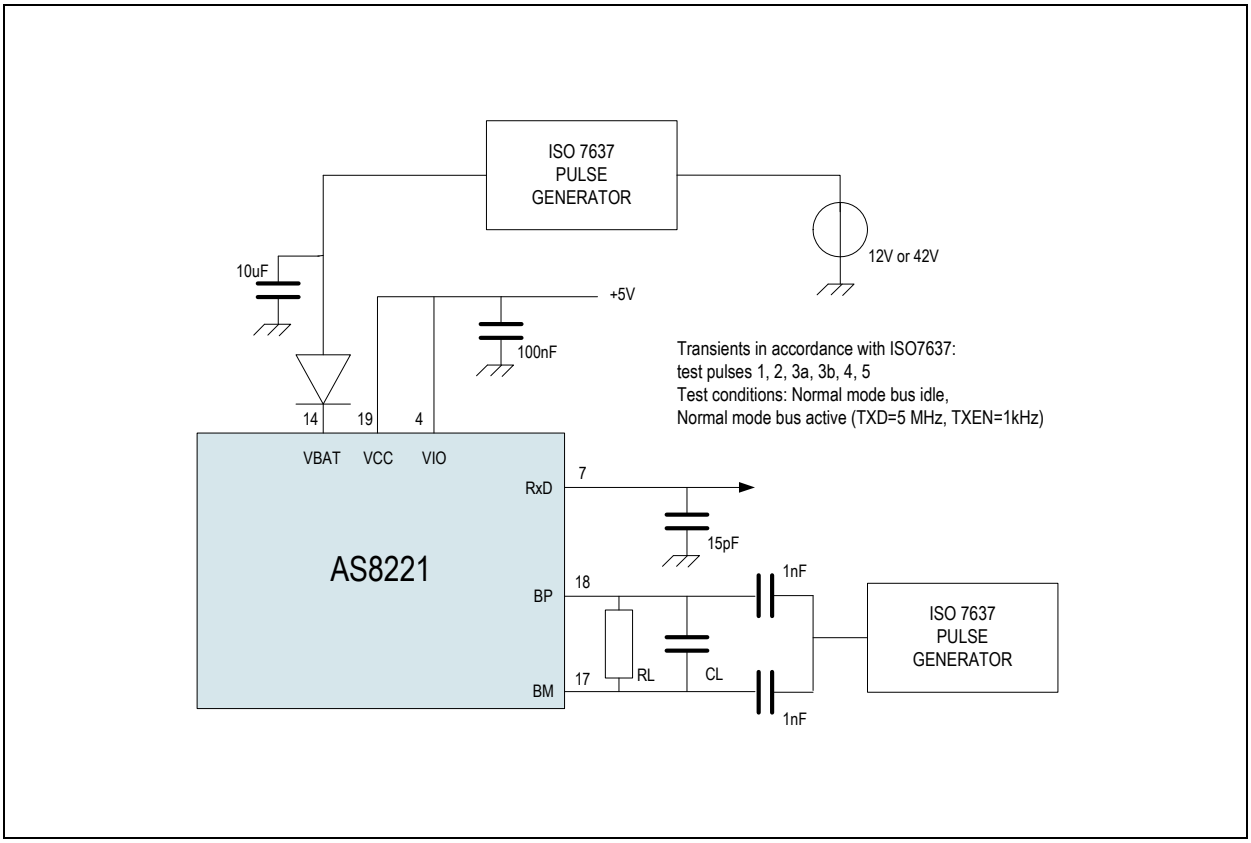
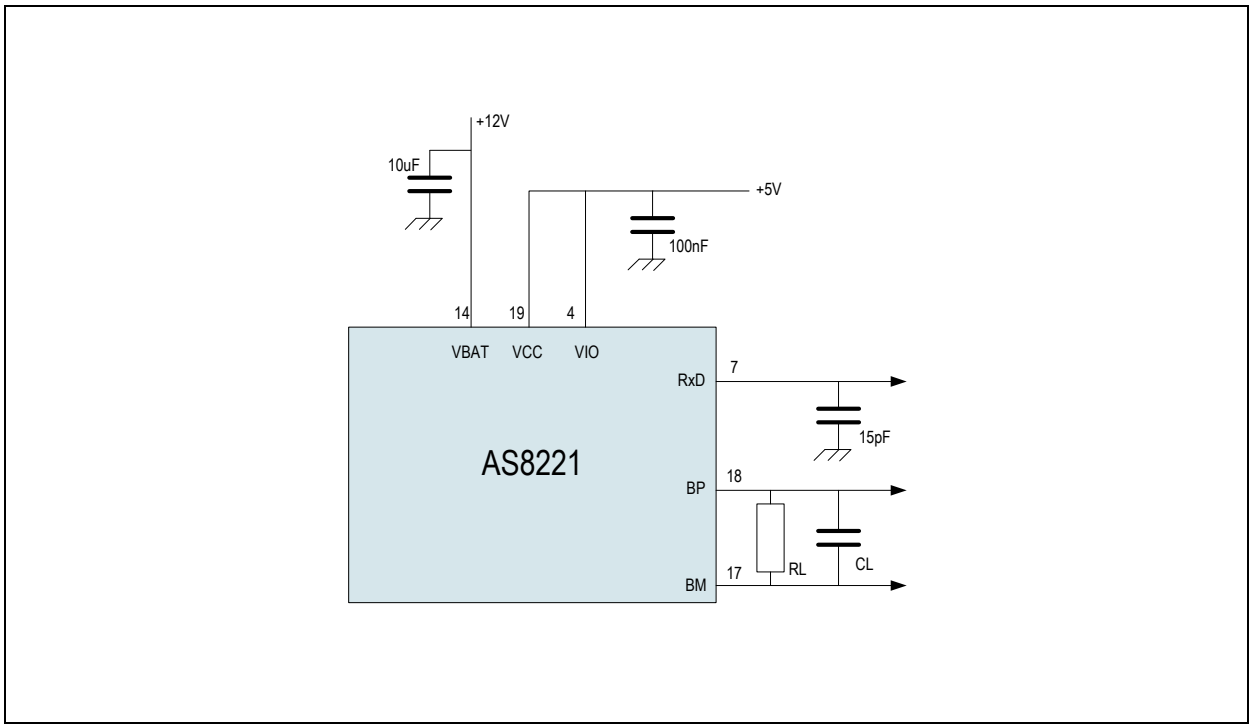
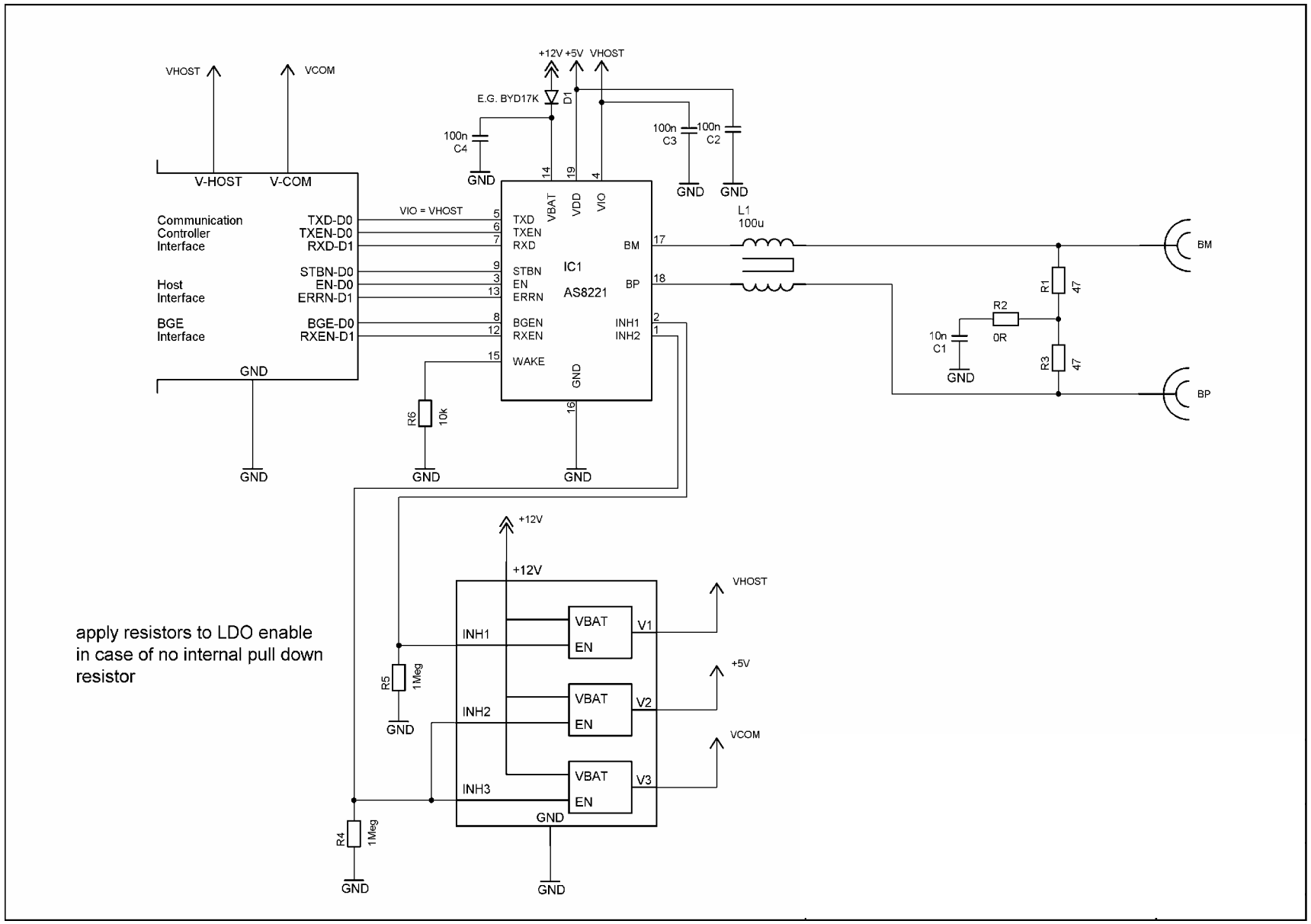


Figure 19. Test Circuit for Dynamic Characteristics



9.12 Application Circuits

Figure 20. AS8221 Application Schematic



10 Appendix

10.1 FlexRay Functional Classes

The AS8221 FlexRay Standard Transceiver has the following Bus Driver functional classes according the FlexRay Electrical Physical Layer Specification V2.1 Rev. B implemented:

- Functional Class: Chapter 8.13.1 “Bus Driver voltage regulator control”
- Functional Class: Chapter 8.13.2 “Bus Driver - Bus Guardian interface”
- Functional Class: Chapter 8.13.4 “Bus Driver logic level adaptation”

10.2 FlexRay Parameter Comparison

The following table shows the comparison of conventions used in AS8221 datasheet and FlexRay Electrical Physical Layer Specification V2.1 Rev. B.

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
Absolute Maximum Ratings			
-	Battery Supply Voltage (V_{BAT})	-	-
-	Supply Voltage (V_{CC})	-	-
-	Supply Voltage (V_{IO})	-	-
-	DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN	-	-
-	DC Voltage on pin WAKE, INH1, INH2	-	-
-	DC Voltage at BP and BM	-	-
-	Input current (latchup immunity)	-	-
-	Electrostatic discharge at bus lines BP, BM, V_{BAT}, WAKE	uESDExt	ESD protection on pins that lead to ECU external terminals
-	Electrostatic discharge	uESDint	ESD on all other pins
-	Transient voltage on BP, BM	-	-
-	Transient voltage on V_{BAT}	-	-
-	Total power dissipation (all supplies and outputs)	-	-
-	Storage temperature	-	-
-	Junction temperature	-	-
-	Package body temperature	-	-
-	Humidity non-condensing	-	-
Supply Voltage			
T_{AMB}	Ambient temperature	T	Ambient temperature
V_{CC} - V_{IO}	Difference of supplies	-	-
I_{BAT}	V_{BAT} current consumption	-	-
I_{CC}	V_{CC} current consumption	-	-

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
I_{IO}	V_{IO} current consumption	-	-
State Transitions			
t_{STBN_RxD}	Delay STBN high to RxD high with wake flag set	-	-
t_{STBN_RxEN}	Delay STBN high to RxEN high with wake flag set	-	-
t_{SLEEP_INH1}	Delay STBN high to INH1 high	-	-
$t_{STANDBY\_INH2}$	Delay STBN high to INH2 high	-	-
t_{SLEEP}	GO-TO-SLEEP hold time	-	-
Transmitter			
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in NORMAL mode (Data0)	$uBDTx_{active}$	Absolute value of uBus while sending
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in NORMAL mode (Data1)	$uBDTx_{active}$	Absolute value of uBus while sending
V_{BUS_DIFF}	Matching between Data0 and Data1 differential bus voltage in NORMAL mode	-	-
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data0 in non-low-power modes	-	-
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data1 in non-low-power modes	-	-
ΔV_{BUS_COM}	Matching between Data0 and Data1 common mode voltage	-	-
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in idle mode	uBDTxidle	Absolute value of uBus, while Idle
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute maximum current when BP is shorted to BM	$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM
$IBP_{GNDShortMax}$	Absolute maximum current when BP is shorted to GND	$IBP_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBM_{GNDShortMax}$	Absolute maximum current when BM is shorted to GND	$IBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND
$IBP_{-5VShortMax}$	Absolute maximum current when BP is shorted to -5V	$IBP_{-5VShortMax}$	Absolute maximum output current when shorted to -5V
$IBM_{-5VShortMax}$	Absolute maximum current when BM is shorted to -5V	$IBM_{-5VShortMax}$	Absolute maximum output current when shorted to -5V
$IBP_{27VShortMax}$	Absolute maximum current when BP is shorted to 27V	$IBP_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V
$IBM_{27VShortMax}$	Absolute maximum current when BM is shorted to 27V	$IBM_{BAT27VShortMax}$	Absolute maximum output current when shorted to 27V

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
$IBP_{48VShortMax}$	Absolute maximum current when BP is shorted to 48V	$IBP_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
$IBM_{48VShortMax}$	Absolute maximum current when BM is shorted to 48V	$IBM_{BAT48VShortMax}$	Absolute maximum output current when shorted to 48V
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	dBDTx10	Transmitter delay, negative edge
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	dBDTx01	Transmitter delay, positive edge
$t_{TxD\_MISMATCH}$	Delay time from TxD to BUS mismatch	dTxAsym	Transmitter delay mismatch | dBDTx10 - dBDTx01 |
t_{BUS10}	Fall time differential bus voltage	dBusTx10	Fall time differential bus voltage (80% ® 20%)
t_{BUS01}	Rise time differential bus voltage	dBusTx01	Rise time differential bus voltage (20% ® 80%)
$t_{TxEN\_BUS\_Idle\_Active}$	Delay time from TxEN to bus active	dBDTxia	Propagation delay idle ®active
$t_{TxEN\_BUS\_Active\_Idle}$	Delay time from TxEN to bus idle	dBDTxai	Propagation delay active ® idle
$t_{TxEN\_MISMATCH}$	Delay time from TxEN to bus mismatch	dBDTxDM	| dBDTxia - dBDTxai |
$t_{BGE\_BUS\_Idle\_Active}$	Delay time from BGE to bus active	dBDTxia	Propagation delay idle ® active
$t_{BGE\_BUS\_Active\_Idle}$	Delay time from BGE to bus idle	dBDTXai	Propagation delay active ® idle
$t_{BUS\_Idle\_Active}$	Differential bus voltage transition time: idle to active	dBusTxia	Transition time idle ® active
$t_{BUS\_Active\_Idle}$	Differential bus voltage transition time: active to idle	dBusTxai	Transition time active → idle
$t_{TxEN\_timeout}$	TxEN timeout	-	-
Receiver			
R_{BP}, R_{BM}	BP, BM input resistance	RCM1, RCM2	Receiver common mode input resistance
R_{DIFF}	BP, BM differential input resistance	-	-
V_{BPidle}, V_{BMidle}	Idle voltage in non-low-power modes on pin BP,BM	uBias	Bus bias voltage during BD_Normal mode
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in low-power modes on pin BP, BM	uBias	Bus bias voltage during low-power modes
I_{BPidle}	Absolute idle output current on pin BP	-	-
I_{BMidle}	Absolute idle output current on pin BM	-	-
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	iBPLeak, iBMLeak	Absolute leakage current, when not powered

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	uBusActiveHigh	Upper Receiver threshold for detecting activity
$V_{BUSActiveLow}$	Activity detection differential input voltage low	uBusActiveLow	Lower Receiver threshold for detecting activity
V_{Data1}	Data1 detection differential input voltage	uData1	Receiver threshold for detecting Data_1
V_{Data0}	Data0 detection differential input voltage	uData0	Receiver threshold for detecting Data_0
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	uData	Mismatch of Receiver thresholds
$V_{RECEIVE\_COM}$	Maximum common mode voltage range when receiving	uCM	Common mode voltage range (with respect to GND) that does not disturb the receive function
t_{BUS_RxD10}	Delay from bus to RxD negative edge	dBDRx10	Receiver delay, negative edge
t_{BUS_RxD01}	Delay from bus to RxD positive edge	dBDRx01	Receiver delay, positive edge
t_{BIT}	Bit time	-	-
t_{RxD_ASYM}	Delay time from bus to RxD mismatch	dRxAsym	Receiver delay mismatch | dBDRx10 – dBDRx01 |
t_{RxD_FALL}	Fall time RxD voltage	dRxSlope	Fall and rise time 20%-80%
t_{RxD_RISE}	Rise time RxD voltage	dRxSlope	Fall and rise time 20%-80%
$t_{BUSIdleDetection}$	Idle detection time	dIdleDetection	Filter-time for idle detection
$t_{BUSActivityDetection}$	Activity detection time	dActivityDetection	Filter-time for activity detection
$t_{BUSIdleReaction}$	Idle reaction time	dBDRxai	Idle reaction time
$t_{BUSActivityReaction}$	Activity reaction time	dBDRxia	Activity reaction time
Wake-Up Detector			
t_{BWU_D0}	Data0 detection time in remote wake-up pattern	dWU0Detect	Acceptance timeout for detection of a Data_0 phase in wake-up pattern
t_{BWU_Idle}	Idle or Data1 detection time in remote wake-up pattern	dWUIdleDetect	Acceptance timeout for detection of a Idle phase in wake-up pattern
t_{BWU_Detect}	Total remote wake-up detection time	dWUTimeout	Acceptance timeout for wake-up pattern recognition
V_{BWUTH}	Bus wake-up detection threshold	-	-
V_{LWUTH}	Local wake-up detection threshold	-	-

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
I_{LWUL}	Low level input current on local WAKE pin	-	-
I_{LWUH}	High level input current on local WAKE pin	-	-
$t_{LWUFilter}$	Local wake filter time	dWakePulseFilter	Wake pulse filter time (spike rejection)
-	V_{BAT} operating range V_{BAT} = +6.5 to + 50V	V_{BAT} for WU detector	Battery voltage required for wake-up detector operation
Supply Voltage Monitor			
V_{BATTHH}	V_{BAT} undervoltage recovery threshold	-	-
V_{BATTHL}	V_{BAT} undervoltage detection threshold	uUVBAT	Undervoltage detection threshold
V_{CCTHH}	V_{CC} undervoltage recovery threshold	-	-
V_{CCTHL}	V_{CC} undervoltage detection threshold	uUVCC	Undervoltage detection threshold
V_{IOTHH}	V_{IO} undervoltage recovery threshold	-	-
V_{IOTHL}	V_{IO} undervoltage detection threshold	uUVIO	Undervoltage detection threshold
t_{UV_DETECT}	Detection time for undervoltage at V_{BAT}, V_{CC}, V_{IO}	dUVBAT, dUVCC, dUVIO	Undervoltage reaction time
t_{UV_REC}	Detection time for undervoltage recovery at V_{BAT}, V_{CC}, V_{IO}	-	-
Bus Error Detection			
I_{THL}	Absolute bus current for low current detection	-	-
I_{THH}	Absolute bus current for high current detection	-	-
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	-	-
t_{BUS_ERROR}	Bus error detection time	-	Detection only required while actively transmitting a data frame, error indication to host latest when transmission stops.
Over Temperature			
OT_{TH}	Over temperature threshold	-	-
OT_{TL}	Over temperature hysteresis	-	-

Table 12. Comparison Table

AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
Power Supply Interface			
ΔV_{OINH}	High level voltage drop on INH1, INH2	-	-
$\lvert I_{IL} \rvert$	Leakage current	-	-
Communication Controller Interface			
V_{TxDIH}	Threshold for detecting TxD as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{TxDIL}	Threshold for detecting TxD as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxDIH}	TxD high level input current	-	-
I_{TxDIL}	TxD low level input current	-	-
V_{TxENIH}	Threshold for detecting TxEN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{TXENIL}	Threshold for detecting TxEN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{TxENIH}	TxEN high level input current	-	-
I_{TxENIL}	TxEN low level input current	-	-
V_{RxDOH}	RxD high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{RxDOL}	RxD low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Host Interface			
V_{STBNIH}	Threshold for detecting STBN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{STBNIL}	Threshold for detecting STBN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{STBNIH}	STBN high level input current	-	-
I_{STBNIL}	STBN low level input current	-	-
$t_{STBN\_DEB\_LP}$	STBN de-bouncing time low-power modes	-	-
$t_{STBN\_DEB\_NLP}$	STBN de-bouncing time non-low-power modes	-	-
V_{ENIH}	Threshold for detecting EN as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high

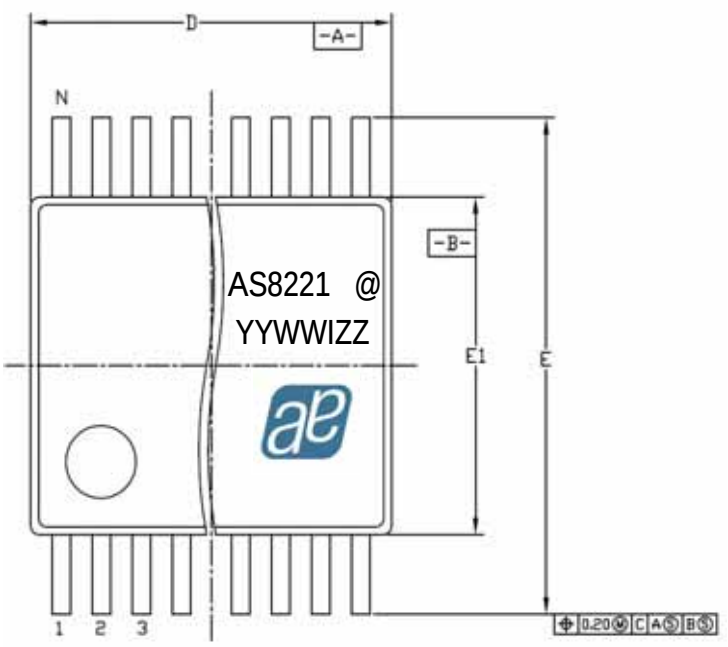
Table 12. Comparison Table

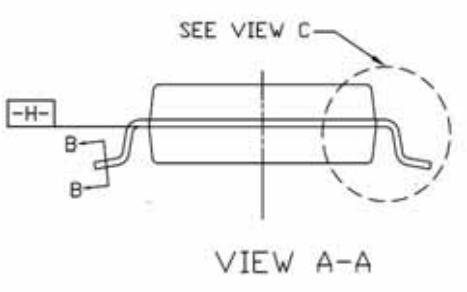
AS8221 Datasheet		FlexRay Electrical Physical Layer Specification V2.1 Rev. B	
Symbol	Parameter	Name	Description
V_{ENIL}	Threshold for detecting EN as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{ENIH}	EN high level input current	-	-
I_{ENIL}	EN low level input current	-	-
$t_{EN\_DEB\_LP}$	EN de-bouncing time low-power modes	-	-
$t_{EN\_DEB\_NLP}$	EN de-bouncing time non-low-power modes	-	-
V_{ERRNOH}	ERRN high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{ERRNOL}	ERRN low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Bus Guardian Interface			
V_{BGEIH}	Threshold for detecting BGE as on logical high	uVIO-IN-HIGH	Threshold for detecting a digital input as on logical high
V_{BGEIL}	Threshold for detecting BGE as on logical low	uVIO-IN-LOW	Threshold for detecting a digital input as on logical low
I_{BGEIH}	BGE high level input current	-	-
I_{BGEIL}	BGE low level input current	-	-
V_{RXENOH}	RxEN high level output voltage	uVIO-OUT-HIGH	Output voltage on a digital output, when in logical high state
V_{RXENOL}	RxEN low level output voltage	uVIO-OUT-LOW	Output voltage on a digital output, when in logical low state
Read Out Interface			
$t_{RO\_EN\_ERRN}$	Propagation delay falling edge EN to ERRN	-	-
$t_{RO\_EN\_TIMEOUT}$	Error-read-out timeout	-	-

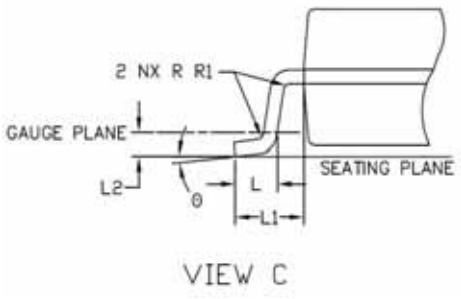
11 Package Drawings and Markings

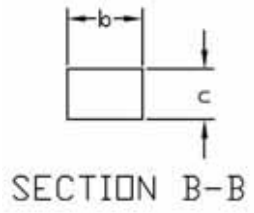
The device is available in a SSOP20 Package.

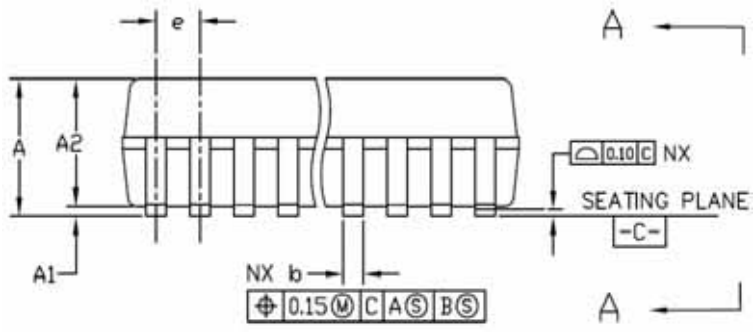
Figure 21. Package Drawings and Dimensions











Symbol	Min	Nom	Max
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N		20	

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.

Marking Information:

YY	WW	I	ZZ	@
Last two digits of the current year	Manufacturing Week	Assembly plant identifier	Assembly traceability code	Sublot identifier

Revision History

Revision	Date	Owner	Description
1.0	Sep 01, 2009	hgl	First version
1.1	Sep 14, 2009		Made sentence corrections and converted the 'Typ' values of Table 3 in to standard format. No Technical Changes to the datasheet.
1.2	May 13, 2010		Updated the ERRN Signalling Table 8. (no functional change)
			Updated Ordering Information Table 13.
			Added Package Drawings and Markings – refer to page 39.
1.3	July 16, 2010		Updated Ordering Information Table 13.
1.4	Oct 30, 2010		Updated the following: VBAT minimum voltage requirement in Electrical Characteristics, Error Flags, Error and Status Flag Bit Order.
	Nov 18, 2010		Updated Absolute Maximum Ratings on page 6, Package Drawings and Markings on page 39.
	Dec 15, 2010		Updated package body temperature under Absolute Maximum Ratings.
1.5	Feb 24, 2011		Figure 12, Figure 13, Figure 14, Figure 15, Figure 16 updated. Added Application Circuits.
1.6	Dec 19, 2011		Updated ESD parameter in Absolute Maximum Ratings on page 6.
1.7	Feb 16, 2012		Updated Package Drawings and Markings section.

Note: Typos may not be explicitly mentioned under revision history.

12 Ordering Information

The devices are available as the standard products shown in Table 13.

Table 13. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS8221-ASSP	AS8221	AS8221 FlexRay Standard Transceiver	Tape & Reel in DryPack	SSOP20

Note: All products are RoHS compliant and austriamicrosystems green.
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