APT5010FN 500V 50A 0.10 Ω
APT4510FN 450V 50A 0.10 Ω

POWER MOS IV™

N - CHANNEL ENHANCEMENT MODE HIGH VOLTAGE POWER MOSFETS

MAXIMUM RATINGS

All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT4510FN	APT5010FN	UNIT
V_{DSS}	Drain-Source Voltage	450	500	Volts
I_D	Continuous Drain Current	50		Amps
I_{DM}	Pulsed Drain Current [1]	200		Amps
V_{GS}	Gate-Source Voltage	±30		Volts
P_D	Total Power Dissipation @ T_C = 25°C, Derate Above 25°C	595		Watts
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150		°C

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions		MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250uA)	APT5010FN	500			Volts
		APT4510FN	450			Volts
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = V_{DSS}, V_{GS} = 0V)				250	µA
	(V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125°C)				1000	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)				±100	nA
$I_D(ON)$	On State Drain Current [2] (V_{DS} > $I_D(ON)$ x $R_{DS}(ON)$ Max, V_{GS} = 10V)		50			Amps
$V_{GS}(TH)$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1mA)		2		4	Volts
$R_{DS}(ON)$	Static Drain-Source On-State Resistance [2] (V_{GS} = 10V, I_D = 0.5 I_D(Cont.))				0.10	Ohms

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.21	°C/W
$R_{\theta JA}$	Junction to Ambient			20	°C/W
T_L	Maximum Lead Temp. for Soldering Conditions: 0.063" from Case for 10 Sec.			300	°C

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T-39-15

DYNAMIC CHARACTERISTICS

APT5010/4510FN

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 10V	4500		6300	pF
C_{oss}	Output Capacitance	V_{DS} = 25V	960		1450	pF
C_{rss}	Reverse Transfer Capacitance	f = 1MHz	400		600	pF
Q_g	Total Gate Charge [3]	V_{GS} = 10V, I_D = I_D(Cont.)	160		260	nC
Q_{gs}	Gate-Source Charge	V_{DD} = 0.5 V_{DSS}	25		40	nC
Q_{gd}	Gate-Drain ("Miller") Charge		130		160	nC
t_d(on)	Turn-on Delay Time	V_{DD} = 0.5 V_{DSS}			30	nS
t_r	Rise Time	V_{GS} = 15V, I_D = I_D(Cont.)			60	nS
t_d(off)	Turn-off Delay Time	R_G = 1.8Ω			120	nS
t_f	Fall Time				70	nS

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			50	Amps
I_{SM}	Pulsed Source Current [1] (Body Diode)			200	Amps
V_{SD}	Diode Forward Voltage [2] (V_{GS} = 0V, I_S = -I_D(Cont.)			1.0	Volts
t_{rr}	Reverse Recovery Time (I_S = -I_D(Cont.) , dI_S/dt = 100A/μs)			600	nS
Q_{rr}	Reverse Recovery Charge			15	μC

SAFE OPERATING AREA CHARACTERISTICS

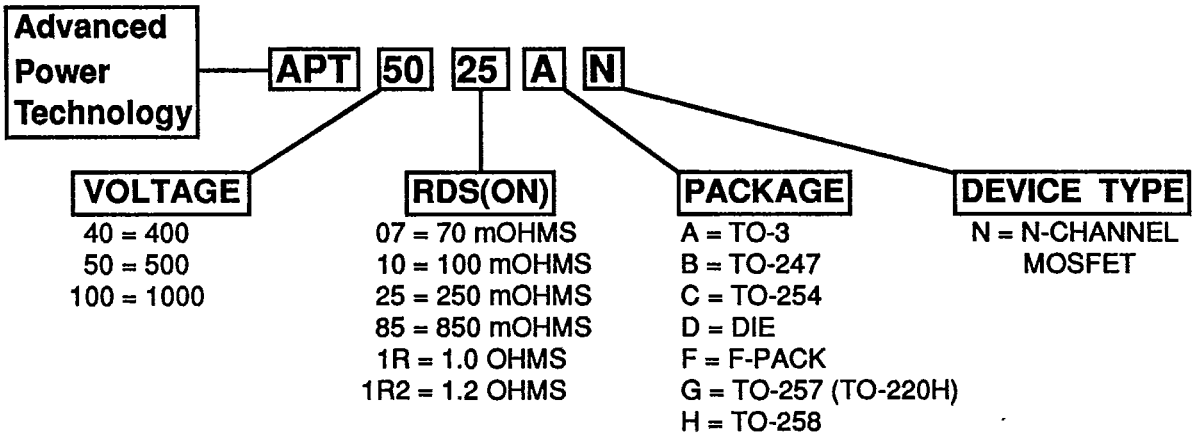
Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
SOA1	Safe Operating Area	V_{DS} = 0.4 V_{DSS} , I_{DS} = P_D / 0.4 V_{DSS} , t = 1 Sec.	595			Watts
SOA2	Safe Operating Area	V_{DS} = P_D / I_D(Cont.) , I_{DS} = I_D(Cont.) , t = 1 Sec.	595			Watts
I_{LM}	Inductive Current Clamped		200			Amps

1.) Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Fig.1)

2.) Pulse Test: Pulse Width < 380 μS Duty Cycle < 2%

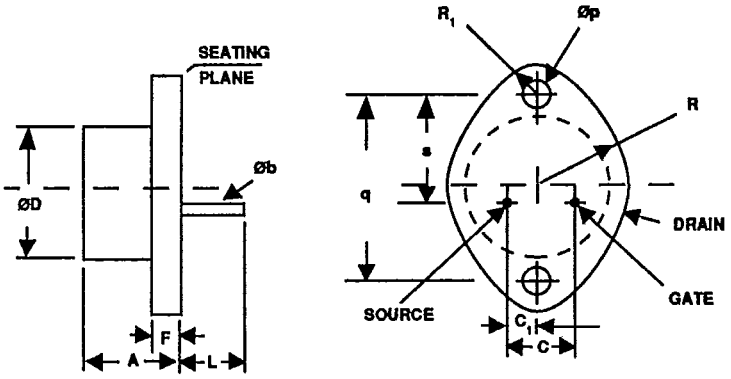
3.) See JEDEC MIL-STD-750C Method 3471

APT PART NUMBERING SYSTEM - EXAMPLES



PACKAGE OUTLINES

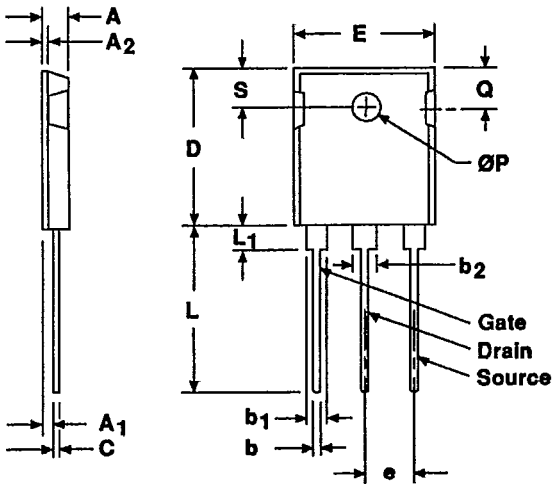
Package A TO-3 (TO-204AA)



SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.250	.360	6.35	9.15	
Øb	.038	.043	.97	1.10	2
ØD		.875		22.23	
C	.420	.440	10.67	11.18	
C_1	.205	.225	5.21	5.72	
F	.060	.135	1.52	3.43	
L	.312	.500	7.92	12.70	2
Øp	.151	.161	3.84	4.09	
q	1.177	1.197	29.90	30.40	
R	.495	.525	12.57	13.34	
R_1	.131	.188	3.33	4.78	
s	.655	.675	16.64	17.15	1

Notes:
1. These dimensions should be measured at points .050" (1.27 mm) to.55" (1.40 mm) below seating plane. When gate is not used, measurement will be made at seating plane.
2. Two leads.

Package B TO-3P (TO-247 Type AD Proposed)

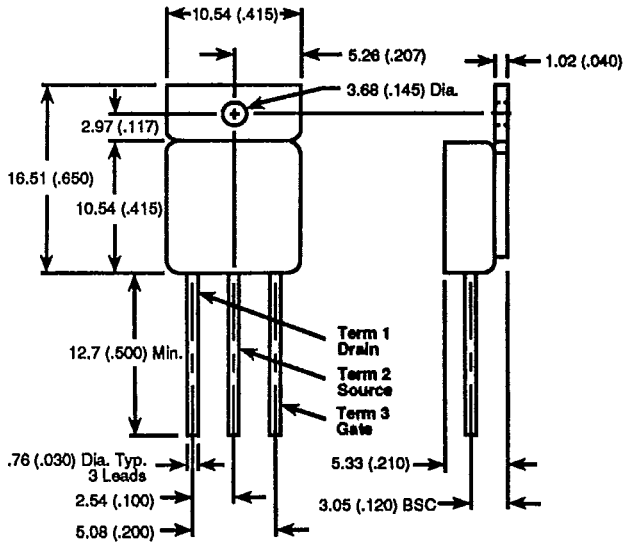


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	.185	.209	4.69	5.31	
A_1	.087	.102	2.21	2.59	
A_2	.059	.098	1.49	2.49	
b	.040	.055	1.01	1.40	4
b_1	.065	.084	1.65	2.13	4
b_2	.113	.123	2.87	3.12	4
C	.016	.031	0.40	0.79	
D	.819	.845	20.80	21.46	
E	.610	.640	15.49	16.26	
e	.215 BSC		5.25 BSC		
L	.780	.800	19.81	20.32	
L_1		.177		4.50	4
ØP	.140	.144	3.55	3.66	
Q	.212	.244	5.38	6.20	
S	.242 BSC		6.15 BSC		

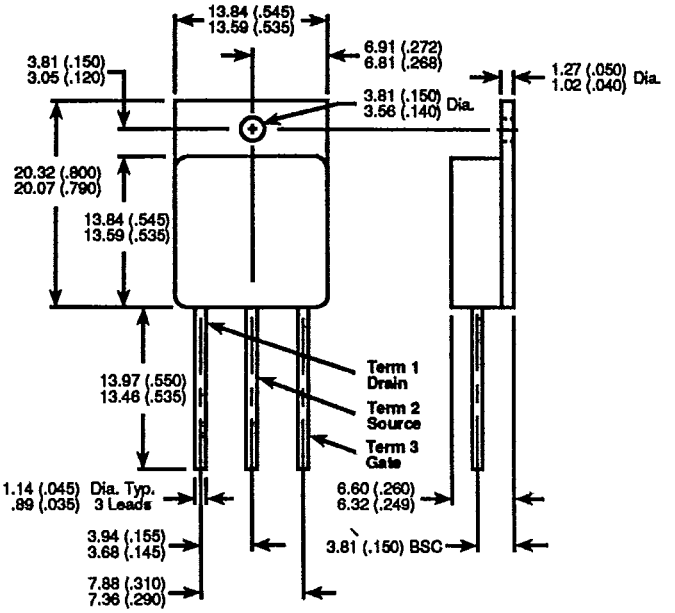
Notes:
1. Refer to applicable symbol list.
2. Dimensions and tolerances per ANSI V14.5, 1982.
3. Maximum radius of .050 on all boot edges and corners.
4. Lead dimensions uncontrolled in L
5. Controlling dimension: Metric.

PACKAGE OUTLINES (Continued)

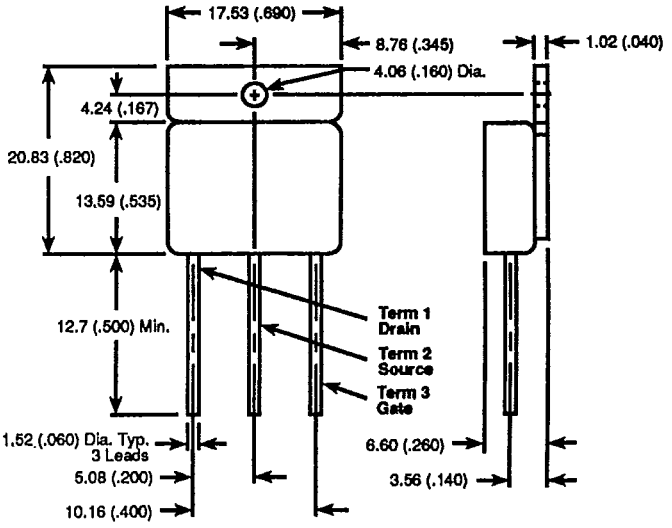
Package G TO-257AA (TO-220 Herm.)



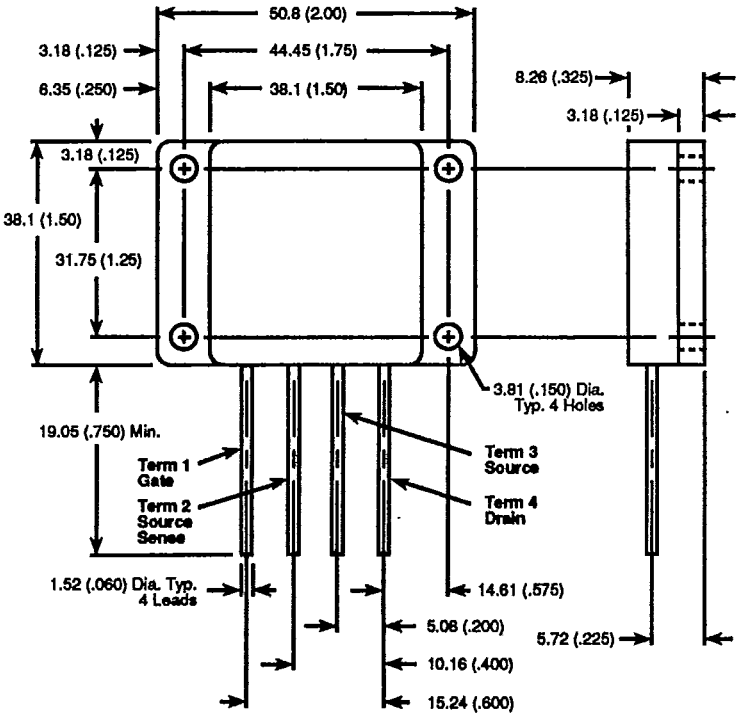
Package C TO-254AA



Package H TO-258AA (TO-247 Herm.)



Package F (F-Pack)

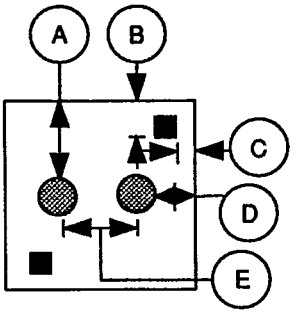


DIE TOPOGRAPHICAL LAYOUT DETAILS FOR APT POWER MOS IV™ DIE

APT - 104 = .199 x .203 In.

Source Pads = .036 In. diam

Gate pads = .018 x .019 In.



Letters = Internal dimensions

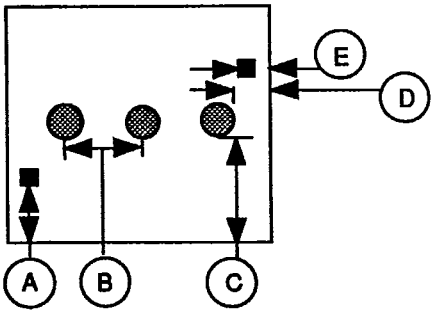
A = .081 In. B = .039 In. C = .018 In.

D = .040 In. E = .082 In.

APT - 105 = .290 x .250 In.

Source Pads = .036 In. diam

Gate pads = .018 x .019 In.



Letters = Internal dimensions

A = .055 In. B = .085 In. C = .105 In.

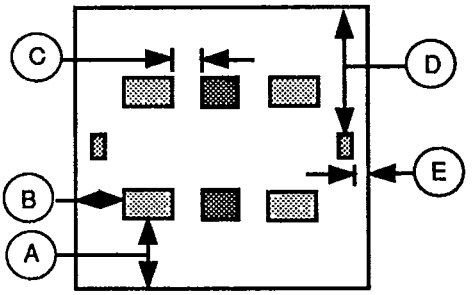
D = .042 In. E = .018 In.

APT - 101 = .320 x .320 In.

Source Pads = .037 x .024 In.

Source Pads = .030 x .024 In.

Gate pads = .014 x .019 In.



Letters = Internal dimensions

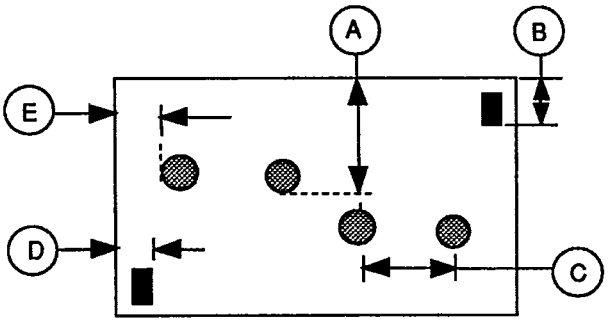
A = .077 In. B = .062 In. C = .048 In.

D = .149 In. E = .018 In.

APT - 102 = .414 x .254 In.

Source Pads = .036 In. diam

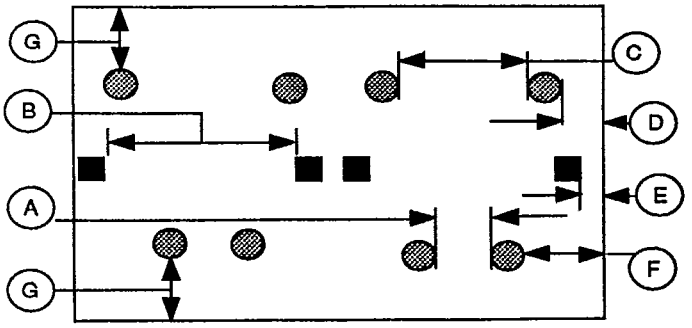
Gate pads = .012 x .019 In.



Letters = Internal dimensions

A = .117 In. B = .037 In. C = .097 In.

D = .031 In. E = .046 In.



APT - 107 = .588 x .388 In.

Source pads = .036

Gate pads = .017 x .018

Letters = Internal dimensions

A = .057 In. B = .240 In. C = .151 In.

D = .045 In. E = .017 In. F = .091 In. G = .088 In.