Am93469

512 x 9 TTL Tag Buffer

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast address to comparator output (MISS)
- Replaces six or more integrated circuits with a single device
- On-chip parity generator and checker
- Easy horizontal and vertical expansion
- Fully TTL compatible
- Integrated reset feature
- 24-pin ceramic DIP (300 Mil) and Flatpak packages

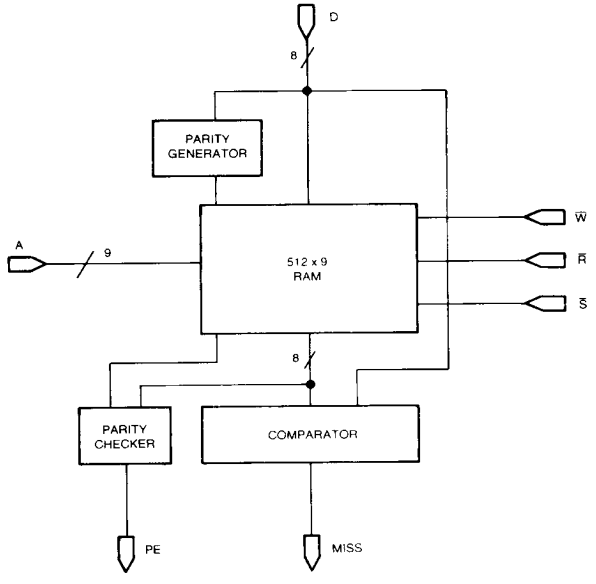
GENERAL DESCRIPTION

The Am93469 Tag Buffer combines a 512 x 9 memory with a comparator. An internal parity generator and parity checker guarantee that no misoperation occurs.

The device has three operational modes: Compare, Write, and Reset. In Compare mode, data is compared to the contents of an address location. Write mode is used to store data. Reset mode is used to clear a single 'valid bit' stream.

The Tag Buffer is designed to be used in a cache memory system for the translation of virtual addresses to physical addresses. The device can also be used in the directory and data cache. It offers state-of-the-art technology performance, while combining the functions of six or more integrated circuits into a single device.

BLOCK DIAGRAM



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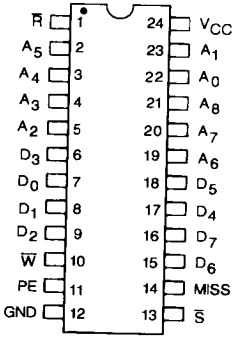
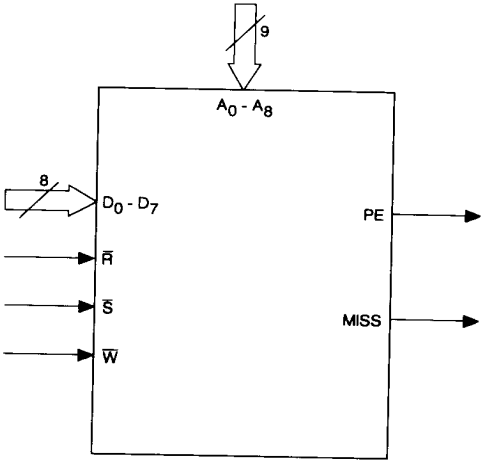
Order # 07562A

CONNECTION DIAGRAM
Top View



CD009152

LOGIC SYMBOL



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V_{CC} = Positive Power Supply
GND = Ground

PIN DESCRIPTION

$A_0 - A_8$ Address (Inputs)
Identifies memory locations.

$D_0 - D_7$ Data (Inputs)
During Compare cycle, eight bits of data are compared with address location given by $A_0 - A_8$ for equality. The result is indicated on the Comparator output pin, MISS. When $\overline{W}$ is LOW, data is written into the address location given by $A_0 - A_8$.

$\overline{R}$ Reset (Input, Active LOW)
Resets D_3 to zero.

$\overline{S}$ Chip Select (Input, Active LOW)
When $\overline{S}$ is LOW, the device is activated. A HIGH on this input will disable the chip and force PE and MISS outputs LOW, allowing easy vertical expansion.

$\overline{W}$ Write Enable (Input, Active LOW)
Must be LOW to write Data ($D_0 - D_7$) into location given by $A_0 - A_8$. PE output is LOW and MISS output HIGH during Write cycle.

MISS Comparator Miss (Output, Active HIGH)
LOW when Data ($D_0 - D_7$) equals content of memory location specified by $A_0 - A_8$. HIGH when mismatch occurs.

PE Parity Error (Output, Active HIGH)
HIGH when the nine bits of internal data do not constitute odd parity.

FUNCTIONAL DESCRIPTION

The Am93469 Tag Buffer has three modes of operation: Compare, Write, and Reset. These modes are described as follows.

Compare Mode

The eight bits of Data inputs are compared with the content of a given memory location for equality. The nine address inputs define each memory location. In this mode, $\overline{W}$ and $\overline{R}$ inputs are HIGH, and $\overline{S}$ is LOW. If the eight bits of Data inputs are exactly the same as the eight bits of data in the given memory location, the MISS output will be LOW. If not, the MISS output will be HIGH. The parity bit is not compared.

Write Mode

The eight bits of data inputs and the one bit of parity are written into the RAM array when both $\overline{S}$ and $\overline{W}$ are LOW, and $\overline{R}$ is HIGH. The MISS output is forced HIGH (the MISS output is associated with the output enable of the data cache). The Parity Error (PE) output is forced LOW.

Reset Mode

When $\overline{R}$ = LOW, $\overline{S}$ = LOW, and $\overline{W}$ = HIGH, a dedicated section of the entire array, D_3, is reset to LOW. The PE output is forced LOW during reset. The MISS output is forced HIGH. All 512 D_3 data bits are reset to a low state. The other seven bits in each address location may change to an undetermined state (HIGH or LOW).

TABLE 1. FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{S}$	$\overline{W}$	=	MISS	DESCRIPTION
				Disabled
			SS ATCH	Compare
				Reset
				Write
				Illegal

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
Suply Voltage ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs ..... −0.5 to V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −5.2 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
V_{CL}	Input Clamp Voltage	I_{IN} = −10 mA		−1.5	V
I_{IL}	Input LOW Current	V_{IN} = 0.4 V		−400	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V		40	μA
I_{SC} (Note 1)	Output Short-Circuit Current	V_{OUT} = 0.0 V		−100	mA
I_{CC}	Supply Current			185	mA

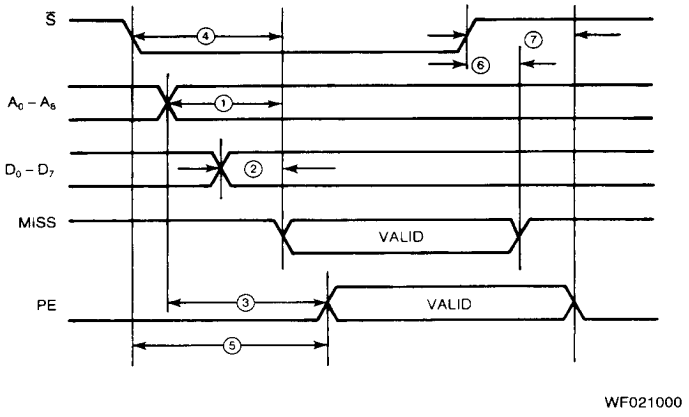
Notes: 1. No more than one output should be short circuited at a time. The duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

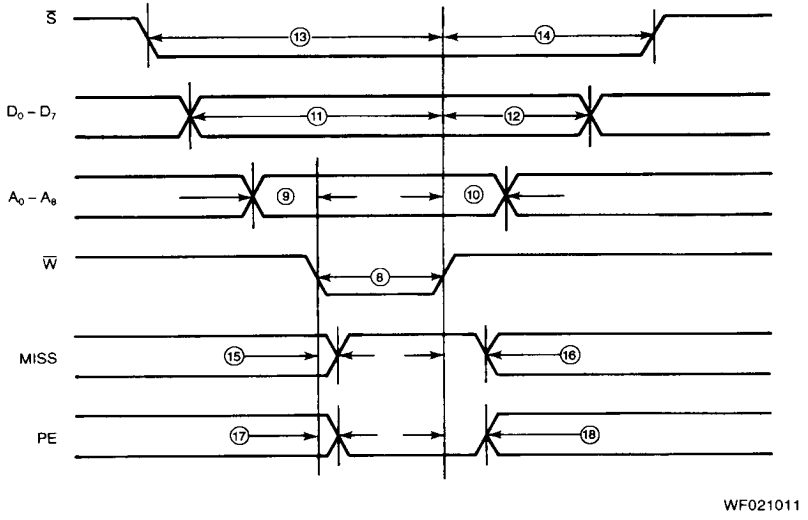
No.	Parameter Symbol	Parameter Description	Min.	Max.	Units
Compare Mode					
1	t_{AVMV}	Address to MISS		20.0	ns
2	t_{DVMV}	Data to MISS		7.0	ns
3	t_{AVPV}	Address to PE		20.0	ns
4	t_{SLMV}	$\overline{S}$ to MISS		7.0	ns
5	t_{SLPV}	$\overline{S}$ to PE		7.0	ns
6	t_{SHML}	$\overline{S}$ to MISS Recovery		7.0	ns
7	t_{SHPL}	$\overline{S}$ to PE Recovery		7.0	ns
Write Mode					
8	t_{WLWH}	Write Pulse Width	15.0		ns
9	t_{AVWL}	Address Setup	3.0		ns
10	t_{WHAX}	Address to $\overline{W}$ Hold	2.0		ns
11	t_{DVWH}	Data to $\overline{W}$ Setup	18.0		ns
12	t_{WHDX}	Data to $\overline{W}$ Hold	2.0		ns
13	t_{SLWH}	$\overline{S}$ to Setup	18.0		ns
14	t_{WHSH}	$\overline{S}$ to Select Hold	2.0		ns
15	t_{WLMH}	$\overline{W}$ to MISS		7.0	ns
16	t_{WHMX}	Write Recovery (MISS)		22.0	ns
17	t_{WLPL}	$\overline{W}$ to PE		7.0	ns
18	t_{WHPX}	Write Recovery (PE)		22.0	ns
Reset Mode					
19	t_{RLRH}	$\overline{R}$ Pulse Width	50.0		ns
20	t_{SLRL}	$\overline{S}$ to $\overline{R}$ Setup	5.0		ns
21	t_{RHSH}	$\overline{S}$ to $\overline{R}$ Hold	10.0		ns
22	t_{WHRL}	$\overline{W}$ to $\overline{R}$ Setup	5.0		ns
23	t_{RHWL}	$\overline{W}$ to $\overline{R}$ Hold	10.0		ns
24	t_{RLMH}	$\overline{R}$ to MISS HIGH		7.0	ns
25	t_{RHMX}	$\overline{R}$ to MISS Recovery		22.0	ns
26	t_{RLPL}	$\overline{R}$ to PE LOW		7.0	ns
27	t_{RHPX}	$\overline{R}$ to PE Recovery		22.0	ns

Notes: 1. All Switching Characteristics are measured at 50% of input to valid output. Both input and output timings are referenced to 1.5 V.

SWITCHING WAVEFORMS

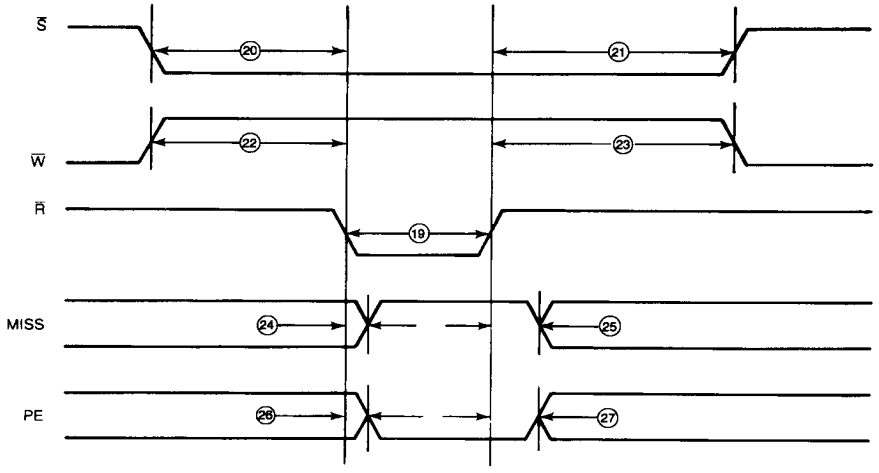


Compare Mode



Write Mode

SWITCHING WAVEFORMS (Cont.)



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Reset Mode

PHYSICAL DIMENSIONS

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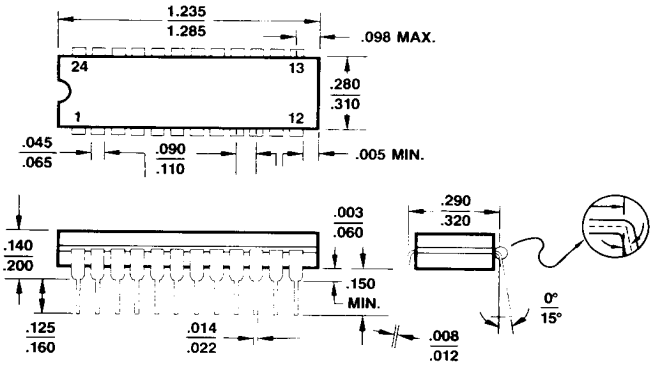

PID # 06850A

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