# 74HC4020; 74HCT4020

## 14-stage binary ripple counter

Rev. 03 — 20 January 2010 Product data sheet

## 1. General description

The 74HC4020; 74HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4020B series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4020; 74HCT4020 are 14-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0, Q3 to Q13). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

## 2. Features

- Multiple package options
- Complies with JEDEC standard no. 7A
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC4020N | –40 °C to +125 °C | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| 74HCT4020N | | | | |
| 74HC4020D | –40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HCT4020D | | | | |
| 74HC4020DB | –40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT4020DB | | | | |

**Table 1. Ordering information** *…continued*

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC4020PW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT4020PW | | | | |
| 74HC4020BQ | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT4020BQ | | | | |

## 5. Functional diagram

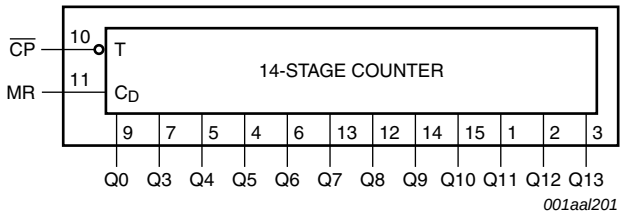



**Fig 1. Functional diagram**

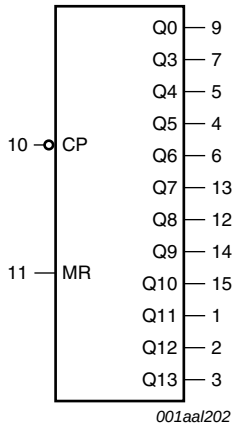



**Fig 2. Logic symbol**

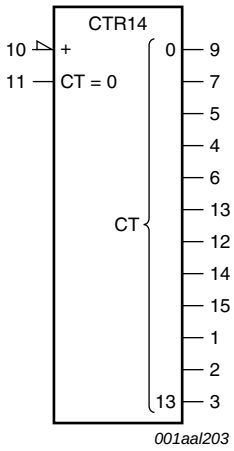



**Fig 3. IEC logic symbol**

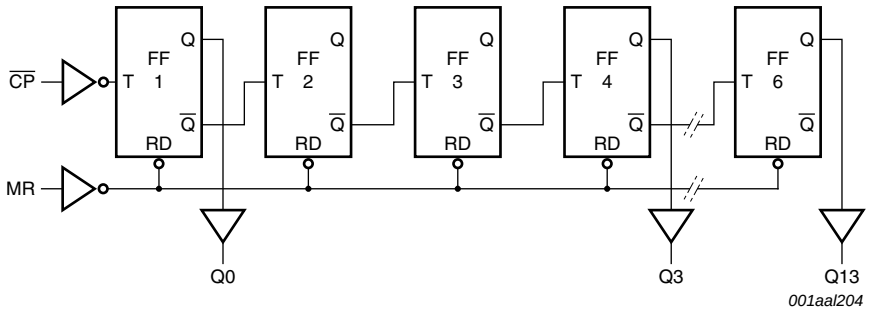



**Fig 4. Logic diagram**

# 6. Pinning information

## 6.1 Pinning

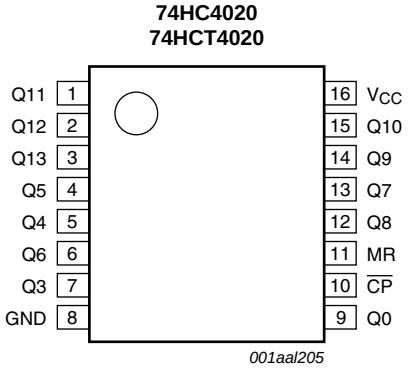
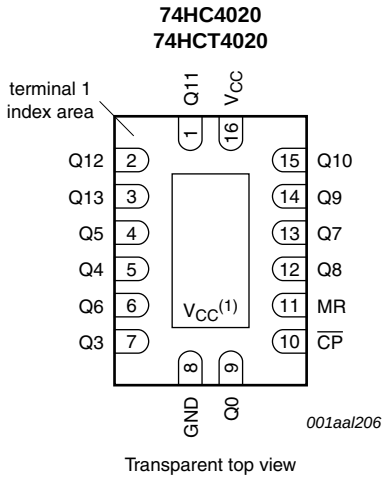



**Fig 5. Pin configuration DIP16, SO16, SSOP16 and TSSOP16**




Transparent top view

(1) The substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input. It is recommended that no connection is made at all.

**Fig 6. Pin configuration DHVQFN16**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Q0, Q3 to Q13 | 9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3 | output |
| GND | 8 | ground (0 V) |
| $\overline{CP}$ | 10 | clock input (HIGH-to-LOW, edge-triggered) |
| MR | 11 | master reset input (active HIGH) |
| $V_{CC}$ | 16 | positive supply voltage |

# 7. Functional description

**Table 3. Function table**

| Input | | Output |
|---|---|---|
| $\overline{CP}$ | MR | Q0, Q3 to Q13 |
| ↑ | L | no change |
| ↓ | L | count |
| X | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

## 7.1 Timing diagram

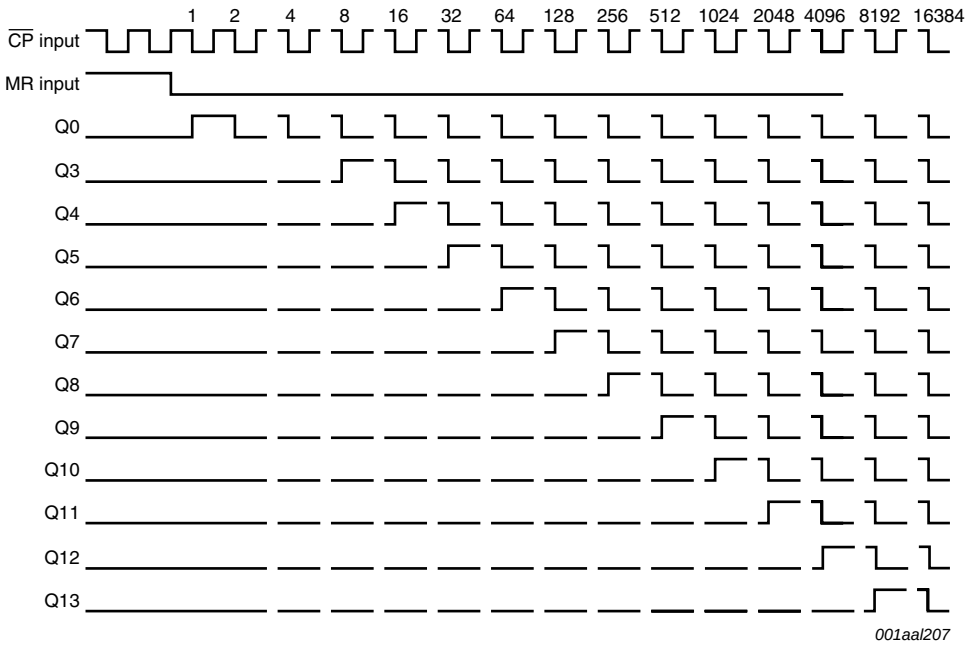



**Fig 7. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O < V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | ±50 | mA |
| $I_{GND}$ | ground current | | | - | ±50 | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | [1] | | | |
| | DIP16 package | | | - | 750 | mW |
| | SO16, SSOP16, TSSOP16 and DHVQFN16 packages | | | - | 500 | mW |

[1] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.
For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.
For SSOP16 and TSSOP16 packages: $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN16 package: $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | 74HC4020 | | | 74HCT4020 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | except for Schmitt-trigger inputs | | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | - | - | - | ns/V |
| $T_{amb}$ | ambient temperature | | −40 | +25 | +125 | −40 | +25 | +125 | °C |

## 10. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC4020** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = −20 μA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = −20 μA; $V_{CC}$ = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O$ = −4.0 mA; $V_{CC}$ = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | | $I_O$ = −5.2 mA; $V_{CC}$ = 6.0 V | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 μA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| **74HCT4020** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = −20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = −4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 20 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | μA |

**Table 6. Static characteristics** *...continued*

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V | - | - | 8.0 | - | 80 | - | 160 | µA |
| $\Delta I_{CC}$ | additional supply current | $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V | | | | | | | | |
| | | pin MR | - | 110 | 396 | - | 495 | - | 539 | µA |
| | | pin $\overline{CP}$ | - | 85 | 306 | - | 383 | - | 417 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see Figure 10*

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC4020** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $\overline{CP}$ to Q0; see Figure 8 | [1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | | - | 39 | 140 | - | 175 | - | 210 | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | | - | 14 | 28 | - | 35 | - | 42 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | | - | 11 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V; $C_L = 50$ pF | | - | 11 | 24 | - | 30 | - | 36 | ns |
| | | Qn to Qn+1; see Figure 9 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | | - | 22 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | | - | 8 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | | - | 6 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V; $C_L = 50$ pF | | - | 6 | 13 | - | 16 | - | 19 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | MR to Qn; see Figure 8 | | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | | - | 55 | 170 | - | 215 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | | - | 20 | 34 | - | 43 | - | 51 | ns |
| | | $V_{CC} = 5.0$ V; $C_L = 15$ pF | | - | 17 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V; $C_L = 50$ pF | | - | 16 | 29 | - | 37 | - | 43 | ns |
| $t_t$ | transition time | Qn; see Figure 8 | [2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V; $C_L = 50$ pF | | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5$ V; $C_L = 50$ pF | | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0$ V; $C_L = 50$ pF | | - | 6 | 13 | - | 16 | - | 19 | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Figure 10*

| Symbol | Parameter | Conditions | | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_W$ | pulse width | $\overline{CP}$ HIGH or LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V; $C_L$ = 50 pF | | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 16 | 4 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V; $C_L$ = 50 pF | | 14 | 3 | - | 17 | - | 20 | - | ns |
| | | MR HIGH; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V; $C_L$ = 50 pF | | 80 | 17 | - | 100 | - | 120 | - | ns |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 16 | 6 | - | 20 | - | 24 | - | ns |
| | | $V_{CC}$ = 6.0 V; $C_L$ = 50 pF | | 14 | 5 | - | 17 | - | 20 | - | ns |
| $t_{rec}$ | recovery time | MR to $\overline{CP}$; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V; $C_L$ = 50 pF | | 50 | 6 | - | 65 | - | 75 | - | ns |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 10 | 2 | - | 13 | - | 15 | - | ns |
| | | $V_{CC}$ = 6.0 V; $C_L$ = 50 pF | | 9 | 2 | - | 11 | - | 13 | - | ns |
| $f_{max}$ | maximum frequency | see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 2.0 V; $C_L$ = 50 pF | | 6.0 | 30 | - | 4.8 | - | 4.0 | - | MHz |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 30 | 92 | - | 24 | - | 20 | - | MHz |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 101 | - | - | - | - | - | MHz |
| | | $V_{CC}$ = 6.0 V; $C_L$ = 50 pF | | 35 | 109 | - | 28 | - | 24 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | | [3] | - | 19 | - | - | - | - | - | pF |
| **74HCT4020** | | | | | | | | | | | |
| $t_{pd}$ | propagation delay | $\overline{CP}$ to Q0; see Figure 8 | [1] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | - | 18 | 36 | - | 45 | - | 54 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 15 | - | - | - | - | - | ns |
| | | Qn to Qn+1; see Figure 9 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | - | 8 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 6 | - | - | - | - | - | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | MR to Qn; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | - | 22 | 45 | - | 56 | - | 68 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | | - | 19 | - | - | - | - | - | ns |
| $t_t$ | transition time | Qn; see Figure 8 | [2] | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | - | 7 | 15 | - | 19 | - | 22 | ns |
| $t_W$ | pulse width | $\overline{CP}$ HIGH or LOW; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 20 | 7 | - | 25 | - | 30 | - | ns |
| | | MR HIGH; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 20 | 8 | - | 25 | - | 30 | - | ns |
| $t_{rec}$ | recovery time | MR to $\overline{CP}$; see Figure 8 | | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | | 10 | 2 | - | 13 | - | 15 | - | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND (ground = 0 V); $C_L$ = 50 pF unless otherwise specified; for test circuit, see Figure 10*

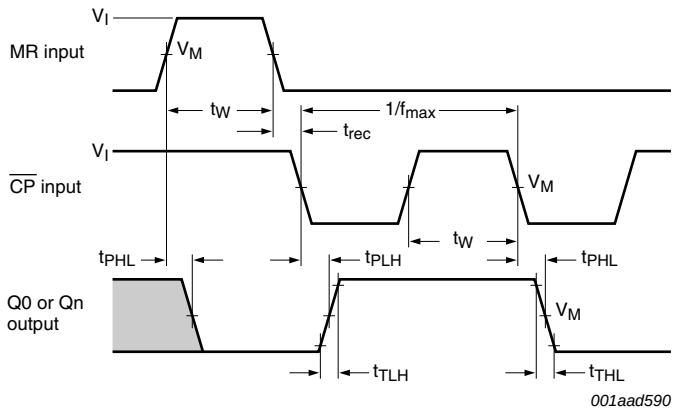
| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $f_{max}$ | maximum frequency | see Figure 8 | | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $C_L$ = 50 pF | 25 | 47 | - | 20 | - | 17 | - | MHz |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | - | 52 | - | - | - | - | - | MHz |
| $C_{PD}$ | power dissipation capacitance | [3] | - | 20 | - | - | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.

[2] $t_t$ is the same as $t_{THL}$ and $t_{TLH}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V.

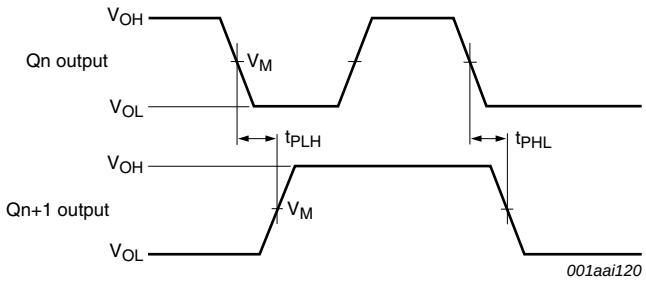
## 12. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 8. Clock ($\overline{CP}$) to output (Qn) propagation delays, clock pulse width, output transition times, maximum clock pulse frequency, master reset (MR) pulse width, master reset to output (Qn) propagation delays and master reset to clock (CP) recovery time**



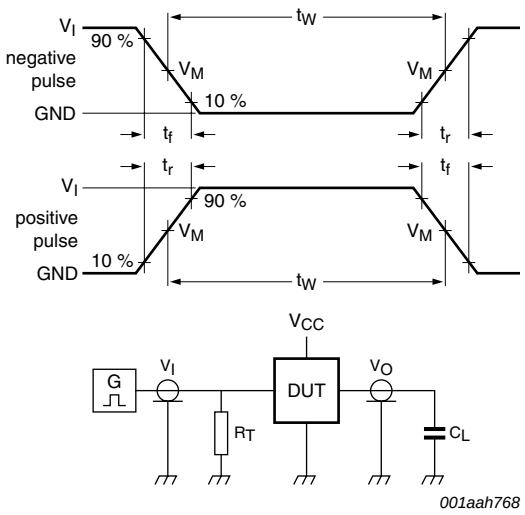

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 9. Waveforms showing the output Qn to output Qn+1 propagation delays**

**Table 8. Measurement points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| 74HC4020 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74HCT4020 | 1.3 V | 1.3 V |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

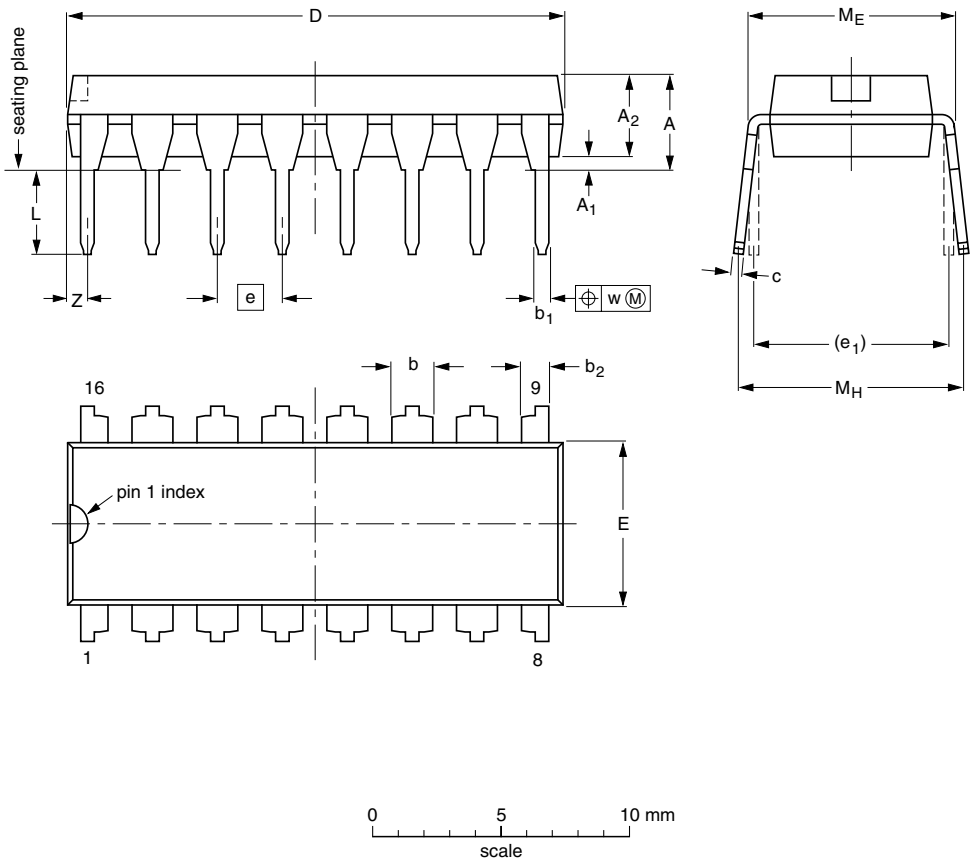
**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load |
|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ |
| 74HC4020 | $V_{CC}$ | 6 ns | 15 pF, 50 pF |
| 74HCT4020 | 3 V | 6 ns | 15 pF, 50 pF |

## 13. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

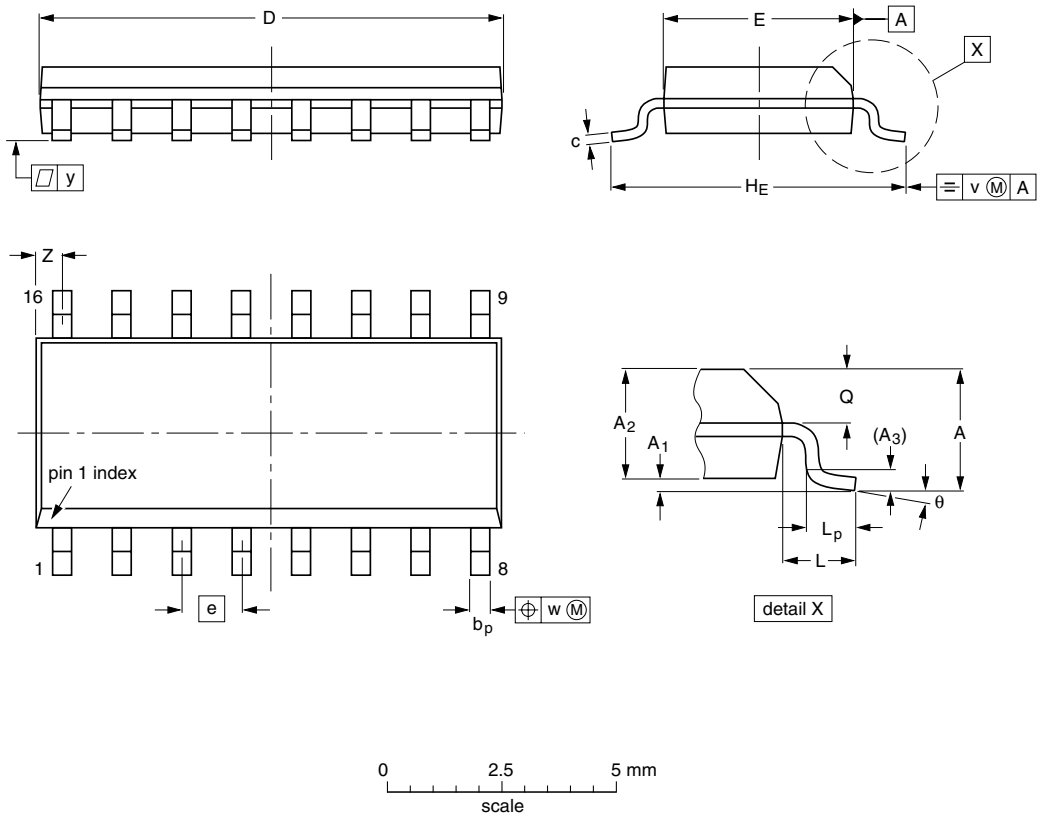
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 11. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

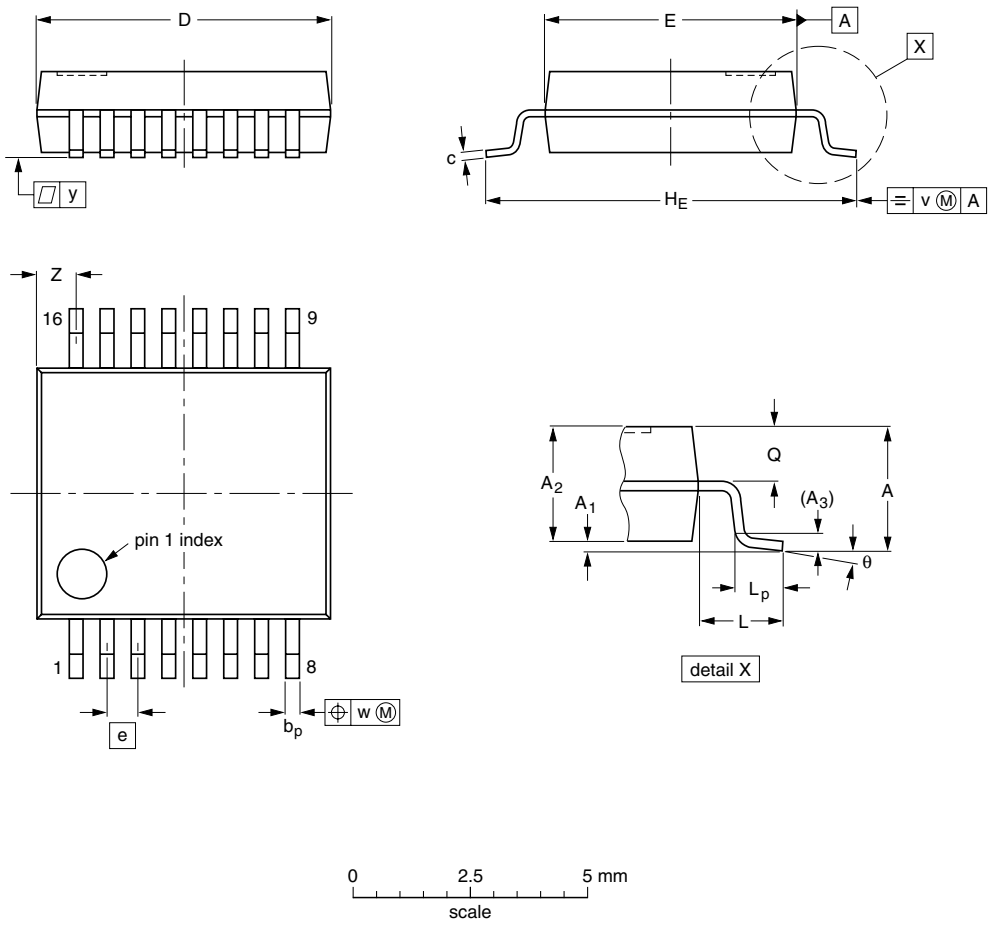
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 12. Package outline SOT109-1 (SO16)**

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | 8°<br>0° |

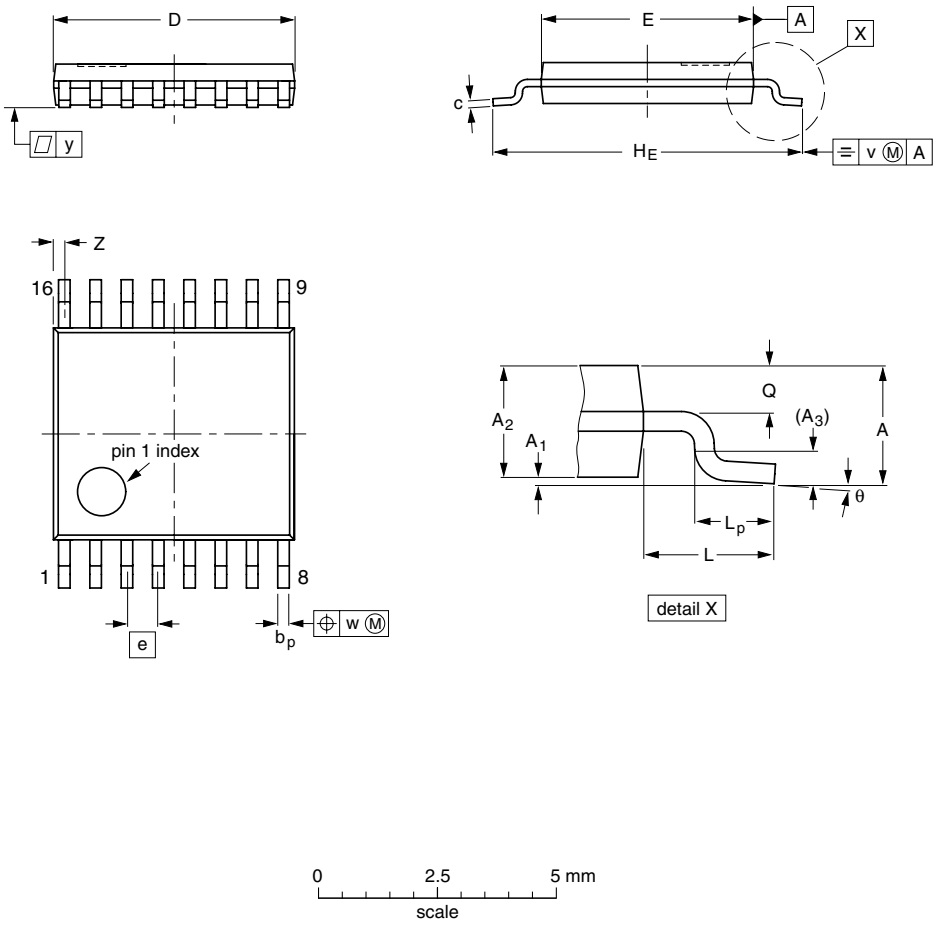
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT338-1 (SSOP16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

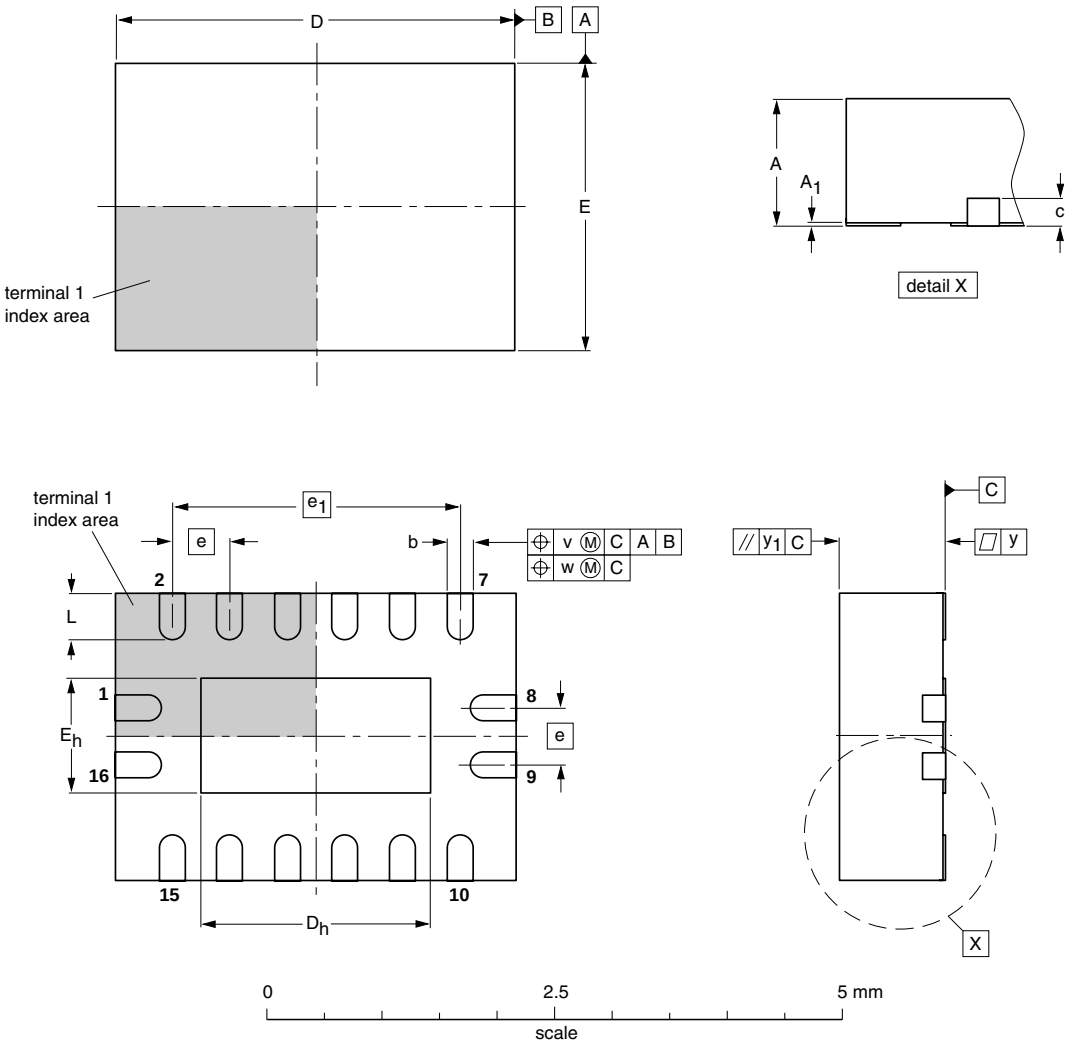
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 14. Package outline SOT403-1 (TSSOP16)**

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 15. Package outline SOT763-1 (DHVQFN16)**

## 14. Abbreviations

**Table 10. Abbreviations**

| Acronym | Abbreviation |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |

## 15. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT4020_3 | 20100120 | Product data sheet | - | 74HC_HCT4020_CNV_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Added type number 74HC4020BQ, 74HCT4020BQ (DHVQFN16 / SOT763-1 package).<br>• Reference to family specifications is replaced by the actual information: Section 4 “Ordering information”, Section 6 “Pinning information”, Section 8 “Limiting values”, Section 9 “Recommended operating conditions”, Section 10 “Static characteristics”, Figure 10 “Test circuit for measuring switching times” | | | |
| 74HC_HCT4020_CNV_2 | 19970901 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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