REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE
93-05-12

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, HIGH INTEGRATION EMBEDDED PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93109
A	67268	

SHEET 1 OF 23

DESC FORM 193
JUL 91

5962-E231-93

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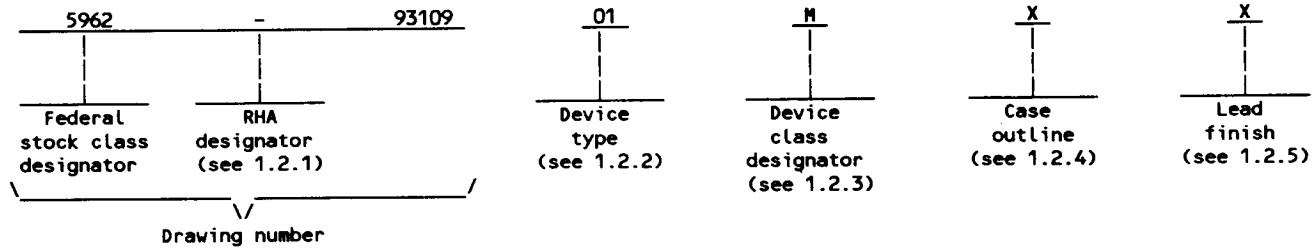
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	80C186EB-8	High integration embedded processor
02	80C186EB-13	High integration embedded processor
03	80C186EB-16	High integration embedded processor

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA5-P88	88	Ceramic, pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

Storage temperature range	-65°C to +150°C
Supply voltage with respect to ground range	-1.0 V dc to +7.0 V dc
Voltage on any pin with respect to ground	-1.0 V dc to +7.0 V dc
Maximum power dissipation (P_D)	0.5 W
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Maximum junction temperature	150°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage, V_{CC}	4.5 V dc ≤ V_{CC} ≤ 5.5 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	2/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage 3/	V_{IL}		1,2,3	All	-0.5 2/	0.3 V_{CC}	V
Input high voltage	V_{IH}		1,2,3	All	.7 V_{CC}	V_{CC} +0.5 2/	V
Input hysterisis on RESIN	V_{HYS}		1,2,3	All	0.5		V
Output low voltage	V_{OL}	I_{OL} = 3.0 mA V_{CC} = 4.5 V	1,2,3	All		0.45	V
Output high voltage	V_{OH}	I_{OH} = -2.0 mA V_{CC} = 4.5 V	1,2,3	All	V_{CC} -.5		V
Input leakage current	I_{LI}	$0\ V \le V_{IN} \le V_{CC}$ V_{CC} = 5.5 V PIN = CLKIN	1,2,3	All		+50	µA
		V_{IN} = 0 V PIN = ERROR V_{CC} = 5.5 V	1,2,3	All	-7	-.275	mA
		$V_{IN} = V_{CC}$ PIN = PEREQ V_{CC} = 5.5 V	1,2,3	All	.275	7	mA
		$V_{IN} = .7V_{CC}$ PINS = A19/ONCE A16-A18, LOCK V_{CC} = 5.5 V 11/	1,2,3	All	-.275	- 5	mA
		$0\ V \le V_{IN} \le V_{CC}$ ALL OTHER INPUTS V_{CC} = 5.5 V	1,2,3	All		+15	µA
Output leakage current 4/	I_{LO}	$.45\ V \le V_{IN} \le V_{CC}$ V_{CC} = 5.5 V	1,2,3	All	-15	+15	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current cold (RESET) 5/	I_{CC}	V_{CC} = 5.5 V	1,2,3	01 02 03		45 73 90	mA
Supply current idle 6/	I_{ID}	V_{CC} = 5.5 V	1,2,3	01 02 03		31 48 63	mA
Supply current power down 7/	I_{PD}	V_{CC} = 5.5 V	1,2,3	All		100	µA
Input capacitance	C_{IN}	Frequency = 1 MHz See 4.4.1c	4	All		15	pF
Input/output capacitance	C_O	Frequency = 1 MHz See 4.4.1c	4	All		15	pF
Functional test		See 4.4.1b	7,8	All			
CLKIN frequency	t_F		9,10,11	01 02 03	0 0 0 2/	16 26.08 32	MHz
CLKIN period	t_C	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02 03	62.5 38.34 31.25		ns
CLKIN high time	t_{CH}	At V_{IH} See figure 3 V_{CC} = 4.5 V	9,10,11	01 02 03	15 12 10		ns
CLKIN low time	t_{CL}	At V_{IL} See figure 3 V_{CC} = 4.5 V	9,10,11	01 02 03	15 12 10		ns
CLKIN rise time 2/	t_{CR}	See figure 3 V_{CC} = 4.5 V	9,10,11	All	1	8	ns
CLKIN fall time 2/	t_{CF}	V_{CC} = 4.5 V See figure 3	9,10,11	All	1	8	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKIN to CLKOUT delay	t_{CD}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02 03	0 0 0	27 23 20	ns
CLKOUT period	t		9,10,11	All		$2*t_C$	ns
CLKOUT high time	t_{PH}		9,10,11	All	(t/2) -5	(t/2) +5	ns
CLKOUT low time	t_{PL}		9,10,11	All	(t/2) -5	(t/2) +5	ns
CLKOUT rise time	t_{PR}		9,10,11	All		6	ns
CLKOUT fall time	t_{PF}		9,10,11	All		6	ns
CLKOUT high to output valid ALE,S2:0,DEN,DT/R,BHE, LOCK, A19:16 8/	t_{CHOV1}		9,10,11	01 02 03	1 1 1	30 25 22	ns
CLKOUT high to output valid GCS0:7,LCS,UCS,NCS, RD,WR 9/	t_{CHOV2}		9,10,11	01 02 03	1 1 1	35 30 27	ns
CLKOUT low to output valid BHE,DEN,LOCK,RESOUT, HLDA,TOOUT,1OUT,A19:16	t_{CLOV1}		9,10,11	01 02 03	1 1 1	30 25 22	ns
CLKOUT low to output valid RD,WR,GCS0:7,LCS,UCS, AD15:0,NCS,INTA1:0,S2:0	t_{CLOV2}		9,10,11	01 02 03	1 1 1	35 30 27	ns
CLKOUT high to output float RD,WR,BHE,DT/R,LOCK, S2:0,A9:16 2/	t_{CHOF}		9,10,11	01 02 03	0 0 0	30 25 25	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKOUT low to output float DEN, AD15:0 2/	t_{CLOF}	See figure 3 V_{CC} = 4.5 V	9,10,11	01 02 03	0 0 0	35 25 25	ns
CLKOUT high to input setup test, NMI,INT4:0,BCLK1:0, T1:OIN,READY,CTS1:0, P2.6, P2.7	t_{CHIS}		9,10,11	ALL	10		ns
CLKOUT high to input hold test, NMI,INT4:0,BCLK1:0, T1:OIN,READY,CTS1:0	t_{CHIH}		9,10,11	ALL	3		ns
CLKOUT low to input setup AD15:0,READY,HOLD,PEREQ, ERROR	t_{CLIS}		9,10,11	ALL	10		ns
CLKOUT high to input hold AD15:0,READY,HOLD,PEREQ, ERROR	t_{CLIH}		9,10,11	ALL	3		ns
ALE high to ALE low	t_{LHLL}		9,10,11	ALL	t-15		ns
ADD valid to ALE low	t_{AVLL}		9,10,11	ALL	(t/2) -10		ns
CHIP selects valid to ALE low	t_{PLLL}		9,10,11	ALL	(t/2) -10		ns
ADD hold from ALE low	t_{LLAX}		9,10,11	ALL	(t/2) -10		ns
ALE low to WR low	t_{LLWL}		9,10,11	ALL	(t/2) -15		ns
ALE low to RD low	t_{LLRL}		9,10,11	ALL	(t/2) -15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
WR high to ALE high	t_{WHLH}	See figure 3 V_{CC} = 4.5 V	9,10,11	ALL	(t/2) -10		ns
Add float to RD low 2/	t_{AFRL}		9,10,11	ALL	0		ns
RD low to RD high	t_{RLRH}		9,10,11	ALL	(2t)-5		ns
WR low to WR high	t_{WLWH}		9,10,11	ALL	(2t)-5		ns
RD high to add ACTIVE	t_{RHAV}		9,10,11	ALL	t-15		ns
DATA out hold after WR high	t_{WHDX}		9,10,11	ALL	t-15		ns
WR high to CS high	t_{WHPH}		9,10,11	ALL	(t/2) -10		ns
RD high to CS high	t_{RHPH}		9,10,11	ALL	(t/2) -10		ns
CS active to CS active	t_{PHPL}		9,10,11	ALL	(t/2) -10		ns
ONCE active to RESIN high 2/	t_{OVRH}		9,10,11	ALL	t		ns
ONCE hold from RESIN high 2/	t_{RHOX}		9,10,11	ALL	t		ns
TXD clock period 10/	t_{XLXL}		9,10,11	ALL	t*(n+1)		ns
TXD CLK low to high 10/ (n > 1)	t_{XLXH}		9,10,11	ALL	t-35	t+35	ns
TXD CLK low to high 10/ (n = 1)	t_{XLXH}		9,10,11	ALL	t-35	t+35	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TXD CLK high to low (n > 1) 10/	t_{XHXL}	See figure 3 V_{CC} = 4.5 V	9,10,11	ALL	(n-1)*t	(n-1)*t	ns
TXD CLK high to low (n = 1) 10/	t_{XHXL}		9,10,11	ALL	t-35	t+35	ns
RXD output data setup to TXD CLK high (n > 1) 10/	t_{QVXH}		9,10,11	ALL	(n-1)*t -35		ns
RXD output data setup to TXD CLK high (n = 1) 10/	t_{QVXH}		9,10,11	ALL	t-35		ns
RXD output data hold after TXD CLK high (n > 1) 10/	t_{XHQX}		9,10,11	ALL	2t-35		ns
RXD output data hold after TXD CLK high (n = 1) 10/	t_{XHQX}		9,10,11	ALL	t-35		ns
RXD output data float after last TXD CLK high 2/	t_{XHQZ}		9,10,11	ALL		t+20	ns
RXD output data setup to TXD CLK high	t_{DVXH}		9,10,11	ALL	t+20		ns
RXD input data hold after TDX CLK high 2/	t_{XHDX}		9,10,11	ALL	0		ns

1/ All testing to be performed to worst-case test conditions unless otherwise specified. All timings are measured at 50% of V_{CC}, except rise and fall times, which are measured between 20% and 80% of V_{CC}. All pins are loaded to 50 pF. The following pins are active low: DEN, S0, S1, S2, BHE, WR, RD, ERROR, NCS, CTS1(P2.4/CTS1), CTS0, RESIN, UCS, LCS, GCS0(P1.0/GCS0), GCS1(P1.1/GCS1), GCS3(P1.2/GCS3), GCS3(P1.3/GCS3), GCS4(P1.4/GCS4), GCS5(P1.0/GCS5), GCS6(P1.1/GCS6), GCS7(P1.2/GCS7), R(DRT/R), LOCK, and TEST(TEST/BUSY).
2/ Guaranteed by design characterization but not tested.
3/ A16-A18, A19/ONCE, LOCK are not tested or guaranteed at this level.
4/ Pins being floated by invoking the ONCE mode or by asserting HOLD. OSCOUT is not tested.
5/ Measured with device in reset and at worst case frequency, V_{CC}, and with all outputs loaded to 50 pF. All floating outputs are driven to V_{CC} or ground.
6/ Device in HALT (idle mode active) and worst case frequency, V_{CC}, and temperature with all outputs loaded to 50 pF. All floating outputs are driven to V_{CC} or ground.
7/ Device in HALT (power down mode active) and worst case frequency, V_{CC}, and temperature with all outputs loaded to 50 pF. All floating outputs are driven to V_{CC} or ground.
8/ t_{CHOV1} applies to BHE, LOCK, and A19:16 only after a HOLD release.
9/ t_{CHOV2} applies to RD and WR only after a HOLD release.
10/ n is the value of the BxCMP register ignoring the I_{CLK} Bit (i.e., I_{CLK} = 0).
11/ These pins have an internal pull-up device that is active while RESIN is low and ONCE mode is not active. Sourcing more current than specified (on any of these pins) may invoke a factory tested mode.

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Pin	Name	Pin	Name	Pin	Name	Pin	Name
1A	DEN#	1M	AD5	12N	N/C	13B	N/C
2B	SO#	1N	AD12	13N	RXD0	13A	INT1
1B	S1#	2N	AD4	13M	TXD0	12A	INT0
2C	S2#	3M	AD11	12L	CTS0#	11B	UCS#
1C	BHE#	3N	AD3	13L	P2.6	11A	LCS#
2D	ALE	4M	AD10	12K	P2.7	10B	P1.0/GCS0#
1D	WR#	4N	AD2	13K	T1IN	10A	P1.1/GCS1#
2E	RD#	5M	AD9	12J	T1OUT	9B	P1.2/GCS2#
1E	ERROR#	5N	AD1	13J	T0IN	9A	P1.3/GCS3#
2F	V_{SS}	6M	V_{SS}	12H	T0OUT	8B	P1.4/GCS4#
1F	V_{CC}	6N	V_{CC}	13H	CLKOUT	8A	V_{CC}
2G	V_{SS}	7M	V_{SS}	12G	V_{SS}	7B	V_{SS}
1G	A19 /ONCE#	7N	N/C	13G	V_{CC}	7A	P1.5/GCS5#
2H	A18	8M	AD8	12F	CLKIN	6B	P1.6/GCS6#
1H	A17	8N	AD0	13F	OSCOUT	6A	P1.7/GCS7#
2J	A16	9M	NCS#	12E	PEREQ	5B	READY
1J	AD15	9N	P2.2/B CLK1	13E	RESOUT	5A	NMI
2K	AD7	10M	P2.1/T XD1	12D	RESIN#	4B	DRT/R#
1K	AD14	10N	P2.0/R XD1	13D	PDTMR	4A	LOCK#
2L	AD6	11M	P2.4/C TS1#	12C	INT4	3B	TEST#/BUSY
1L	AD13	11N	P2.3/S INT1	13C	INT3	3A	HOLD
2M	N/C	12M	P2.5/B LCK0	12B	INT2	2A	HLDA

- Indicates an active low signal

FIGURE 1. Terminal connections.

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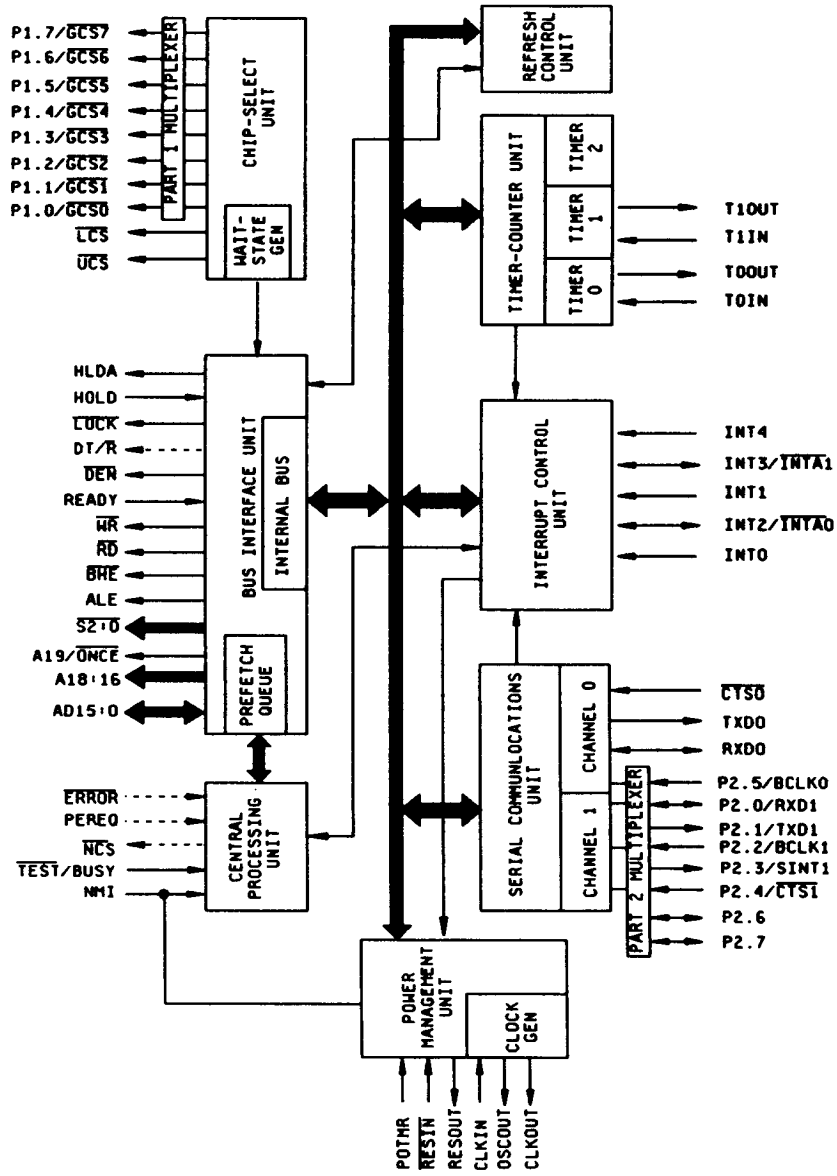

FIGURE 2. Block diagram.

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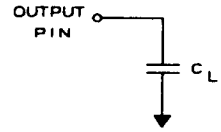

C_L = 50 pF for all signals

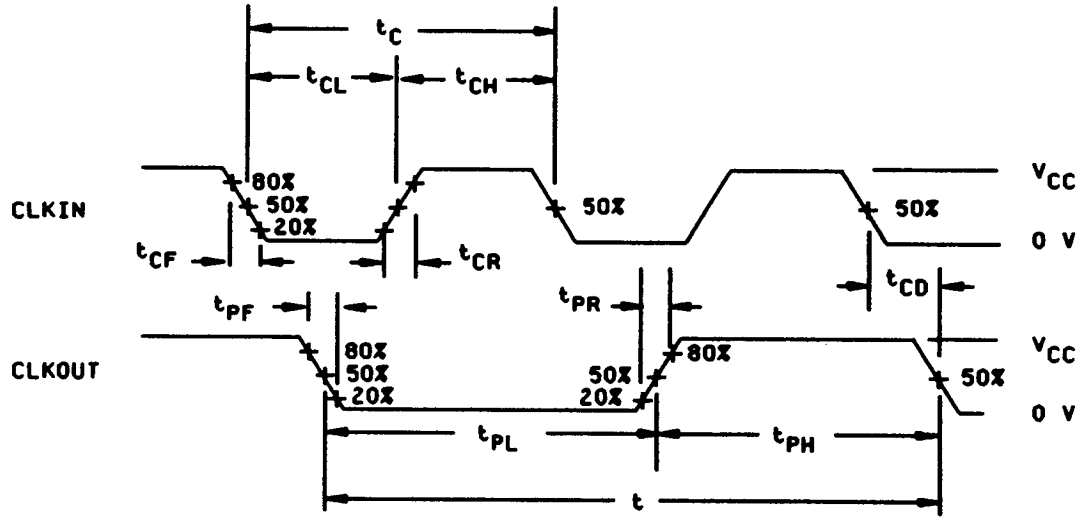

FIGURE 3. Timing waveforms.

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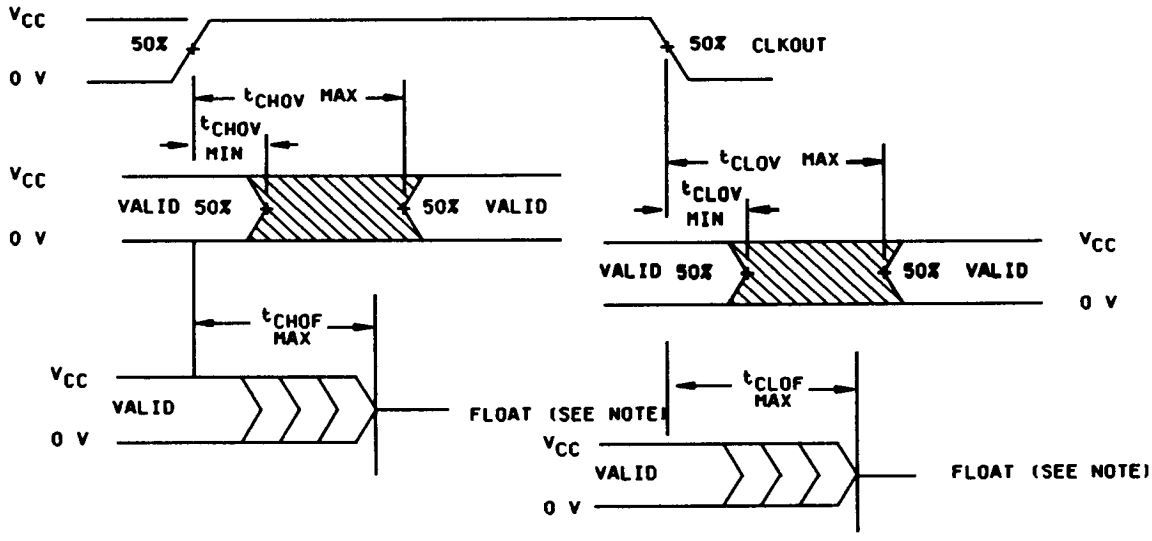
Output delay and float waveform



NOTE: 20% V_{CC} < FLOAT < 80% V_{CC}.

Input setup and hold

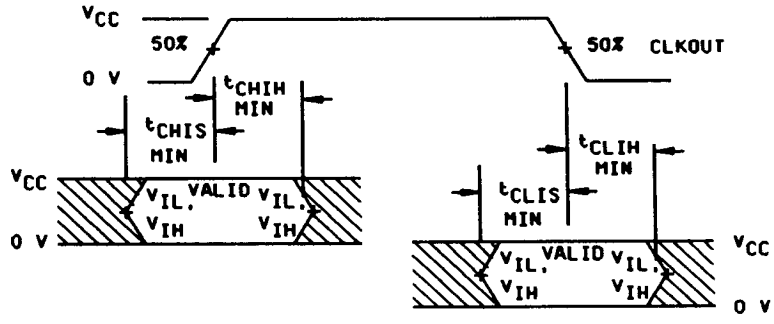


FIGURE 3. Timing waveforms - Continued.

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		REVISION LEVEL	SHEET 14

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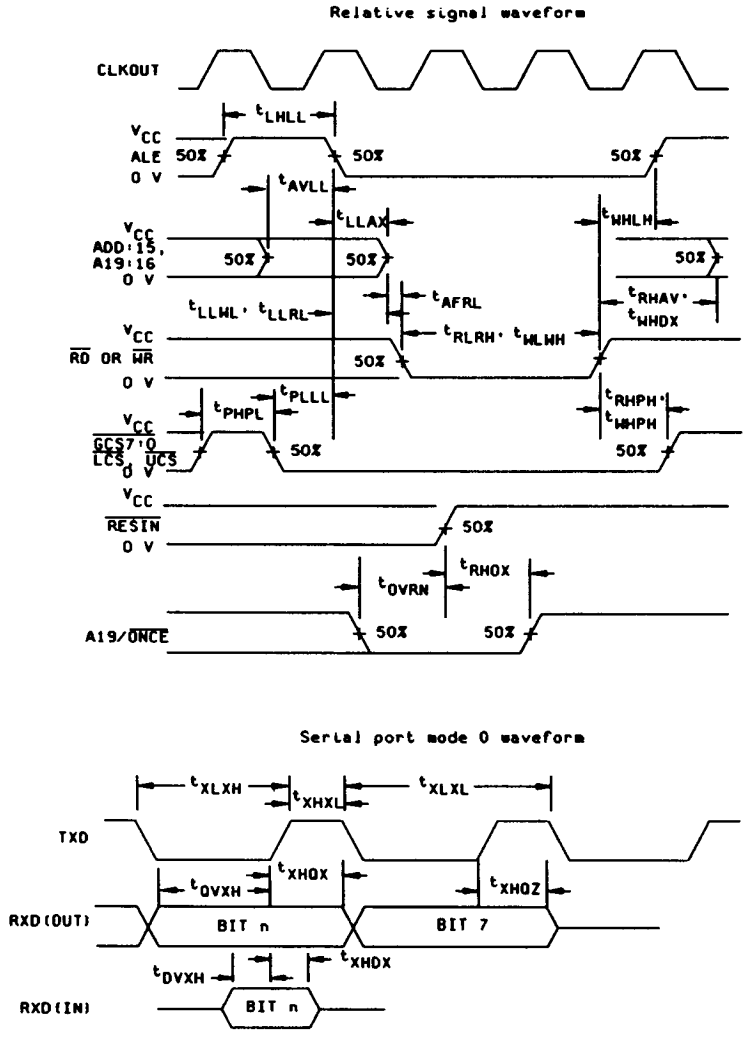

FIGURE 3. Timing waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

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4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_O) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)					
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group B end-point electrical parameters (see 4.4)			2,8A,10		
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10		2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)					

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

TABLE III. Pin descriptions.

Name	Type	Description
V_{CC}		Power connections consist of four pins which must be shorted externally to a V_{CC} board plane.
V_{SS}		Ground connections consist of six pins which must be shorted externally to a V_{SS} board plane.
CLKIN	1	Clock input is an input for an external clock. An external oscillator operating at two times the required M80C186EB operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
CLKIN	I A(E)	Clock input is an input for an external clock. An external oscillator operating at two times the required M80C186EB operating frequency can be connected to CLKIN. For crystal operation, CLKIN (along with OSCOUT) are the crystal connections to an internal Pierce oscillator.
OSCOUT	O H(Q) R(Q) P(Q)	Oscillator output is only used when using a crystal to generate the external clock. OSCOUT (along with CLKIN) are the crystal connections to an internal Pierce oscillator. This pin is not to be used as 2X clock output for non-crystal applications (i.e., this pin is N.C. for non-crystal applications). OSCOUT does not float in ONCE mode.
CLKOUT	O H(Q) R(Q) P(Q)	Clock output provides a timing reference for inputs and outputs of the processor, and is one-half the input clocks (CLKIN) frequency. CLKOUT has a 50% duty cycle and transitions every falling edge of CLKIN.
$\overline{\text{RESIN}}$	I A(L)	Reset in causes the M80C186EB to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active. The rising edge (low-to-high) transition synchronizes CLKOUT when CLKIN before the M80C186EB begins fetching opcodes at memory location OFFFFOH.
RESOUT	O H(0) R(1) P(0)	Reset output that indicates the M80C186EB is currently in the reset state. RESOUT will remain active as long as RESIN remains active.
PDTMR	I/O A(L) H(WH) R(Z) P(1)	Power-down timer pin (normally connected to an external capacitor) that determines the amount of time the M80C186EB waits after an exit from power down before resuming normal operation. The duration of time required will depend on the startup characteristics of the crystal oscillator.
NMI	I A(E)	Non-maskable interrupt input causes a type-2 interrupt to be serviced by the CPU. NMI is latched internally.
$\overline{\text{TEST/BUSY}}$	I	TEST is used during the execution of the WAIT instruction to suspend CPU operation until the pin is sampled active (LOW). $\overline{\text{TEST}}$ is alternately known as BUSY when interfacing with an M80C187 numerics coprocessor.

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TABLE III. Pin descriptions - Continued.

Name	Type	Description
AD15:0	I/O S(L) H(Z) R(Z) P(X)	These pins provide a multiplexed Address and Data bus. During the address phase of the bus cycle, address bits 0 through 15 are presented on the bus and can be latched using ALE 8- or 16-bit data information is transferred during the data phase of the bus cycle.
A18:16 A19/ONCE	H(Z) R(WH) P(X)	These pins provide multiplexed Address during the address phase of the bus cycle. Address bits 16 through 19 are presented on these pins and can be latched using ALE. These pins are driven to a logic 0 during the data phase of the bus cycle. During a processor reset (RESIN) active), A19/ONCE is used to enable ONCE mode. A18:16 must not be driven low during reset or improper M80C186EB.
$\overline{S2:0}$	0 H(Z) R(Z) P(1)	Bus cycle Status are encoded on these pins to proide bus transaction information. S2:0 are encoded as follows: S2 S1 S0 Bus Cycle initiated 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive (no bus activity)
ALE	0 H(0) R(0) P(0)	Address Latch Enable output is used to strobe address information into a transparent type latch during the address phase of the bus cycle.
$\overline{BHE}$	0 H(Z) R(Z) P(X)	Byte High Enable output to indicate that the bus cycle in progress is transferring data over the upper half of the data bus. BHE and A0 have the following logical encoding: A0 BHE Encoding 0 0 Word Transfer 0 1 Even Byte Transfer 1 0 Odd Byte Transfer 1 1 Refresh Operation
$\overline{RD}$	0 H(Z) R(Z) P(1)	READ output signals that the accessed memory or I/O device must drive data information onto the data bus.
$\overline{WR}$	0 H(Z) R(Z) P(1)	WRITE output signals that data available on the data bus are to be written into the accessed memory or I/O device.
READY	I A(L) S(L)	READY input to signal the completion of a bus cycle. READY must be active to terminate any M80C186EB bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.
$\overline{DEN}$	0 H(Z) R(Z) P(1)	Data Enable output to control the enable of bi-directional transceivers when buffering a M80C186EB system. DEN is active only when data is to be transferred on the bus.

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TABLE III. Pin descriptions - Continued.

Name	Type	Description
DT/$\overline{R}$	O H(Z) R(Z) P(X)	Data Transmit/Receive output controls the direction of a bi-directional buffer when buffering an M80C186EB system.
$\overline{LOCK}$	I/O H(Z) R(WH) P(1)	LOCK output indicates that the bus cycle in progress is not to be interrupted. The M80C186EB will not service other bus requests (such as HOLD) while LOCK is active. This pin is configured as a weakly held high input while RESIN is active and must not be driven low.
HOLD	I A(L)	HOLD request input to signal that an external bus master wishes to gain control of the local bus. The M80C186EB will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
HLDA	O H(1) R(0) P(0)	Hold Acknowledge output to indicate that the M80C186EB has relinquish control of the local bus. When HLDA is asserted, the M80C186EB will (or has) floated its data bus and control signals allowing another bus master to drive the signal directly.
$\overline{NCS}$	O H(1) R(1) P(1)	Numerics Coprocessor Select output is generated when accessing a numerics coprocessor.
$\overline{ERROR}$	I A(L)	ERROR input that indicates the last numerics coprocessor operation resulted in an exception condition. An interrupt TYPE 16 is generated if ERROR is sampled active at the beginning of a numerics operation.
PEREQ	I A(L)	Co-Process Request signals that a data transfer between an External Numerics Coprocessor and Memory is pending.
$\overline{UCS}$	O H(1) R(1) P(1)	Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. After reset, UCS is configured to be active for memory accesses between OFFC00H and OFFFFFH.
$\overline{LCS}$	O H(1) R(1) P(1)	Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user. LCS is inactive after a reset.
P1.0/$\overline{GCS0}$ P1.1/$\overline{GCS1}$ P1.2/$\overline{GCS2}$ P1.3/$\overline{GCS3}$ P1.4/$\overline{GCS4}$ P1.5/$\overline{GCS5}$ P1.6/$\overline{GCS6}$ P1.7/$\overline{GCS7}$	O H(X)/H(1) R(1) P(X)/P(1)	These pins provide a multiplexed function. If enabled, each pin can provide a Generic Chip Select output which will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip Select, each pin may be used as a general purpose output Port. As an output port pin, the value of the pin can be read internally.
T0OUT T1OUT	O H(Q) R(1) P(Q)	Timer Output pins can be programmed to provide a single clock or continuous waveform generation, depending on the time mode selected.

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TABLE III. Pin descriptions - Continued.

Name	Type	Description
T0IN T1IN	I A(L) A(E)	Timer Input is used either as clock or control signals, depending on the timer mode selected.
INT0 INT1 INT4	I A(E,L)	Maskable Interrupt input will cause a vector to a specific type interrupt routine. To allow interrupt expansion. INT0 and/or INT1 can be used with INTA0 and INTA1 to interface with an external slave controller.
INT2/$\overline{\text{INTA0}}$ INT3/INTA1	I/O A(E,L) /H(1) R(Z) /P(1)	These pins provide a multiplexed function. As inputs, they provide a maskable interrupt that will cause the CPU to vector to a specific type interrupt routine. As outputs, each is programmatically controlled to provide an INTERRUPT ACKNOWLEDGE handshake signal to allow interrupt expansion.
P2.7 P2.6	I/O A(L) H(X) R(Z) P(X)	Bi-directional, open-drain Port pins.
$\overline{\text{CTS0}}$ P2.4/$\overline{\text{CTS1}}$	I A(L)	Clear-To-Send input is used to prevent the transmission of serial data on their respective TXD signal pin. $\overline{\text{CTS1}}$ is multiplexed with an input only port function.
TXD0 P2.1/TXD1	O H(X)/H(Q) R(1) P(X)/P(Q)	Transmit Data output provides serial data information. TXD1 is multiplexed with an output only Port function. During synchronous serial communications, TXD will function as a clock output.
RXD0 P2.0/RXD1	I/O A(L) R(Z) H(Q) P(X)	Receive Data input accepts serial data information. RXD1 is multiplexed with an input only Port function. During synchronous serial communications, RXD is bi-directional and will become an output for transmission or data (TXD becomes the clock).
P2.5/BCLK0 P2.2/BCLK1	I A(L)/A(E)	Baud Clock input can be used as an alternate clock source for each of the integrated serial channels. BCLKx is multiplexed with an input only Port function, and cannot exceed a clock rate greater than one-half the operating frequency of the M80C186EB.
P2.3/SINT1	O H(X)/H(Q) R(0) P(X)/P(Q)	Serial Interrupt output will go active to indicate serial channel 1 requires service. SINT1 is multiplexed with an output only Port function.

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6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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