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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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APPROVED BY: D.A. Cook

DRAWING APPROVAL DATE: 15 MARCH 1990

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, REMOTE TERMINAL INTERFACE WITH 1K X 16 RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89576

SHEET 1 OF 23

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1297-2

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89576	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT1553B RTR	Remote terminal interface with 1K X 16 RAM

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	P-BC, (68-pin, 1.135" x 1.135" x .345"), pin grid array package
Y	C-G5, (68-terminal, .960" x .960" x .135"), leaded chip carrier with unformed leads
Z	C-7, (68-terminal, .962" x .962" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range, (V_{DD})	-0.3 V dc minimum to +7.0 V dc maximum
DC input/dc output voltage range	-0.3 V dc minimum to +7.3 V dc maximum
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D)	300 mW 1/
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Latchup immunity (I_{LU})	±150 mA
Lead temperature(soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	5.5 V dc
Maximum low level input voltage (V_{IL})	0.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Operating frequency (F_O)	12 MHz

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard,and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$ $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
Low level input voltage	V_{IL}		1,2,3		0.8	V
High level input voltage	V_{IH}			2.0		
Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$		-1 110 -2000	1 2000 -110	µA
Low level output voltage	V_{OL}	$I_{OL} = 3.2$ mA			0.4	V
High level output voltage	V_{OH}	$I_{OH} = -400$ µA		2.4		
Three-state output leakage current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		-10	10	µA
Short-circuit output current 1/ 2/	I_{OS}	$V_{DD} = 5.5$ V, $V_O = V_{DD}$ $V_{DD} = 5.5$ V, $V_O = 0$ V		-90	90	mA
Quiescent current 3/	Q_{IDD}				1.5	
Average operating current 1/4/	I_{DD}	F = 12 MHz, $C_L = 50$ pF			50	
Input capacitance	C_{IN}	See 4.3.1.c	4		10	pF
Output capacitance	C_{OUT}				15	
Bidirectional I/O capacitance	C_{IO}				20	
Functional tests		See 4.3.1.d	7,8			

See footnotes at the end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{CTRL}$(H) set up wrt $\overline{CS}$(L) 5/	t_1	See figure 3 1/ Microprocessor RAM read cycle	9,10,11	10		ns
RD/$\overline{WR}$(H) set up wrt $\overline{CS}$(L)	t_2			10		
ADDR(9:0) valid to $\overline{CS}$(L) (address set up)	t_3			10		
$\overline{CS}$(L) to DATA(15:0) valid 5/	t_4				155	
$\overline{OE}$(L) to DATA(15:0) don't care (active)	t_5				65	
$\overline{CS}$(H) to $\overline{CTRL}$ don't care	t_6			0		
$\overline{CS}$(H) to ADDR(9:0) don't care	t_7			0		
$\overline{OE}$(H) to DATA(15:0) high impedance	t_8				40	
$\overline{CS}$(L) to $\overline{CS}$(H) 6/	t_9			220	5500	
$\overline{CS}$(H) to $\overline{CS}$(L)	t_{10}			85		
$\overline{CS}$(H) to RD/$\overline{WR}$ don't care	t_{11}			0		
$\overline{CS}$(H) to DATA(15:0) invalid 7/	t_{12}			25		
$\overline{OE}$(L) to $\overline{OE}$(H)	t_{13}			65		

See footnotes at the end of the table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{CTRL}$(H) set up wrt $\overline{CS}$(L)	t_1	See figure 3 1/ Microprocessor RAM write cycle	9,10,11	10		ns
RD/$\overline{WR}$(L) set up wrt $\overline{CS}$(L)	t_{14}			10		
ADDR(9:0) valid to $\overline{CS}$(L) (address set up)	t_3			10		
DATA(15:0) valid to $\overline{CS}$(L) (DATA set up)	t_{15}			0		
$\overline{OE}$(H) to DATA(15:0) high impedance	t_{16}			40		
$\overline{CS}$(H) to RD/$\overline{WR}$ don't care	t_{11}			0		
$\overline{CS}$(H) to ADDR(9:0) don't care	t_7			0		
$\overline{CS}$(H) to DATA(15:0) don't care	t_{17}			20		
$\overline{CS}$(L) to $\overline{CS}$(H) 6/	t_{18}			180	5500	
$\overline{CS}$(H) to $\overline{CS}$(L)	t_{10}			85		
$\overline{CS}$(H) to $\overline{CTRL}$ don't care	t_6			0		

See footnotes at the end of the table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{CTRL}$(L) set up wrt $\overline{CS}$(L)	t_{19}	See figure 3 1/ Control register write cycle	9,10,11	0		ns
RD/$\overline{WR}$(L) set up wrt $\overline{CS}$(L)	t_{20}			0		
$\overline{CS}$(L) to $\overline{CS}$(H) 6/	t_{21}			50	5500	
$\overline{CS}$(H) to DATA(15:0) don't care (hold time)	t_{22}			0		
$\overline{CS}$(H) to $\overline{CTRL}$ don't care	t_6			0		
$\overline{CS}$(H) to RD/$\overline{WR}$ don't care	t_{11}			0		
$\overline{OE}$(H) to DATA(15:0) high impedance	t_{23}			40		
DATA(15:0) valid to $\overline{CS}$(L) (DATA setup)	t_{15}			0		
$\overline{CTRL}$(L) set up wrt $\overline{CS}$ (L)	t_{19}	See figure 3 1/ Status register read cycle		0		
$\overline{CS}$(L) to $\overline{CS}$(H) 6/	t_{24}			65	5500	
RD/$\overline{WR}$(H) set up wrt $\overline{CS}$(L)	t_{25}			0		
$\overline{CS}$(L) to DATA(15:0) valid	t_{26}				65	
$\overline{CS}$(H) to $\overline{CTRL}$ don't care	t_{27}			5		
$\overline{CS}$(H) to RD/$\overline{WR}$ don't care	t_{28}			5		
$\overline{OE}$(L) to DATA(15:0) valid 5/ don't care(active)	t_5				65	
$\overline{OE}$(H) to DATA(15:0) high impedance	t_8				40	

See footnotes at the end of the table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{OE}$(L) to $\overline{OE}$(H)	t_{13}	See figure 3 1/ Status register read cycle	9,10,11	65		
$\overline{CS}$(L) to DATA(15:0) don't care	t_{29}			25		
VALMSG(H) before $\overline{TIMERON}$(L)	t_{30}	See figure 3 1/ RT failsafe timer signal relationships		0	35	ns
$\overline{TIMERON}$(L) before first biphase out zero(H)	t_{31}				1.2	µs
$\overline{TIMERON}$ low pulse width (time-out)	t_{32}			727.3	727.4	
$\overline{COMSTR}$(L) to $\overline{TIMERON}$(H)	t_{33}				25	ns
VALMSG(H) to ILLCOM(H) 8/	t_{34}				3.3	µs
$\overline{COMSTR}$(L) to ILLCOM(H) 9/	t_{35}				664	ns
$\overline{COMSTR}$(L) to ILLCOM(H) 9/	t_{35}				18.2	µs
ILLCOM(H) to ILLCOM(L) 10/	t_{36}			500		ns
12MHz(H) to $\overline{MC}$/SA valid	t_{37}	See figure 3 Status output timing		0	14	ns
Command word to $\overline{MC}$/SA Valid 1/ 11/	t_{38}			2.1	2.8	µs
12MHz(H) to $\overline{COMSTR}$(L)	t_{39}			0	17	ns
Command word to $\overline{COMSTR}$(L) 1/ 11/	t_{40}			3.2	3.7	µs
12MHz(H) to $\overline{BRDCST}$(L)	t_{41}			0	32	ns
Command word to $\overline{BRDCST}$(L) 1/ 11/	t_{42}			2.6	3.2	µs

See footnotes at the end of the table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le 125°C$ unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
12MHz(H) to T/$\overline{R}$ valid	t_{43}	See figure 3 Status output timing	9,10,11	0	57	ns
Command word to T/$\overline{R}$ valid 1/ 11/	t_{44}			2.2	2.7	µs
12MHz(H) to VALMSG(H)	t_{45}			0	32	ns
Command word to VALMSG(H) 1/ 11/ 12/	t_{46}			6.2	6.7	µs
12MHz(H) to MERR(H)	t_{47}			0	37	ns
$\overline{COMSTR}$(L) to $\overline{COMSTR}$(H) 1/	t_{48}			485	500	
12MHz(H) to RBUSY(H) 1/	t_{49}			0	37	
Command word to RBUSY(H) 1/	t_{50}			3.2	3.8	µs
12MHz(H) to $\overline{TERACT}$(L)	t_{51}			0	37	ns
Command word to $\overline{TERACT}$(L) 1/ 11/	t_{52}			3.1	3.7	µs
12MHz(H) to RTRT(H)	t_{53}			0	32	ns
Command word to RTRT(H) 1/ 11/	t_{54}			21.0	22.0	µs
$\overline{MRST}$(L) to $\overline{MRST}$(H) 1/	t_{55}			500		ns
RBUSY(H) to RBUSY(L) (2.7 µs) 1/ 6/ (5.7 µs)	t_{56}				5.5 8.5	µs
RBUSY(L) to RBUSY(H) (2.7 µs) 1/ 6/ (5.7 µs)	t_{57}			3.10 240		µs ns

See footnotes at the end of table.

1/ Guaranteed to the limits specified in table I, if not tested

2/ Not more than one output may be shorted at a time for a maximum duration of one second.

3/ All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

4/ Includes current input pull-ups. Instantaneous surge currents on the order of 1.0 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.

5/ "wrt" defined as "with respect to".

6/ The maximum amount of time that $\overline{CS}$ can be held low is 5500 ns if the user has selected the 5.7 µs RBUSY option. For the 2.7 µs RBUSY option, the maximum $\overline{CS}$ low time is 2500 ns.

7/ Assumes $\overline{OE}$ is asserted.

8/ The ILLCOM pin must be asserted within 3.3 µs after VALMSG goes to a logic 1 if the RTR is to respond with the message error bit of the status word at a logic 1.

9/ If the illegal command is mode code 2, 4, 5, 6, 7 or 18, the ILLCOM pin must be asserted within 664 ns after command strobe ($\overline{COMSTR}$) transitions to logic 0. Asserting the ILLCOM pin within the 664 ns inhibits the mode code function.
For an illegal receive command, the ILLCOM pin is asserted within 18.2 µs after the $\overline{COMSTR}$ transitions to a logic 0 in order to suppress data words from being stored. In addition, the ILLCOM pin must be at a logic 1 throughout the reception of the message until VALMSG is asserted. This does not apply to illegal transmit commands since the status word is transmitted first.

10/ For transmit command illegalization.

11/ Command word measured from mid-bit crossing.

12/ Receive last data word to Valid Message active (VALMSG(H)).
Transmit command word to Valid Message active (VALMSG(H)).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	MCSA1	C11	DATA14	J10	DATA3
A3	MCSA2	D1	ADDR7	J11	DATA4
A4	MCSA4	D2	ADDR8	K1	RD/$\overline{WR}$
A5	MERR	D10	DATA11	K2	$\overline{CS}$
A6	$\overline{TERACT}$	D11	DATA12	K3	$\overline{MRST}$
A7	$\overline{BRDCST}$	E1	V_{DD}	K4	RTA3
A8	2MHZ	E2	ADDR6	K5	RTA1
A9	TBZ	E10	DATA9	K6	RTPTY
A10	TAZ	E11	DATA10	K7	RBO
B1	$\overline{MC}$/SA	F1	ADDR5	K8	RAO
B2	MCSAO	F2	V_{SS}	K9	ILLCOM
B3	MCSA3	F10	V_{DD}	K10	DATA1
B4	T/$\overline{R}$	F11	DATA8	K11	DATA2
B5	TXERR	G1	ADDR3	L2	12MHZ
B6	$\overline{TIMERON}$	G2	ADDR4	L3	RTA4
B7	RTRT	G10	DATA7	L4	RTA2
B8	$\overline{COMSTR}$	G11	V_{SS}	L5	RTAO
B9	TBO	H1	ADDR1	L6	RBZ
B10	TAO	H2	ADDR2	L7	RAZ
B11	DATA15	H10	DATA5	L8	VALMSG
C1	ADDR9	H11	DATA6	L9	$\overline{OE}$
C2	RBUSY	J1	$\overline{CTRL}$	L10	DATAO
C10	DATA13	J2	ADDRO		

FIGURE 1. Terminal connections.

Device type	01				
Case outlines	Y and Z				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
01	V_{SS}	24	ILLCOM	47	TBZ
02	ADDR5	25	$\overline{OE}$	48	$\overline{COMSTR}$
03	ADDR4	26	DATA0	49	2MHZ
04	ADDR3	27	DATA1	50	RTRT
05	ADDR2	28	DATA2	51	$\overline{BRDCST}$
06	ADDR1	29	DATA3	52	$\overline{TIMERON}$
07	ADDR0	30	DATA4	53	$\overline{TERACT}$
08	$\overline{CTRL}$	31	DATA5	54	TXERR
09	RD/$\overline{WR}$	32	DATA6	55	MERR
10	$\overline{CS}$	33	DATA7	56	T/$\overline{R}$
11	12MHZ	34	V_{SS}	57	MCSA4
12	$\overline{MRST}$	35	V_{DD}	58	MCSA3
13	RTA4	36	DATA8	59	MCSA2
14	RTA3	37	DATA9	60	MCSA1
15	RTA2	38	DATA10	61	MCSA0
16	RTA1	39	DATA11	62	$\overline{MC}$/SA
17	RTA0	40	DATA12	63	RBUSY
18	RTPTY	41	DATA13	64	ADDR9
19	RBZ	42	DATA14	65	ADDR8
20	RB0	43	DATA15	66	ADDR7
21	RAZ	44	TA0	67	ADDR6
22	RA0	45	TAZ	68	V_{DD}
23	VALMSG	46	TB0		

FIGURE 1. Terminal connections - Continued.

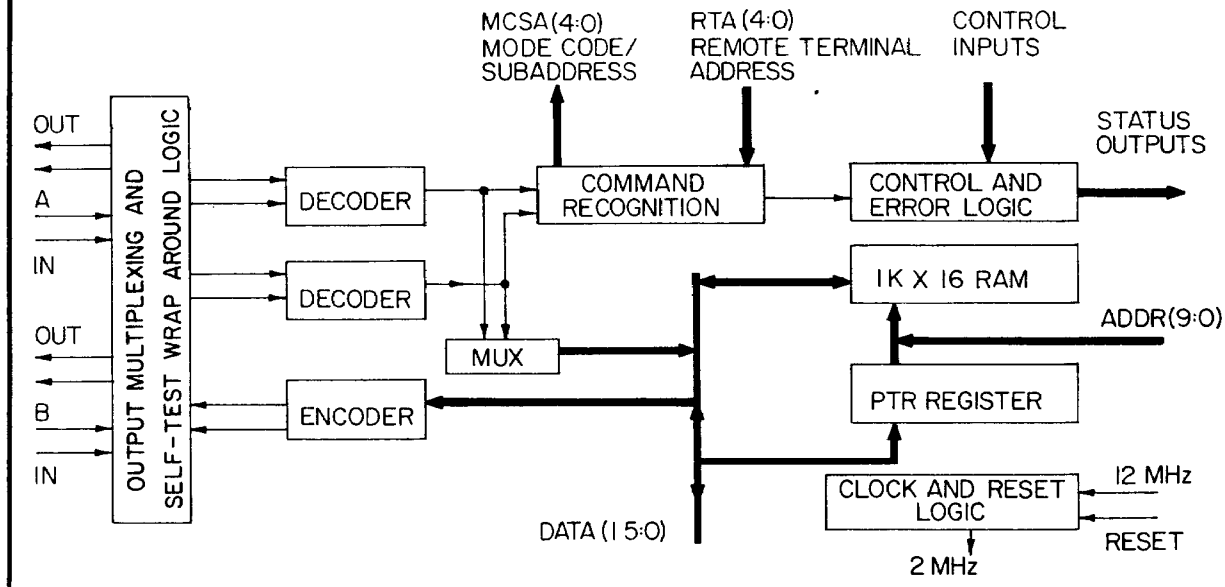

FIGURE 2. Functional block diagram.

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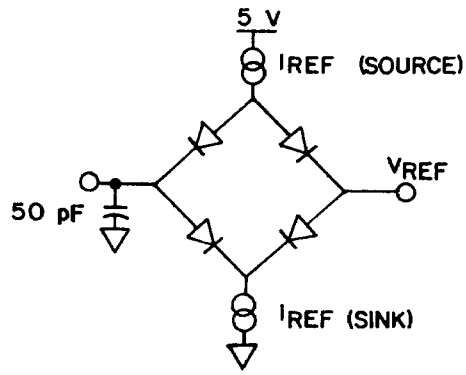
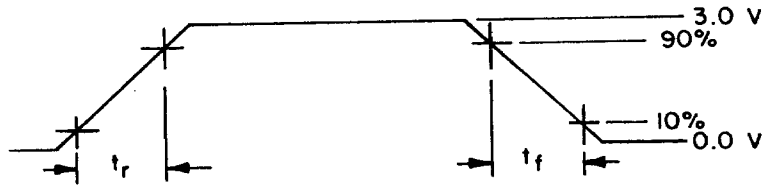


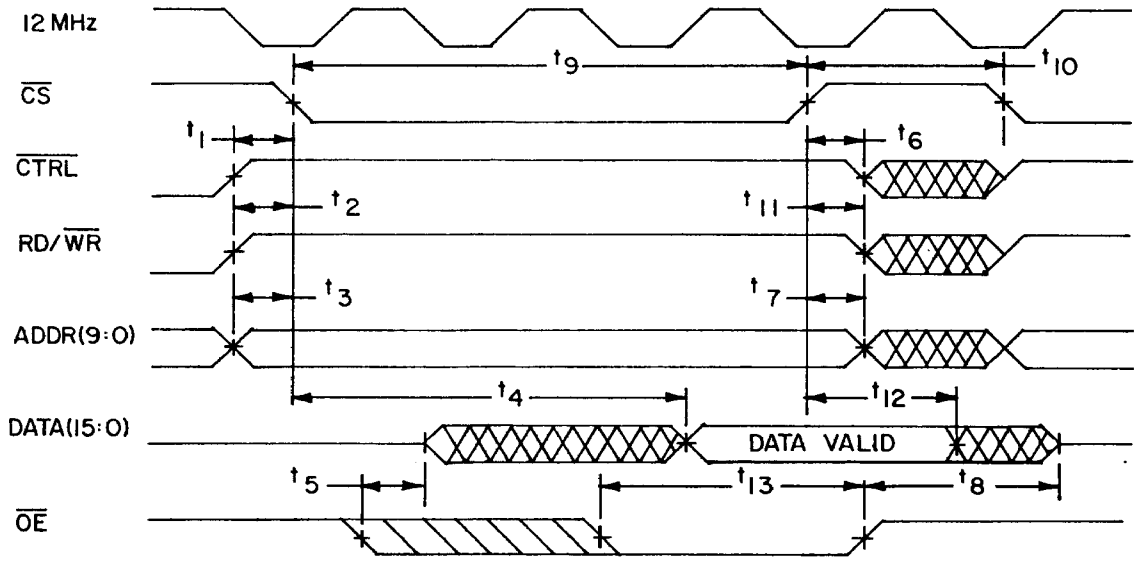
NOTE: 50 pF including scope probe and test socket,
$V_{REF} = (V_{OL}$ maximum + V_{OH} minimum)/2



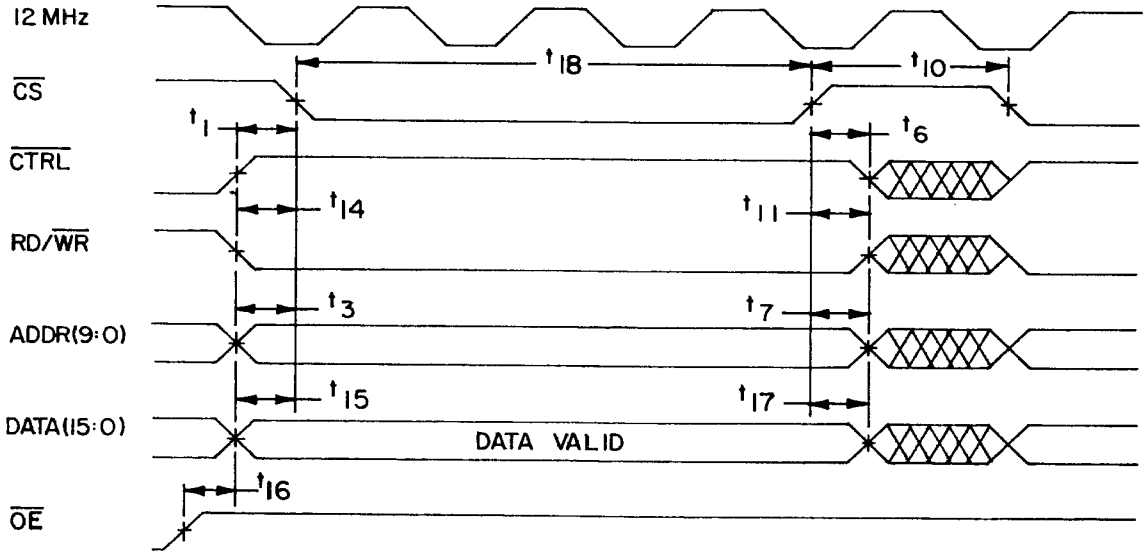
Input pulses

NOTE: $t_r = t_f < 2$ ns

FIGURE 3. Switching test circuit and waveforms.

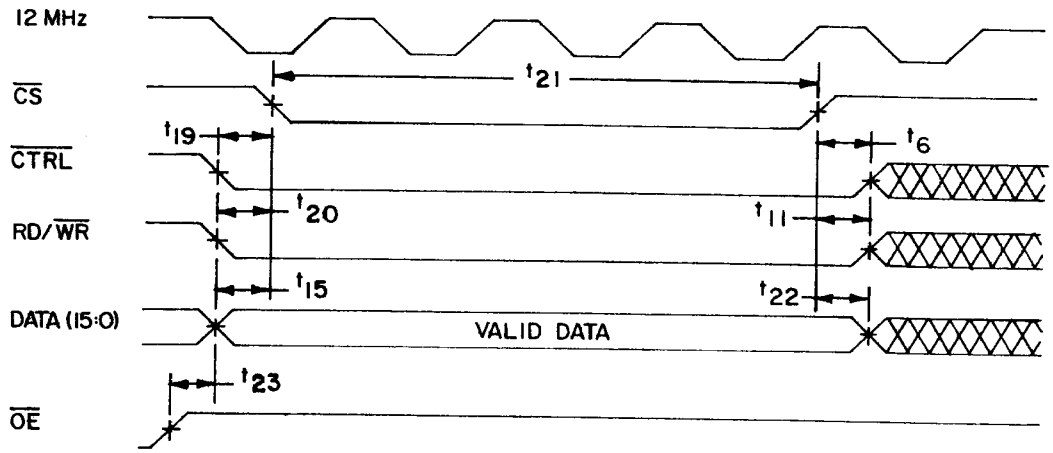


Microprocessor RAM read

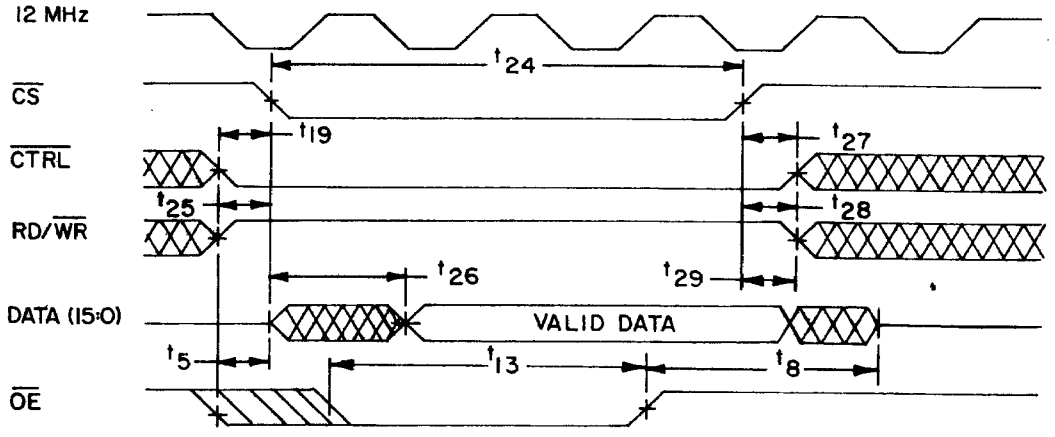


Microprocessor RAM write

FIGURE 3. Switching test circuit and waveforms - Continued.



Control register write



Status register read

FIGURE 3. Switching test circuit and waveforms - Continued.

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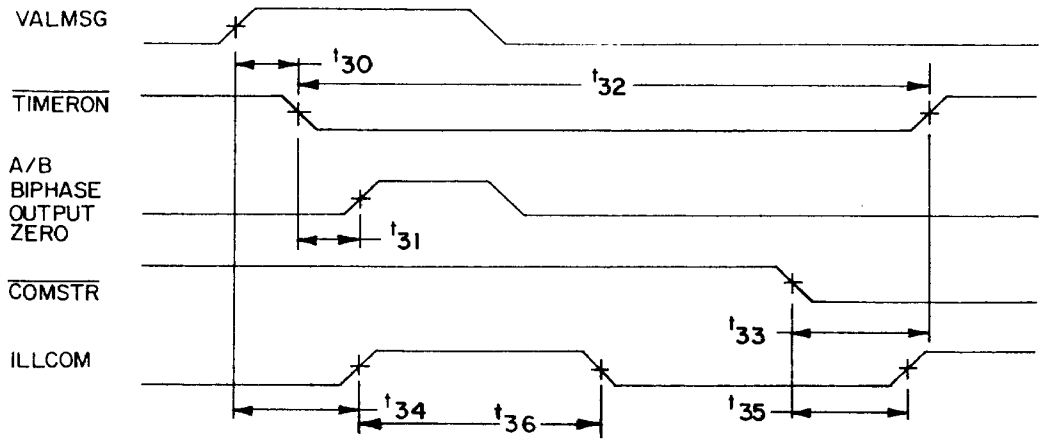
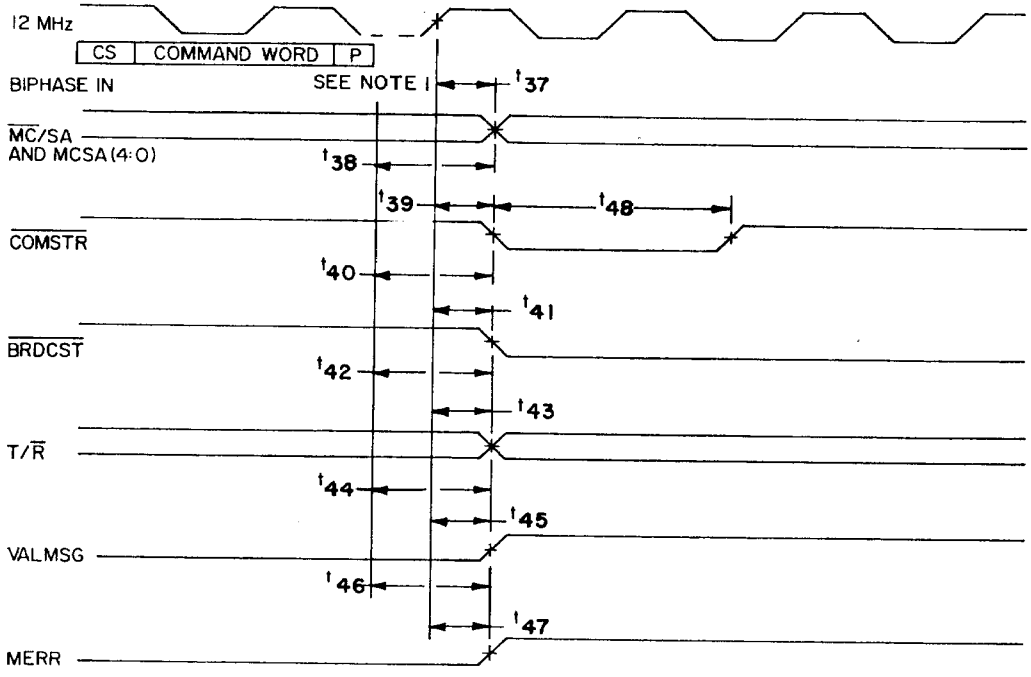


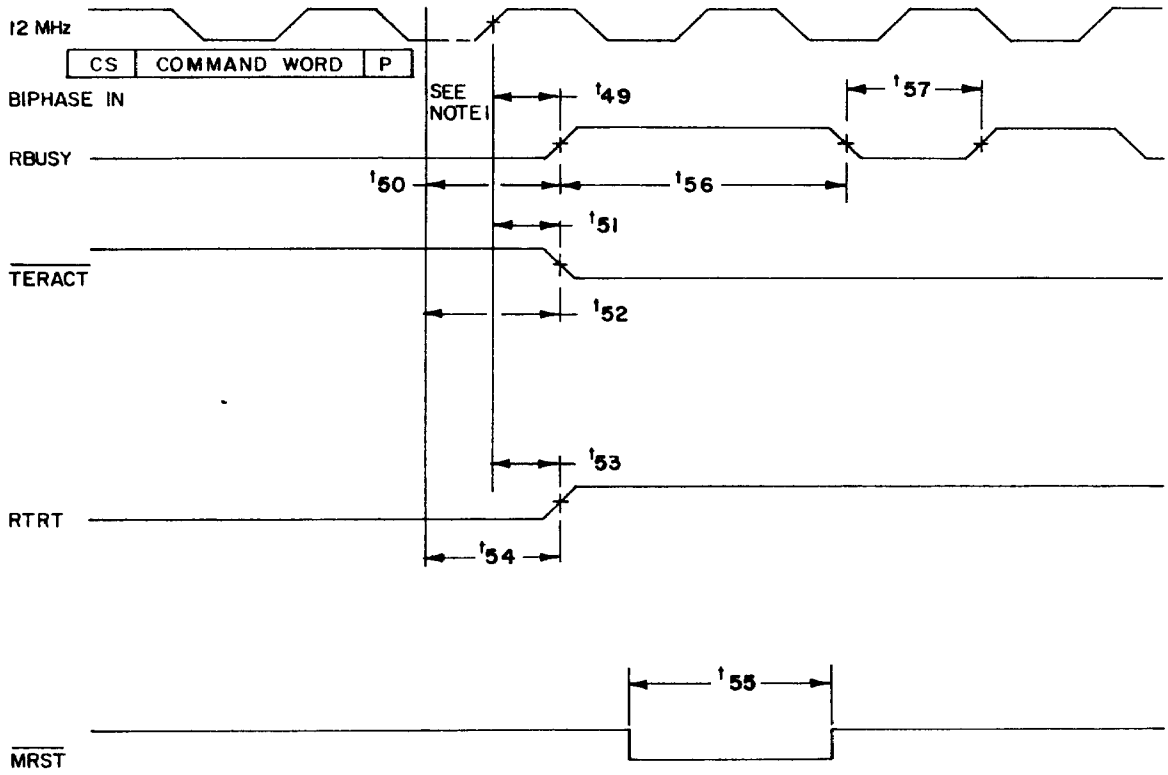
RT fail-safe timer signal relationships



NOTE: Measured from the mid-bit parity crossing.

Status output timing

FIGURE 3. Switching test circuit and waveforms - Continued.



NOTE: Measured from mid-bit parity crossing.

Status output timing

FIGURE 3. Switching test circuit and waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 or table IV, method 5010 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 or method 5010 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 or table IV method 5010 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, C_{IO}) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 10 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendor/s test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I or 5010, table IV
Interim electrical parameters (method 5004 or 5010)	---
Final electrical test parameters (method 5004 or 5010)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005 or 5010)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005 or 5010)	1, 2, 7, 8A

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.6 Pin descriptions.

Name	Type	Active	Description
DATA(15)	TTB		Bit 15(MSB) of the bidirectional data bus
DATA(14)	TTB		Bit 14 of the bidirectional data bus
DATA(13)	TTB		Bit 13 of the bidirectional data bus
DATA(12)	TTB		Bit 12 of the bidirectional data bus
DATA(11)	TTB		Bit 11 of the bidirectional data bus
DATA(10)	TTB		Bit 10 of the bidirectional data bus
DATA(9)	TTB		Bit 9 of the bidirectional data bus
DATA(8)	TTB		Bit 8 of the bidirectional data bus
DATA(7)	TTB		Bit 7 of the bidirectional data bus
DATA(6)	TTB		Bit 6 of the bidirectional data bus
DATA(5)	TTB		Bit 5 of the bidirectional data bus
DATA(4)	TTB		Bit 4 of the bidirectional data bus
DATA(3)	TTB		Bit 3 of the bidirectional data bus
DATA(2)	TTB		Bit 2 of the bidirectional data bus
DATA(1)	TTB		Bit 1 of the bidirectional data bus
DATA(0)	TTB		Bit 0 (LSB) of the bidirectional data bus
ADDR(9)	TI		Bit 9 (MSB) of the address bus
ADDR(8)	TI		Bit 8 of the address bus
ADDR(7)	TI		Bit 7 of the address bus
ADDR(6)	TI		Bit 6 of the address bus
ADDR(5)	TI		Bit 5 of the address bus
ADDR(4)	TI		Bit 4 of the address bus
ADDR(3)	TI		Bit 3 of the address bus
ADDR(2)	TI		Bit 2 of the address bus
ADDR(1)	TI		Bit 1 of the address bus
ADDR(0)	TI		Bit 0 (LSB) of the address bus
$\overline{CS}$	TI	AL	Chip select
RD/$\overline{WR}$	TI		Read/write
$\overline{CTRL}$	TI	AL	Control
$\overline{OE}$	TI	AL	Output enable
$\overline{BRDCST}$ 1*	TO	AL	Broadcast
T/$\overline{R}$ 0*	TO		Transmit/receive
RTRT 0*	TO	AH	Remote terminal to remote terminal
VALMSG 0*	TO	AH	Valid message
RBUSY 0*	TO	AH	RTR busy
ILLCOM	TDI	AH	Illegal command
MERR 0*	TO	AH	Message error
TXERR 0*	TO	AH	Transmission error
$\overline{TIMERON}$ 1*	TO	AL	Fail-safe timer
$\overline{COMSTR}$ 1*	TO	AL	Command strobe
$\overline{TERACT}$ 1*	TO	AL	Terminal active
$\overline{MC/SA}$ 0*	TO		Mode code/subaddress indicator
MCSA0 0*	TO		Mode code/subaddress output 0
MCSA1 0*	TO		Mode code/subaddress output 1
MCSA2 0*	TO		Mode code/subaddress output 2
MCSA3 0*	TO		Mode code/subaddress output 3
MCSA4 0*	TO		Mode code/subaddress output 4

6.6 Pin descriptions - continued

Name	Type	Active	Description
RTA4	TUI		Remote terminal address bit 4 (MSB)
RTA3	TUI		Remote terminal address bit 3
RTA2	TUI		Remote terminal address bit 2
RTA1	TUI		Remote terminal address bit 1
RTA0	TUI		Remote terminal address bit 0 (LSB)
RTPTY	TUI		Remote terminal address parity
RAZ	TI		Receiver-channel A, zero input
RA0	TI		Receiver-channel A, one input
RBZ	TI		Receiver-channel B, zero input
RB0	TI		Receiver-channel B, one input
TAZ 0*	TO		Transmitter-channel A, zero output
TA0 0*	TO		Transmitter-channel A, one output
TBZ 0*	TO		Transmitter-channel B, zero output
TB0 0*	TO		Transmitter-channel B, one output
$\overline{MRST}$	TUI	AL	Master reset
12MHz	TI		12 MHz input clock
2MHz	TO		2 MHz output clock
V_{DD}	PWR		+5 V dc power
	PWR		+5 V dc power
V_{SS}	GND		Reference ground
	GND		Reference ground

NOTES:
TI = TTL Input
TUI = TTL Input (pull-up)
TDI = TTL Input (pull-down)
TO = TTL Output
TTO = Three-state TTL Output
TTB = Three-state TTL Bidirectional
AH = Active high
AL = Active low
* = Values marked with asterisks indicate the initialized values of these bits.

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6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8957601XX	65342	UT1553B RTR G
5962-8957601YX	65342	UT1553B RTR W
5962-8957601ZX	65342	UT1553B RTR A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	United Technologies Microelectronics Center 1575 Garden of the Gods Colorado Springs, Colorado 80907

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