SONY

CXB1561Q-Y

s3R-IC for Optical Fiber Cimmunication Receiver

Description

The CXB1561Q-Y achieves the 3R optical-fiber cimmunication receiver functions (Reshaping, Regenerating and Retiming) on a single chip using with a SAW filter.

Features

- 3R-IC with a built-in post-amplifier (SAW filter system)
- Signal interruption alarm output
- Data shutdown function for signal interruption
- Timing phase can be fine adjusted
- Delay length for edge detector (differentiator) can be selected
- Single 5V power supply

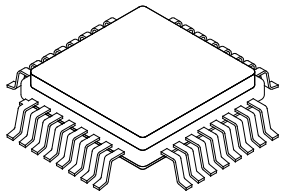
Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +7.0	V
• Operating case temperature	T_C	–55 to +125	°C
• Storage temperature	Tstg	–65 to +150	°C
• Output current (surge current)	Io	0 to 50 (100)	mA
• D/D input current	IID	–200 to +400	µA
• SC/SC input current	IIC	–100 to +400	µA
• S1/S2 input voltage	VIS	V_{CC} to V_{EE} + 1.2	V

Recommended Operating Conditions

• Supply voltage	$V_{CC} - V_{EE}$	5.0 ± 0.5	V
• Operating case temperature	T_C	–40 to +85	°C

32 pin QFP (Ceramic)



Structure

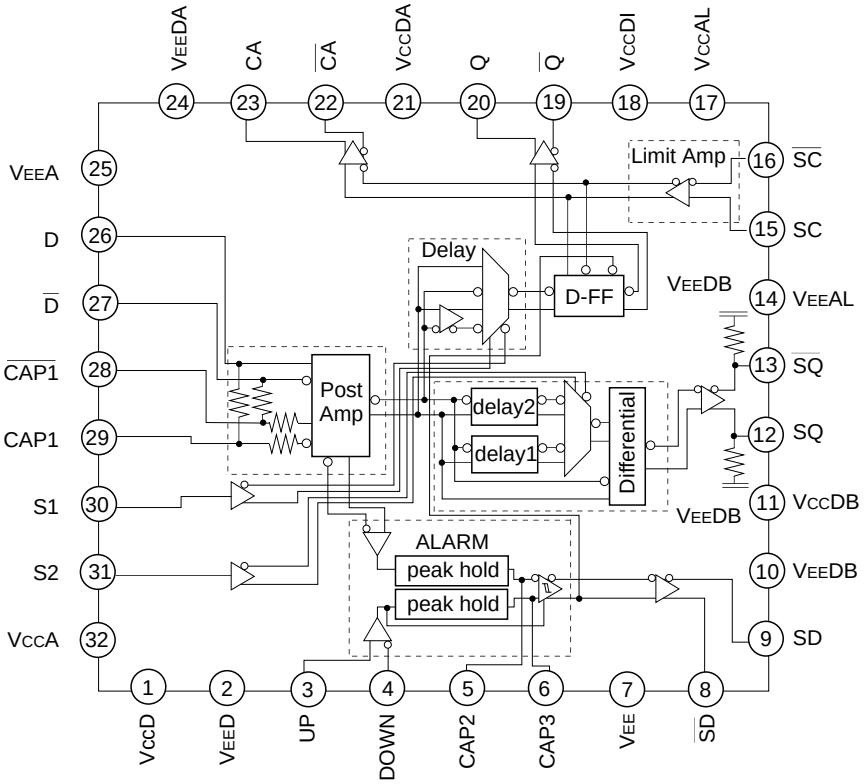
Bipolar silicon monolithic IC

Applications

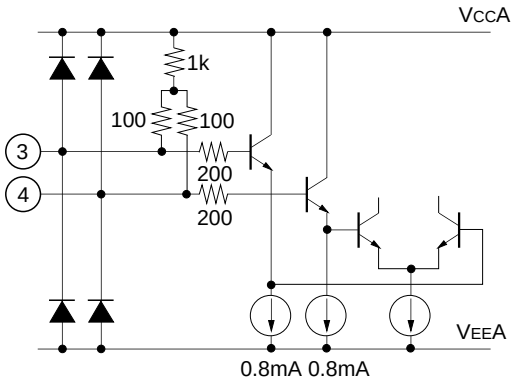
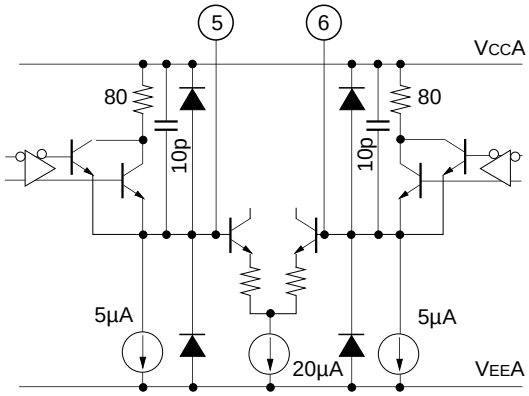
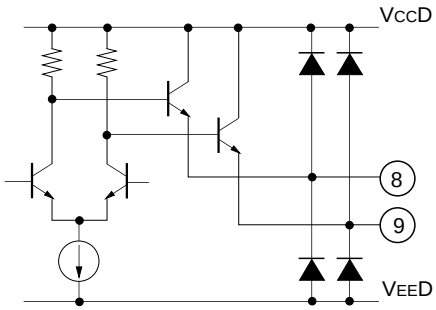
- SONET: 622.08Mbps, 155.52Mbps
- Fiber channel: 531.25Mbps, 265.625Mbp
- Clock multiplication: X2, X4

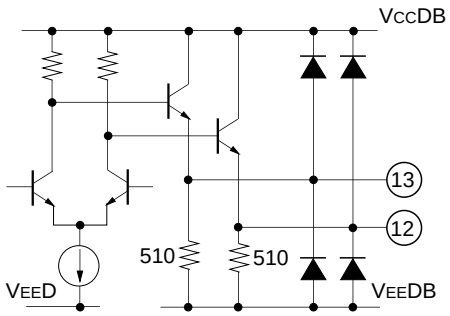
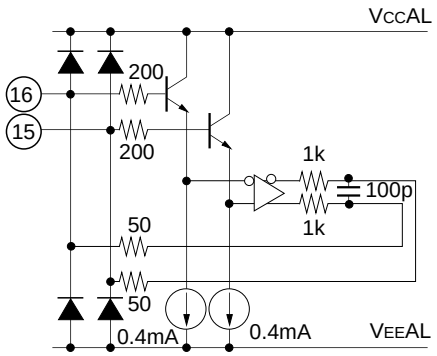
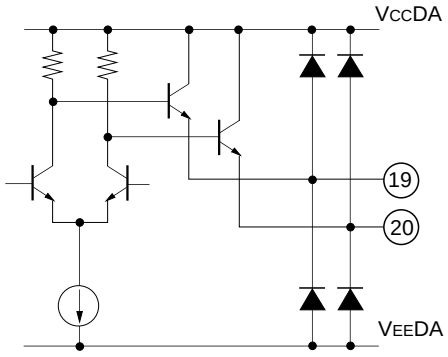
E93615B6Z

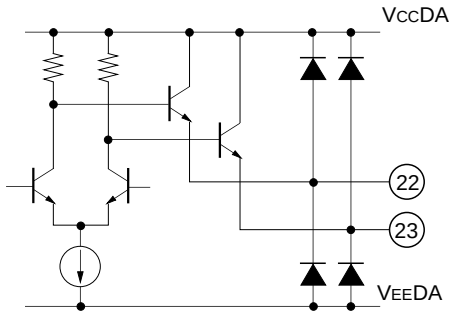
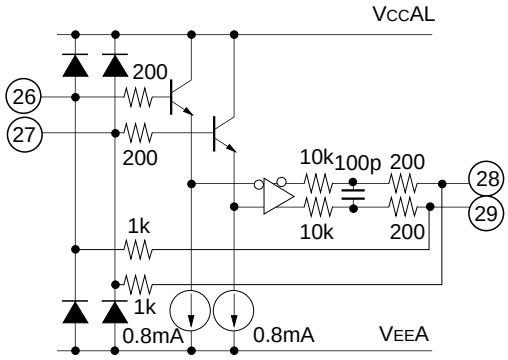
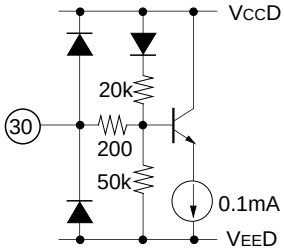
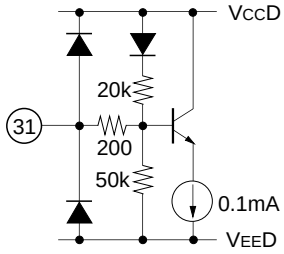
Block Diagram



Pin Description

Pin No.	Symbol	Typical pin voltage DC	Typical pin voltage AC	Equivalent circuit	Description
1	VccD	0V			Positive power supply pin for digital block.
2	VEED	–5V			Negative power supply pin for digital block.
3	UP	–1.3V			Resistor connection pins for alarm level setting. UP pin: When the resistance connection to this pin is increased, the alarm level becomes higher. DOWN pin: When the resistance connected to this pin is increased, the alarm level becomes lower.
4	DOWN	–1.3V			
5	CAP2	–1.8V			Capacitance connection pins for alarm block peak hold circuit. (Each pin incorporates a capacitance of approximately 10pF.) CAP2 pin: Peak hold capacitance connection pin for the post-amplifier signal output. CAP3 pin: Peak hold capacitance connection pin for the alarm level setting block.
6	CAP3	–1.8V			
7	VEE	–5V			Negative power supply pin.
8	$\overline{SD}$		–0.9V to –1.7V		Alarm output pins. Terminate these pins in 510Ω at VEE.
9	SD		–0.9V to –1.7V		
10	VEEDB	–5V			Negative power supply pin for differential circuit.
11	VccDB	0V			Positive power supply pin for differential circuit.

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
12	SQ		–0.9V to –1.7V		Differential output pins.
13	$\overline{SQ}$		–0.9V to –1.7V		
14	VEEAL	–5V			Negative power supply pin for limiter amplifier.
15	SC	–1.3V	–0.9V to –1.7V		Limiter amplifier input pins. Ensure that these inputs are AC-coupled.
16	$\overline{SC}$	–1.3V	–0.9V to –1.7V		
17	VccAL	0V			Positive power supply pin for limiter amplifier.
18	VccDI	0V			Positive power supply pin for internal digital circuit.
19	$\overline{Q}$		–0.9V to –1.7V		Data signal output pins. Terminate these pins in 50Ω at VTT = –2V.
20	Q		–0.9V to –1.7V		
21	VccDA	0V			Positive power supply pin for output circuit.

Pin No.	Symbol	Typical pin voltage		Equivalent circuit	Description
		DC	AC		
22	$\overline{CA}$	—	–0.9V to –1.7V		Clock signal output pins. Terminate these pins in 50Ω at VTT = –2V
23	CA	—	–0.9V to –1.7V		
24	VEEDA	–5V			Negative power supply pin for output circuit.
25	VEEA	–5V			Negative power supply pin for analog block.
26	D	–1.3V	–0.9V to –1.7V		Post-amplifier input pins. Ensure that these inputs are AC-coupled.
27	$\overline{D}$	–1.3V	–0.9V to –1.7V		
28	$\overline{CAP1}$				Capacitance connection pins to determine the high cut-off frequency for post-amplifier feedback.
29	CAP1				
30	S1	–2.0V			Delay switchover input pin for delay block. ΔT = T (S1: High) – T (S1: open Low) = 134ps (typ. target)
31	S2	–2.0V			Pulse width switchover input pin for differential circuit. S2: open low For 622Mbps S2: High For 155Mbps
32	VccA	0V			Positive power supply pin for analog block.

Electrical Characteristics

• DC characteristics (Vcc = 0V, V_{EE} = –5V ± 10%, Tc = –40 to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I_{EE}		–157	–110	–74	mA
CA/$\overline{CA}$, Q/$\overline{Q}$ High output voltage	V_{OH}-Vcc	Termination: Rt = 50Ω, V_{TT} = –2V*1	–1.03		–0.88	V
		Termination: Rt = 50Ω, V_{TT} = –2V	–1.15		–0.88	
CA/$\overline{CA}$, Q/$\overline{Q}$ Low output voltage	V_{OL}-Vcc	Termination: Rt = 50Ω, V_{TT} = –2V*1	–1.81		–1.62	
		Termination: Rt = 50Ω, V_{TT} = –2V	–1.86		–1.60	
SD/$\overline{SD}$ High output voltage	V_{OH}a-Vcc	Termination: Rt = 510Ω, to V_{EE}*1	–1.08		–0.82	
		Termination: Rt = 510Ω, to V_{EE}	–1.20		–0.83	
SD/$\overline{SD}$ Low output voltage	V_{OL}a-Vcc	Termination: Rt = 510Ω, to V_{EE}*1	–1.90		–1.57	
		Termination: Rt = 510Ω, to V_{EE}	–1.95		–1.55	
S1/S2 High input voltage	V_{IH}-Vcc		–1.17		0	
S1/S2 Low input voltage	V_{IL}-Vcc		–3.00		–1.47	
S1/S2 High input current	I_{IH}				150	µA
S1/S2 Low input current	I_{IL}		–90			

*1 V_{EE} = –5V, Tc = 0 to 85°C

• AC characteristics (Vcc = 0V, V_{EE} = –5V ± 10%, V_{TT} = –2V, Tc = –40 to 85°C)

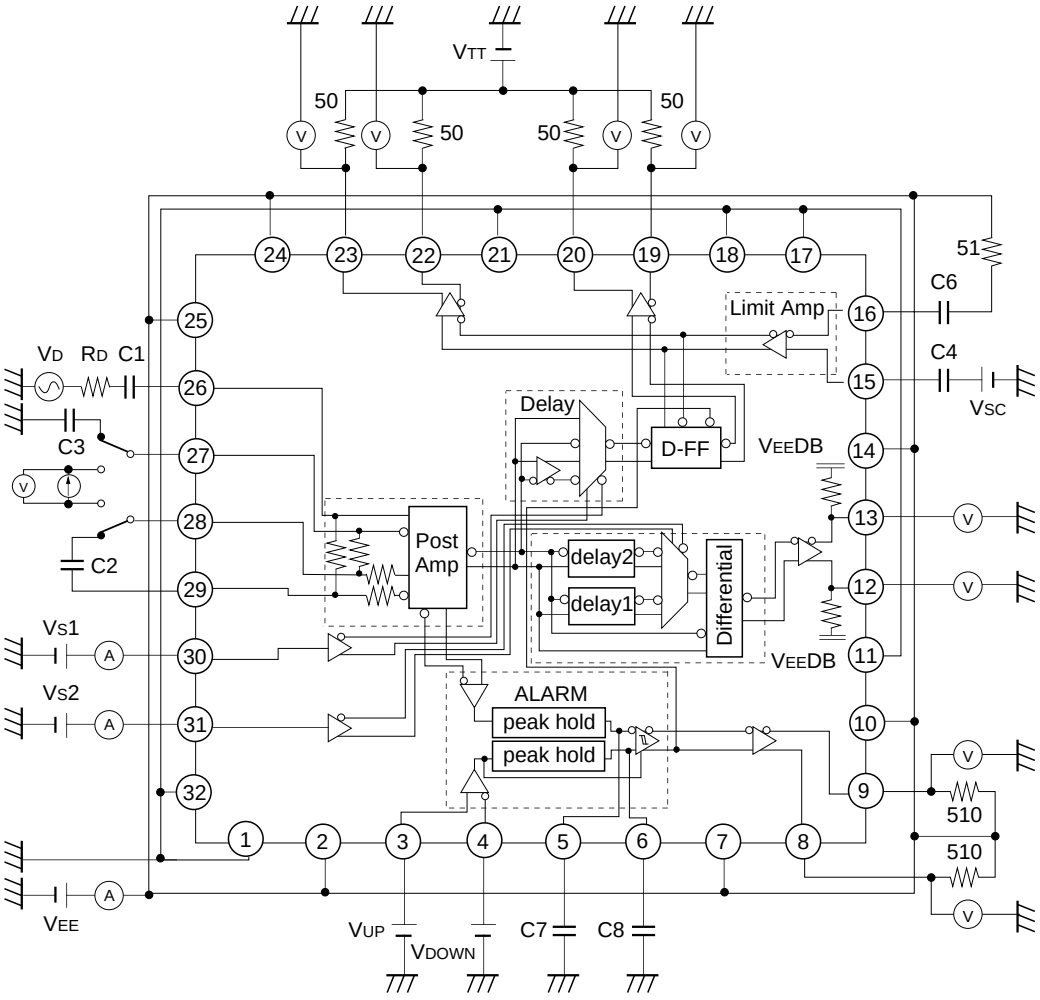
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data rate	Da	S2: open low	414.72	622.08		Mbps
	Db	S2: High	155.52	311.04		
D/$\overline{D}$ input resistance	RINM		750	1000	1250	Ω
D/$\overline{D}$ input identification max. voltage	VmaxM	For single-end input, DC cut-off	1000			mVp-p
Post Amp Gain	GP	Internal signal: 400mV	45			dB
SQ output pulse width	τd1	S2: open low	525	760	1075	ps
	τd2	S2: High	1050	1625	2150	
SQ output amplitude	VoB	Output, DC cut-off, 50Ω load	480	670	850	mV
SQ rise time	TrB	50Ω load, 20% to 80%	200	300	420	ps
SQ fall time	TfB		200	300	400	
SC/$\overline{SC}$ input resistance	RinL		37.5	50	62.5	Ω
SC/$\overline{SC}$ input identification max voltage	VinL	For single-end input, DC cut-off	1000			mVp-p
Limit Amp Gain	GL	Internal signal: 400mV	30			dB
Phase margin for the flip-flop block	Δθ		320	340		deg
Q/$\overline{Q}$ rise time	TrQ	50Ω load, 20% to 80%	200	440	650	ps
Q/$\overline{Q}$ fall time	TfQ		200	410	650	
CA/$\overline{CA}$ rise time	TrC		150	245	350	
CA/$\overline{CA}$ fall time	TfC		120	215	350	
CA/CA output duty cycle	Du		45	50	55	%

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Identification maximum voltage amplitude of alarm level	VmaxA	D·single-phase input conversion	30			mVp-p
Hysteresis width	ΔP	*2	2	6	12	dB
SD/$\overline{SD}$ response assert time	Tas	Low → High*2			100	µs
SD/$\overline{SD}$ response deassert time	Tdas	High → Low*2	2.5		100	

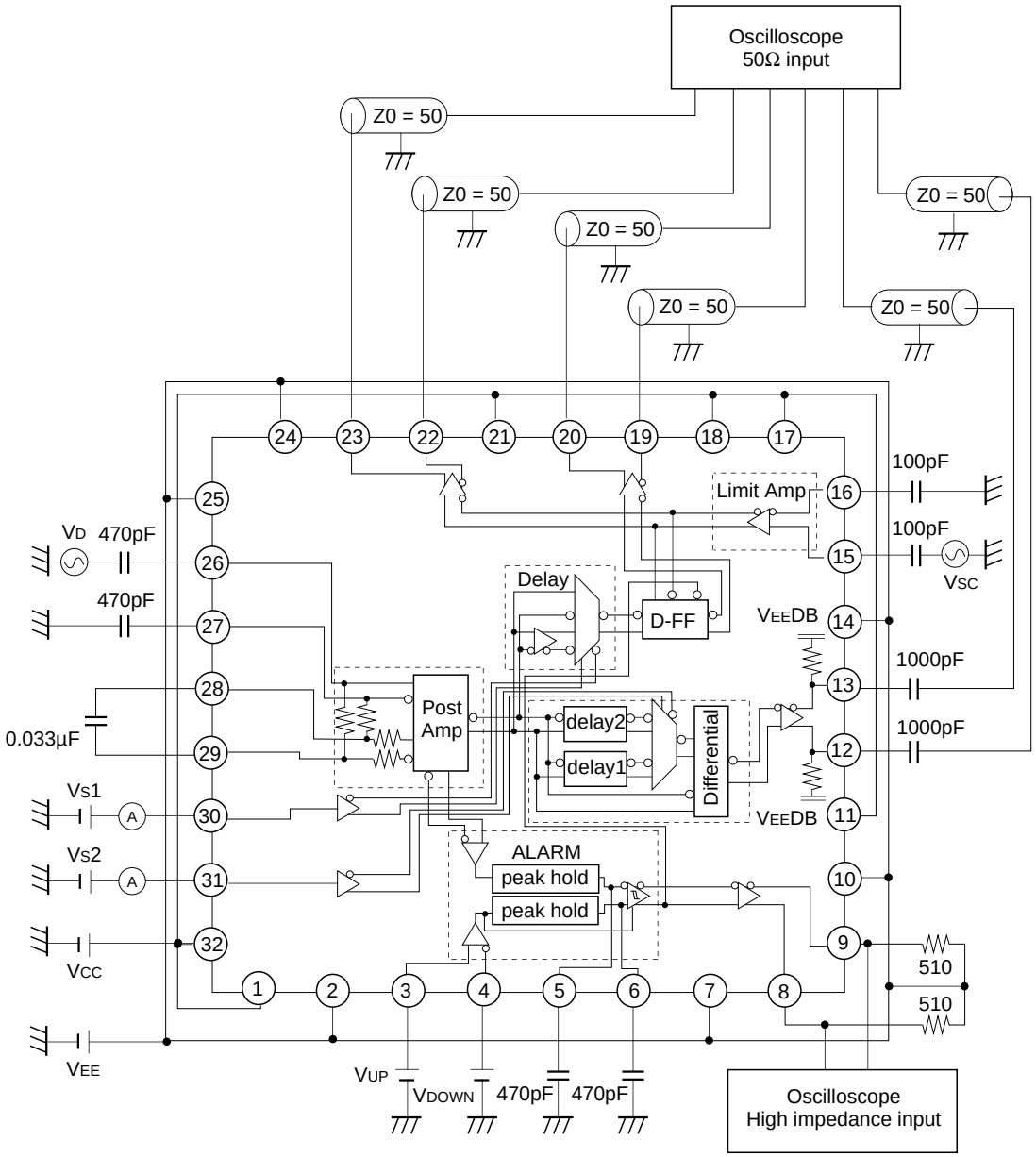
*2 CAP2/CAP3 pin capacitance 470pF, V (UP pin) – V (DOWN pin) = 10mV, D input voltage = 130mVp-p

Electrical Characteristics Measurement Circuit

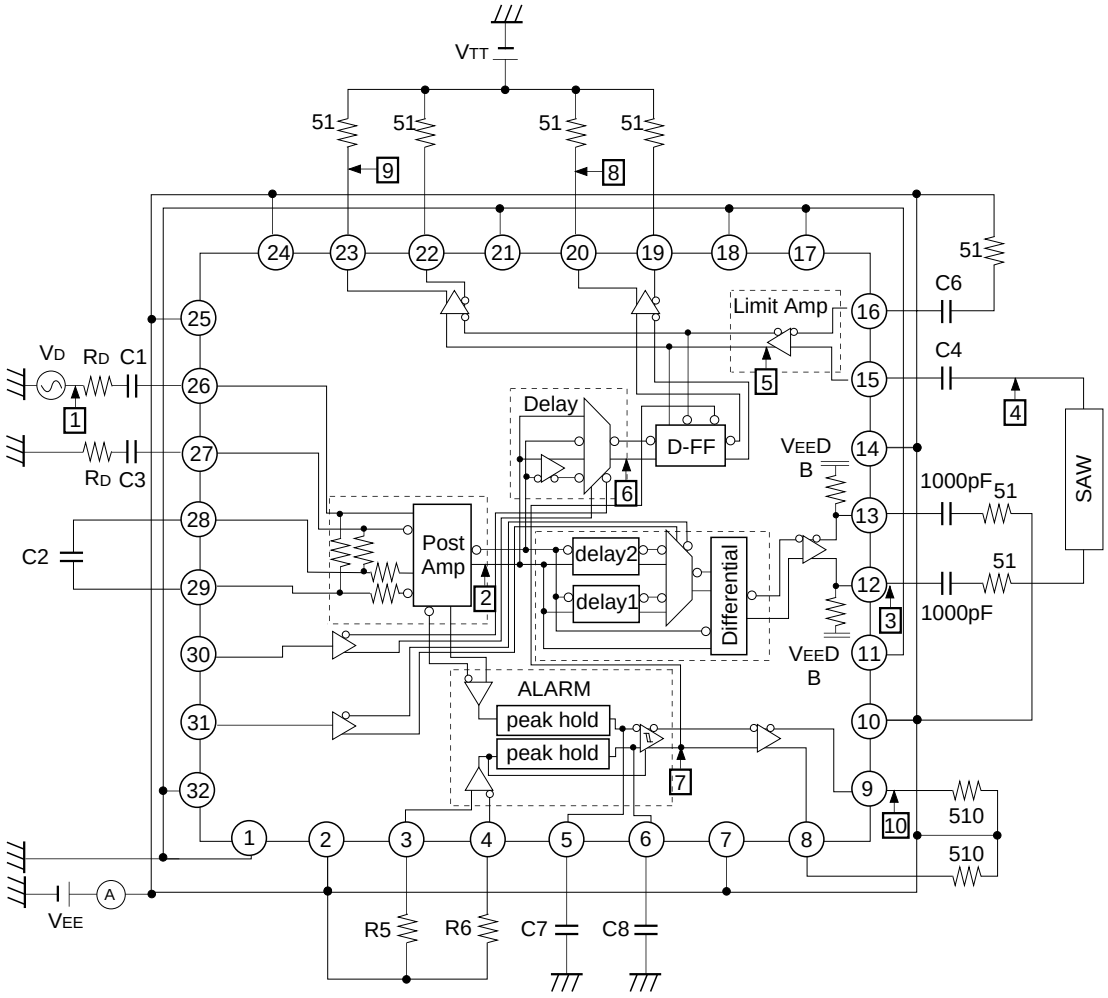
For DC Characteristics



For AC Characteristics



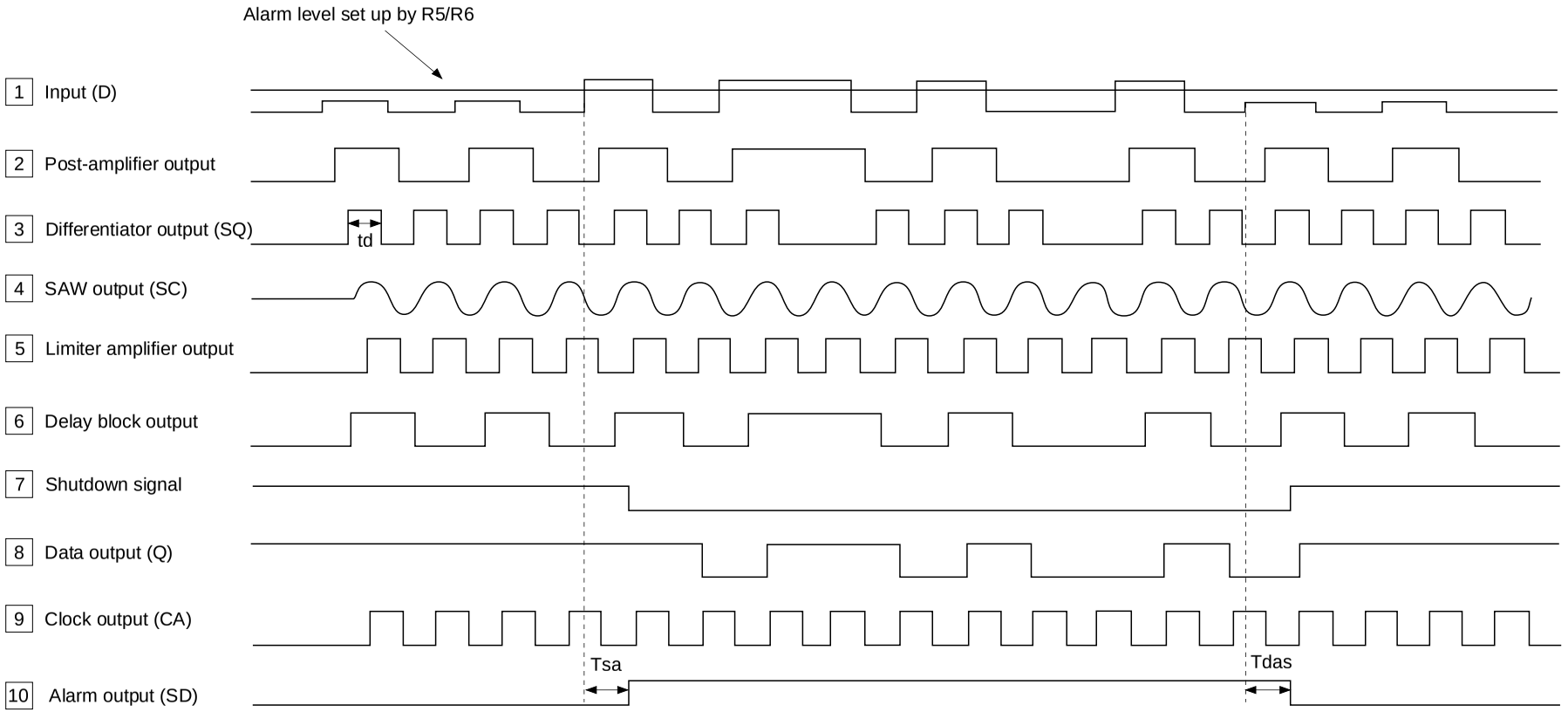
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Timing Chart

Sectional waveforms of the Application circuit



Alarm Block Logic

Optical signal input status	SD	$\overline{SD}$	Q
Signal input	High level	Low level	—
Signal interruption	Low level	High level	Fixed at High level

Only the data (Q. $\overline{Q}$), not clock, is shut down for signal interruption.

Description of Operation

1. Overall operations

The structure of optical-fiber communication receiver system is shown in Fig. 1. The CXB1561Q-Y performs the 3R operations indicated below.

- Photodiode .....Converts a data optical signal to a current signal.
- Pre Amp.....Converts a data current signal to a voltage signal (however, the voltage level is feeble).
- 3R .....1) Amplifies a feeble data voltage signal (Reshaping).
  2) Outputs a data signal in sync with a clock signal (Retiming).
  3) Outputs both data and clock signals as ECL level signals (Regenerating).

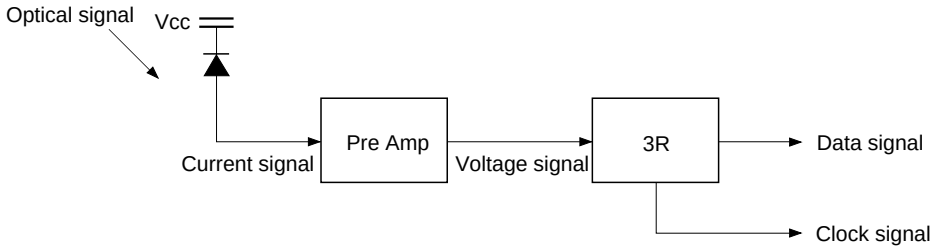


Fig. 1. Optical fiber communication receiver system clock

The signal flow of the CXB1561Q-Y, including the SAW filter, is as shown in Fig. 2. First, the feeble signal output of the pre-amplifier enters the post-amplifier and is amplified to an IC internal logic level. The amplified signal is then divided into the clock and data sides shown below. The clock side derives a clock signal from a data signal. First, the post-amplifier signal enters the differentiator, which generates a pulse output having an uniform width at the signal rise and fall times. This output pulse enters the SAW filter, which generates resonance at regular intervals and outputs a SIN wave having a resonance frequency. This signal output then enters the limiter amplifier and is amplified to an IC internal logic level. This amplified signal is used as the D-FF block clock signal. In the data side, on the other hand, the post-amplifier signal enters the delay section, where the signal is delayed to accomplish data/clock synchronization at the D-FF block. The signals separated into the clock and data sides are therefore synchronized with each other at the D-FF block and output to the outside.

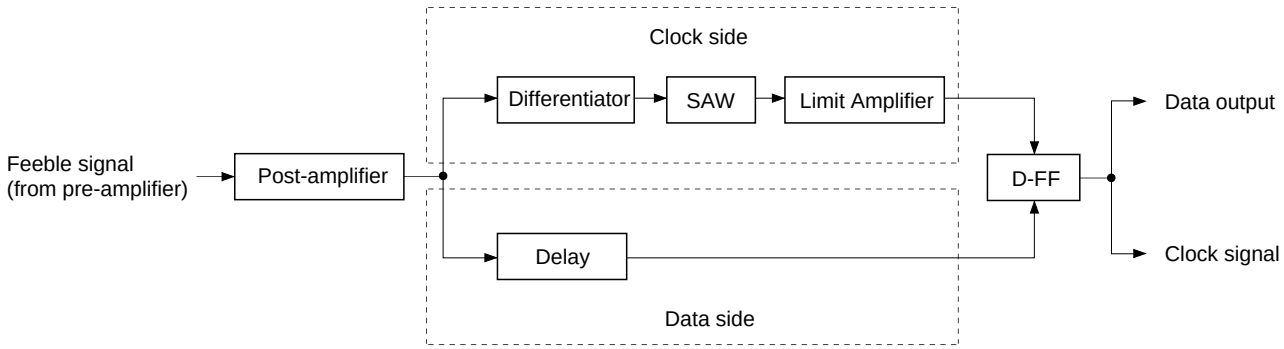


Fig. 2. Signal flow

2. Delay length selection for edge detector (differentiator) (S2 pin operations)

The larger the resonance frequency (SAW filter) component in the input signal, the greater the SAW filter output. Therefore, the CXB1561Q-Y is designed to offer differing differentiator pulse widths in the 622.08Mbps and 155.52Mbps of the SONET. The pulse width varies as follows according to the S2 pin input.

S2: open Low → For 622.08Mbps, 531.25Mbps
S2: High → For 155.52Mbps, 265.625Mbps

3. Timing phase fine adjustment (S1 pin operations)

As explained under overall operations, the data signal delay is adjusted by the delay block to synchronize the clock and data signals at the D-FF block. However, as the clock signal is output to the outside when it passes through the SAW filter, the clock delay varies with the SAW filter type and on-board wiring length. To compensate for such a clock external delay variations more or less, the delay provided by the data delay section can be varied by switching S1 pin input. The delay change ΔT is set up as follows.

ΔT = T (S1: open Low) – T (S1: High) = 134ps (design target value)

The above indicates that the delay provided by the data delay block is ΔT greater when S1 is open Low than when S1 is High.

4. Alarm output and data shutdown functions

When the input signal level is lower than the alarm setting level, the CXB1561Q-Y generates an alarm signal and forcibly places the data output on a High level. For alarm level identification, a comparator having a hysteresis function is used to prevent misoperations of alarm output. The hysteresis width is designed so that the gain is always maintained constant (design target value: 6dB) without regard to the alarm setting level.

The alarm level setting is determined by the voltage difference between Pins 3 (UP) and 4 (DOWN).
Therefore, a desired voltage should be generated between the UP and DOWN pins and that the UP pin voltage is higher than the DOWN pin voltage.

Notes of Operation

1. Post-amplifier block

In the post-amplifier block, the DC bias is automatically fed back by capacitors C1 and C2 as shown in Fig. 3. So, input with the DC cut-off. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 for post-amplifier, and external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the lower frequency of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 values so as to avoid the occurrence of peaking characteristics. The R1 and R2 target values and C1 and C2 typical values are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 27 to capacitor C3 that has the same capacitance as capacitor C1.
As this circuit is designed for mark density 1/2.,it is not recommended to use for mark density substantially different from 1/2.

R1 (internal) → 1kΩ
C1 (external) → 470pF
→ f2 → 340kHz

R2 (internal) → 10kΩ
C2 (external) → 0.033uF
→ f1 → 480Hz

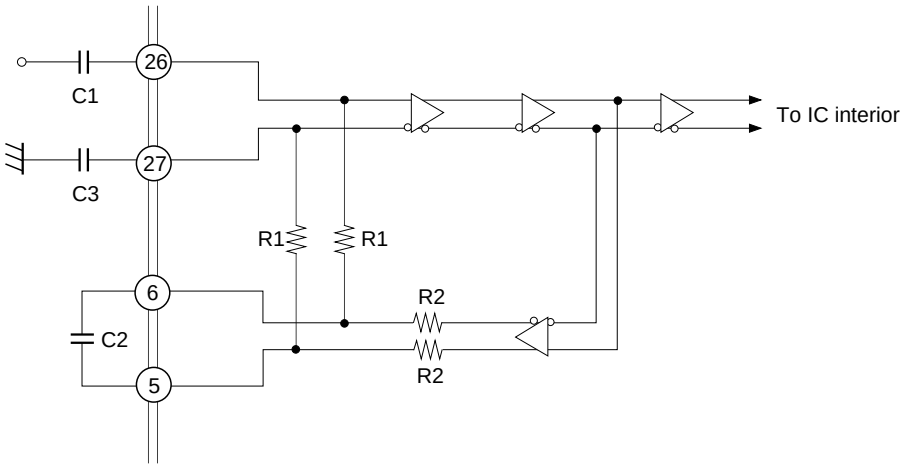


Fig. 3.

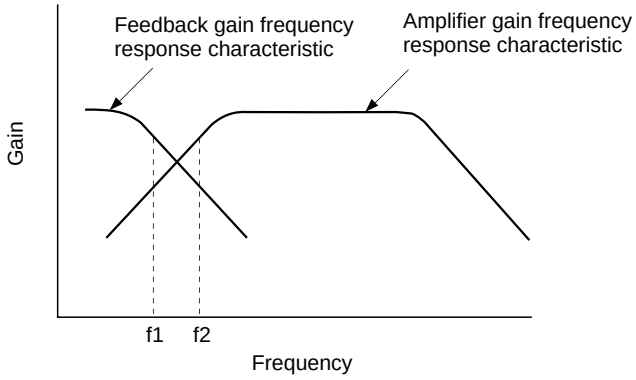


Fig. 4.

2. Limiter amplifier block

In the limiter amplifier block, the DC bias is automatically fed back by capacitor C4 and IC internal capacitor C5 as shown in Fig. 5. So, input with the DC cut-off. As is the case with the post-amplifier, external capacitor C4 and IC internal resistor R3 determine the low input cut-off frequency f2 of limiter amplifier. Further, IC internal capacitor C5 and IC internal resistor R4 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the lower frequency of the amplifier gain characteristics depending on the f1/f2 combination, set the C4 value so as to avoid the occurrence of peaking characteristics. The R3, R4, and C5 target values and C4 typical value are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 16 to capacitor C6 that has the same capacitance as capacitor C4.

R3 (internal) → 50Ω
C4 (external) → 100pF
→ f2 → 32MHz

R4 (internal) → 1kΩ
C5 (internal) → 100pF
→ f1 → 1.6MHz

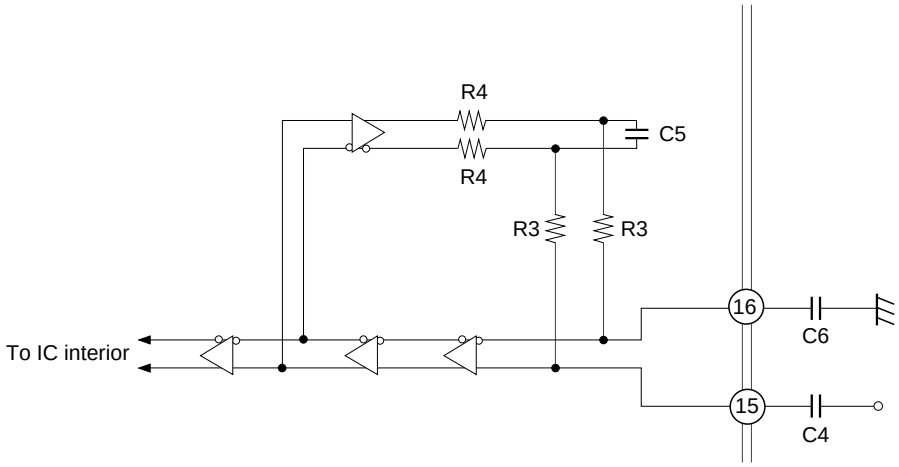


Fig. 5.

3. Alarm block

As shown in Fig. 6, the alarm block requires alarm level setting external resistors R5 and R6 and peak hold capacitors C7 and C8. When the resistance value provided for resistor R5 is increased, the alarm setting level rises. When the resistance value provided for resistor R6 is increased, the alarm setting level lowers. However, the voltage of Pin 3 should be higher than the voltage of Pin 4. For the alarm level setting, see Fig. 7. In the relationship between the alarm setting level and hysteresis width, the hysteresis width maintains a constant gain (design target value: 6dB) as shown in Fig. 8. External capacitors C7 and C8 are used for input signal and alarm level peak hold capacitance. The C7 and C8 capacitance values should be set so as to obtain desired assert time and deassert time settings for the alarm signal. The additional resistances R10 and R11 make deassert time smaller. The R5, R6, C7, and C8 typical values are as indicated below. (A capacitance of approximately 10pF is built in Pins 5 and 6 respectively.)

R5 → 5k + αΩ
R6 → 5kΩ
C7, 8 → 470pF

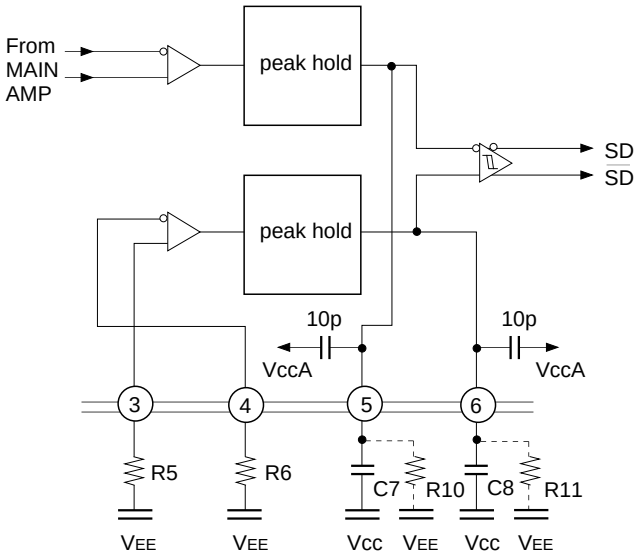
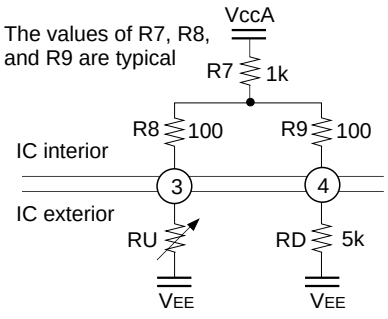


Fig. 6.



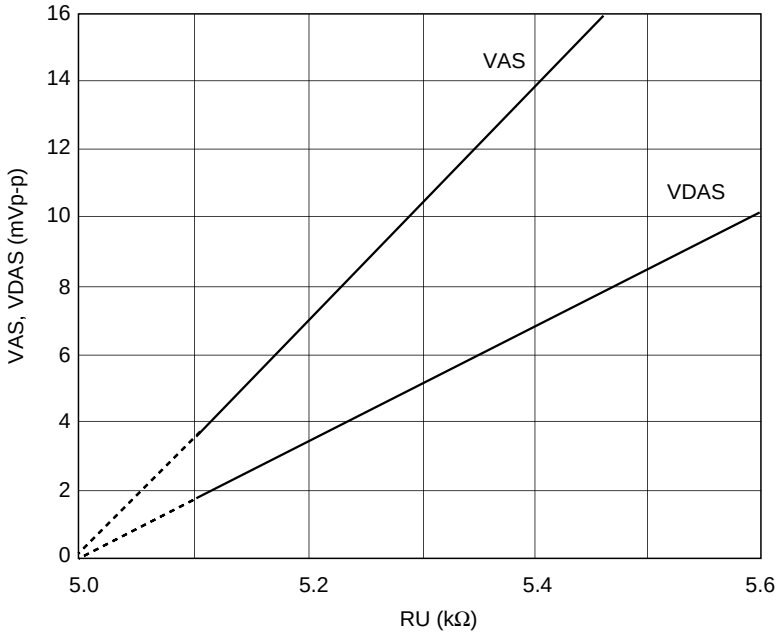


Fig. 7.

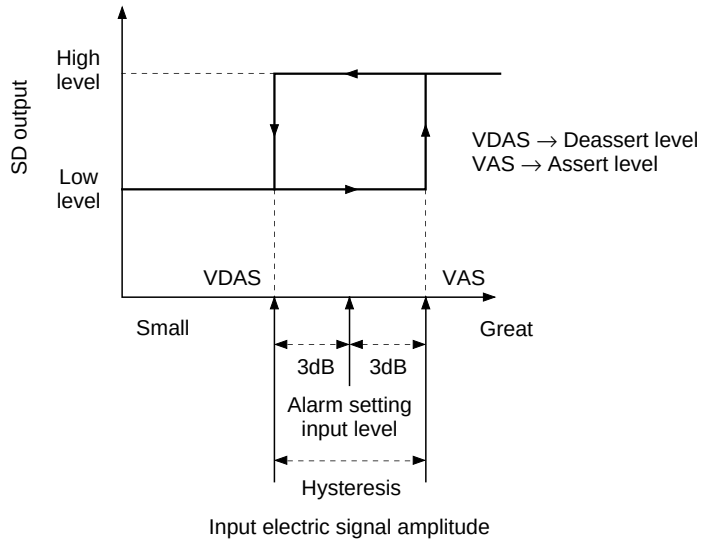


Fig. 8.

4. SAW peripheral board design

In the signal flow from the differentiator through the SAW filter to the limiter amplifier, the signal is output to the outside at the SAW filter. To assure proper timing in the IC, therefore, the board wiring length must be appropriately designed. For the data and clock timing adjustment at the D-FF in the IC, the Typ. state position must conform to Fig. 9 because the D-FF phase margin is the greatest when the clock is positioned at the center of data. Further, the Min. state must comply with the D-FF setup time, and the Max. state must conform to the D-FF hold time. Since the clock signal occurs at regular intervals, synchronization must be accomplished at least at a certain integer multiple of the clock period. The above timing setup is derived from the equation below. The board wiring must therefore be designed to satisfy the equation.

T = T (SAW filter delay time) + T (wiring delay time)
{+ T (delay time for the IC which amplifies the SAW filter output when it is feeble)}

(1) Typical value
Construction shown in Fig. 10-a): T(typ.) = (n + 3/4) ∗ Tsaw – Tsdc (typ.)
Construction shown in Fig. 10-b): T(typ.) = (n + 1/4) ∗ Tsaw – Tsdc (typ.)

(2) Minimum value
T (min.) > T (typ.) + Tsff – 1/2 ∗ Tsaw + (Tsdc (typ.) – Tsdc (min.))

(3) Maximum value
T (max.) < T (typ.) – Thff + 1/2 ∗ Tsaw + (Tsdc (typ.) – Tsdc (max.))

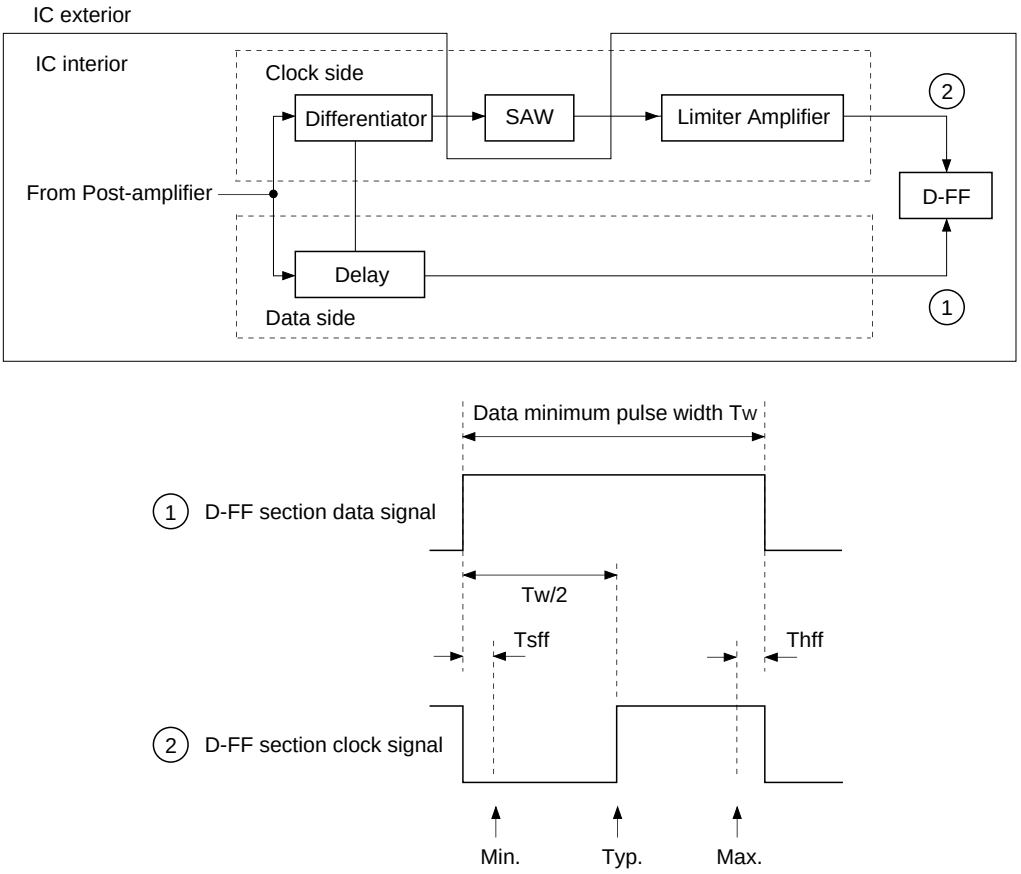


Fig. 9. D-FF timing

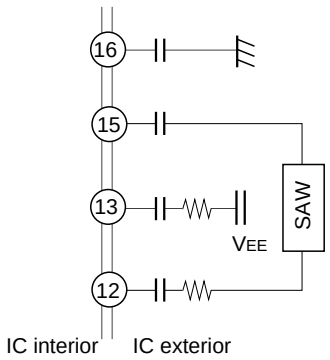


Fig. 10-a)

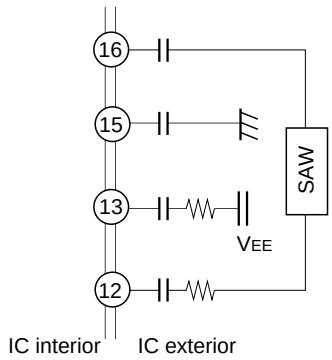


Fig. 10-b)

For the constants in the equation on the preceding page, see the table below.

n = integer (0,1,2, · · ·)
Tsaw = SAW resonance frequency cycle

622.08Mbps → Tsdc = Tsdc1
155.52Mbps → Tsdc = Tsdc2

S2 pin: open Low → T'sdc = Tsdc
S2 pin: High → T'sdc = Tsdc – ΔT

(Vcc = 0V, V_{EE} = –5V ± 10%, Tc = 0 to 85°C)

Item		Symbol	Min.	Typ.	Max.	Unit
Time difference for timing	622.08Mbps	Tsdc1	613	747	929	ps
	155.52Mbps	Tsdc2	822	1050	1549	
Variable delay time		ΔT	100	134	163	
D-FF setup time		Tsff	70			
D-FF hold time		Thff	100			

When, for instance, the standard board wiring length is calculated for a data rate of 622Mbps, the following result is obtained.

Tsaw = 1607.5ps
Assuming the absolute phase of SAW filter = –10deg;
Board wiring delay time → 5.85ps/mm
Construction → Fig. 10-a)
n = 0

Under the above conditions, the following results.

T (typ.) = (n+3/4) ∗ Tsaw – Tsdc (typ.) = (0 + 3/4) ∗ 1607.5 – 747 = 458.6ps
T wiring length (typ.) = T (typ.) – TSAW filter = 458.6 – 1607.5 ∗ (10/360) = 413.9ps
Wiring length (typ.) = T wiring length (typ)/(board wiring delay time) = 413.9/5.85 = 70.8mm

5. Order of power ON

The CXB1561Q-Y has a number of power supplies. Note that the IC may break down if the following power-ON order is not observed (no problem occurs when all the power supplies are turned ON simultaneously).

(1) When all Vcc power supplies are turned ON first
(The V_{CC}A, V_{CC}AL, V_{CC}D, V_{CC}DA, and V_{CC}DB may be turned in any order.)
Turn ON the V_{EE} power supplies in any order.

(2) When all VEE power supplies are turned ON first
(The V_{EE}, V_{EE}A, V_{EE}AL, V_{EE}D, V_{EE}DA, and V_{EE}DB may be turned in any order.)
Turn ON the V_{CC}AL, V_{CC}DA, and VccDB (in any order) → the V_{CC}D → V_{CC}A.

6. Differential Output Waveform

The DC cut-off capacitance is connected between the differential output block and SAW filter as shown in Fig. 11 so that the waveforms are varied according to the ratio of the High level and Low level for the output waveform as shown in Fig. 12. So, note that the waveforms are different for SQ and $\overline{SQ}$.

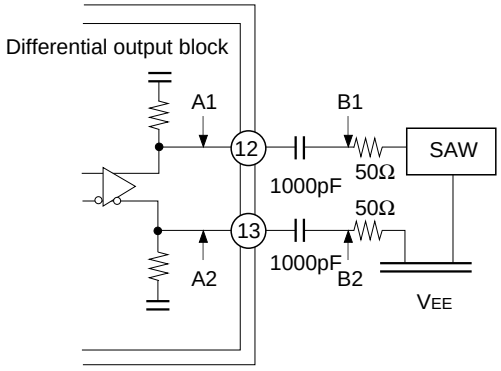


Fig. 11.

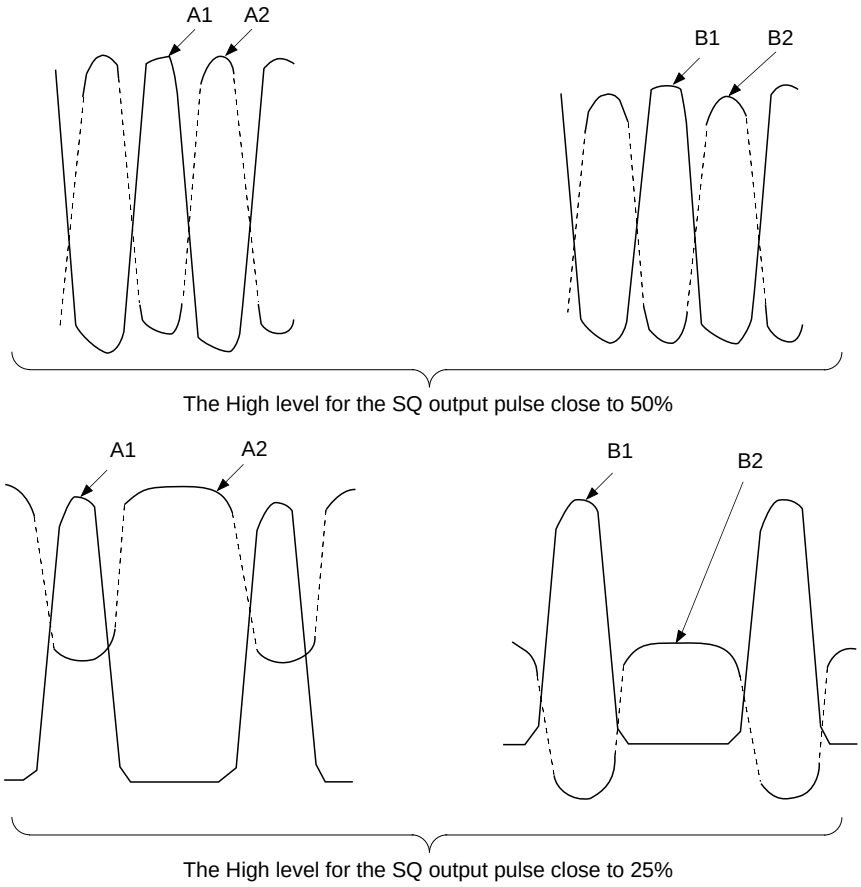


Fig. 12.

7. Evaluation Board

Saw peripheral board design is important for system performance. Fig.13 shows Evaluation board for 622.08Mbps and the characteristics of the test circuit (Fig.14) is shown in Fig.15 to 18.

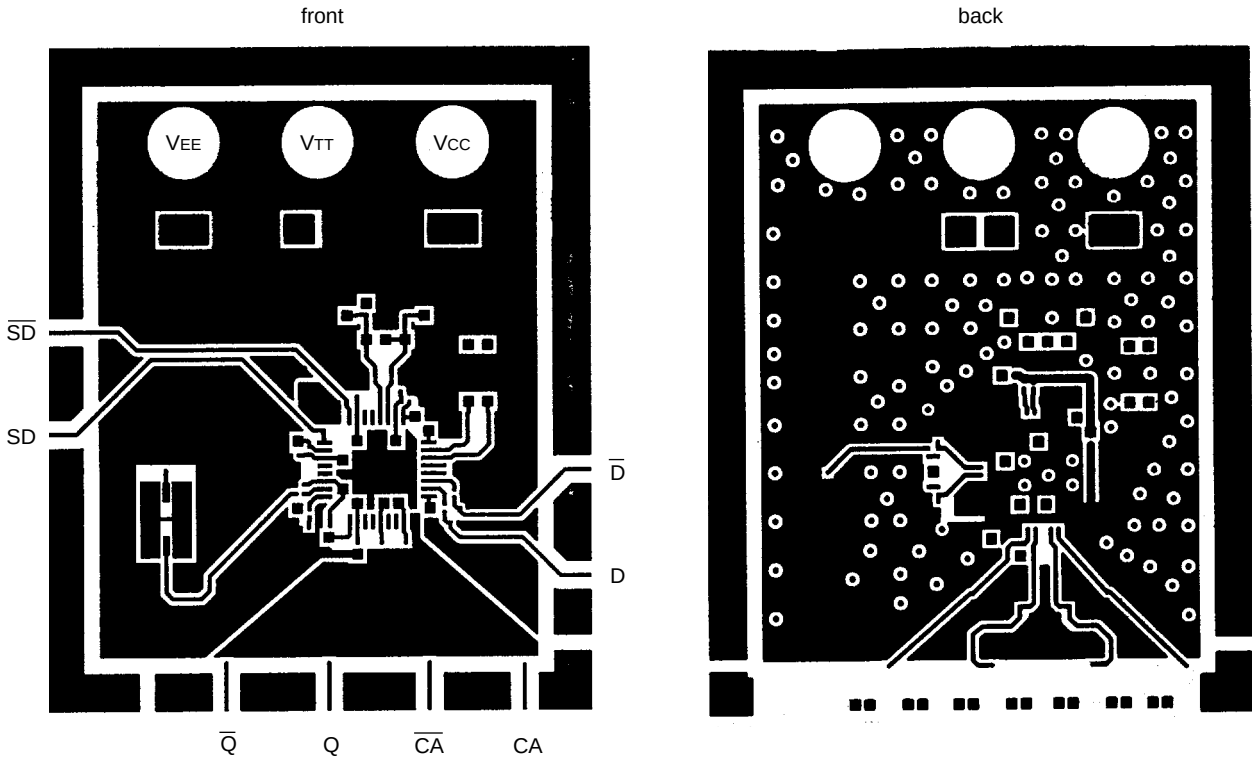


Fig. 13. Evaluation board pattern

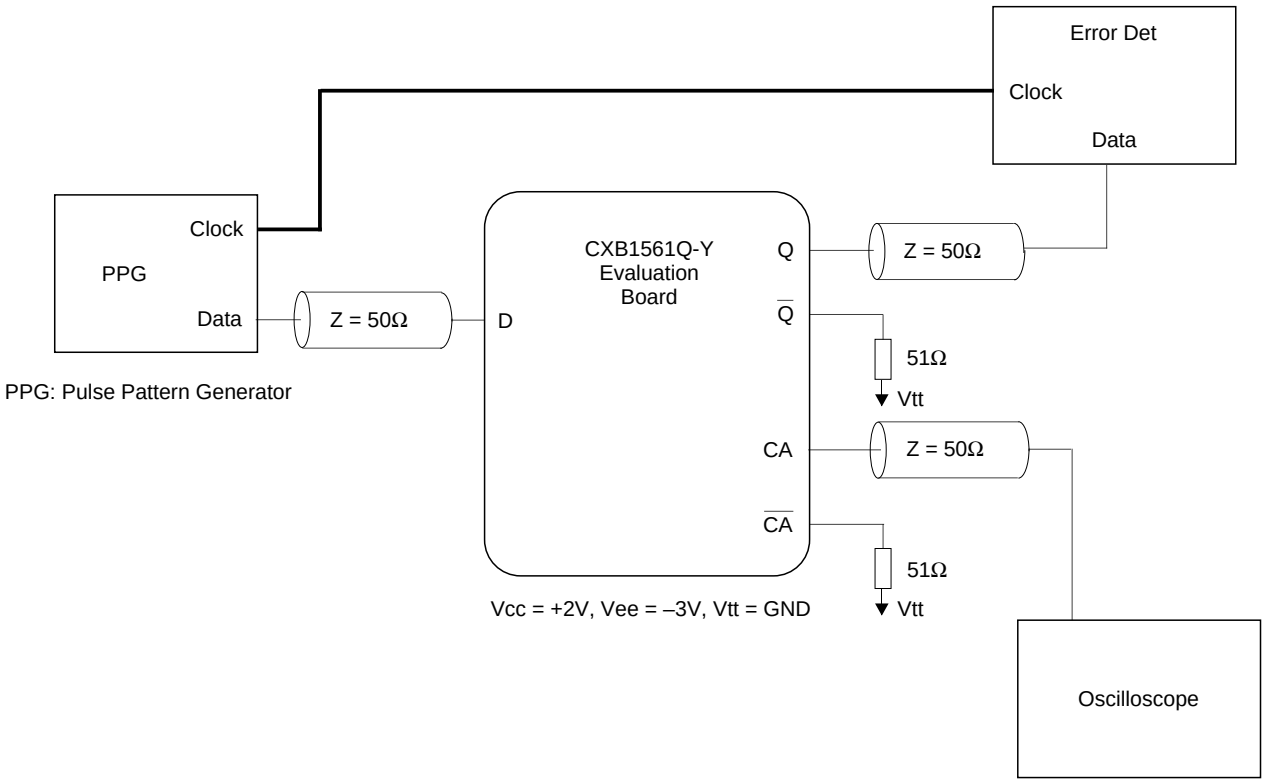


Fig. 14. Measurement Circut

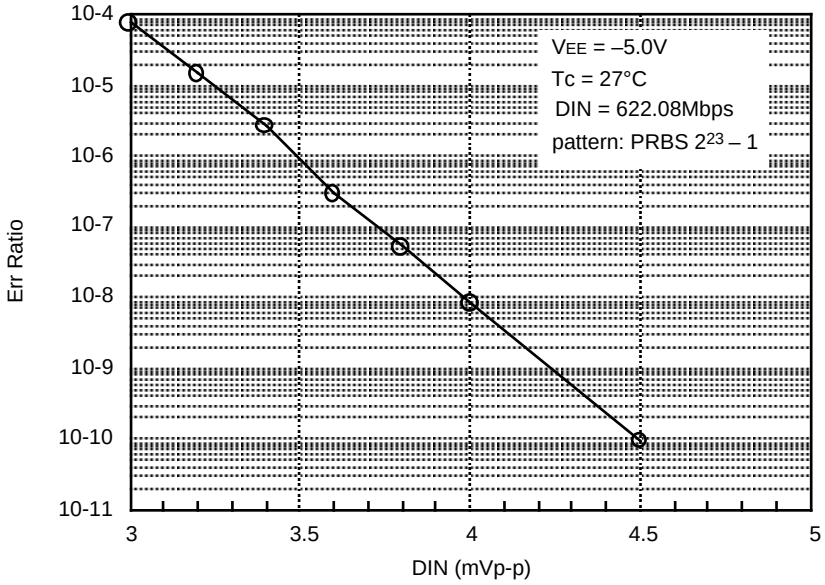


Fig. 15. Error rate vs. Input signal (mark density 1/2, pattern 2N23-1, Tc = 27°C)

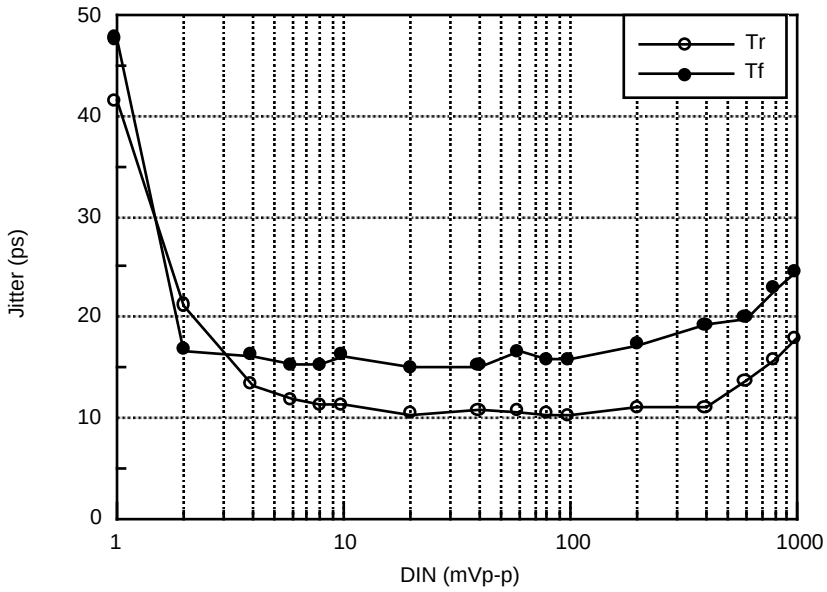


Fig. 16. Clock jitter vs. Input signal (mark density 1/2, pattern 2N23-1, Tc = 27°C)

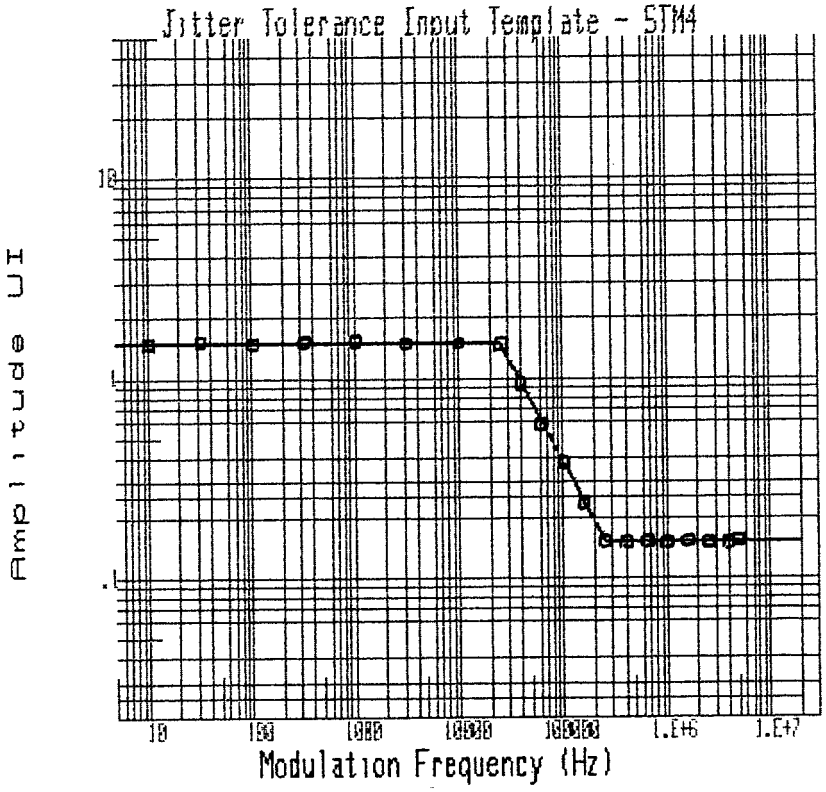


Fig. 17. jitter transfer (mark density 1/2, pattern 2N23-1, input voltage = 6mVp-p, Tc = 27°C)

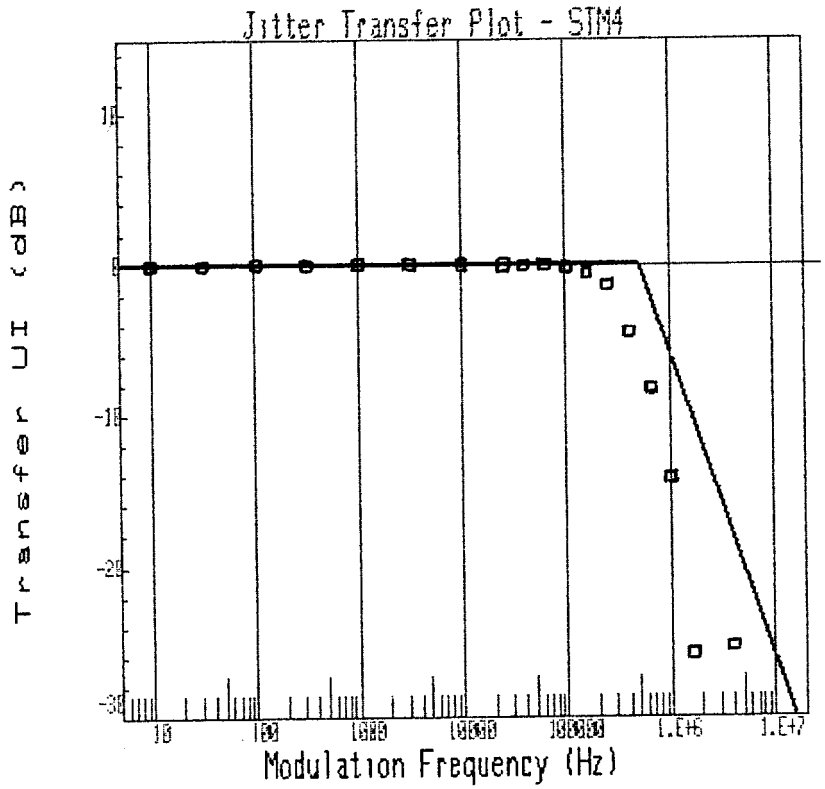
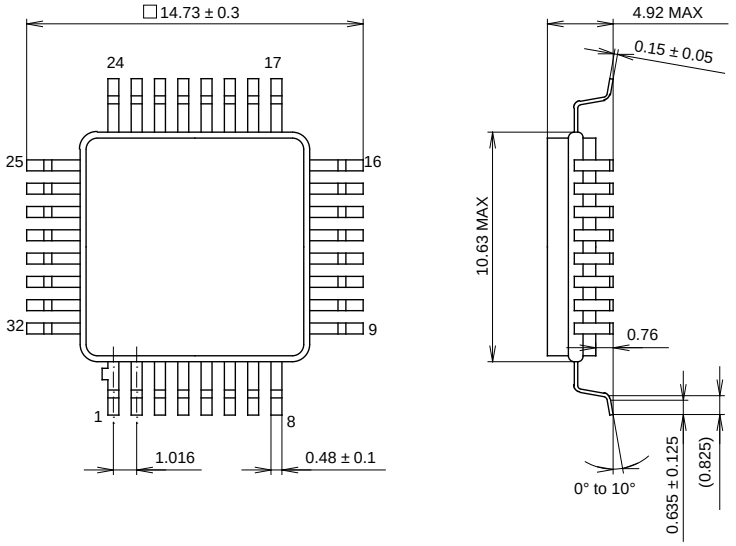


Fig. 18. jitter tolerance (mark density 1/2, pattern 2N23-1, input voltage = 6mVp-p, Tc = 27°C)

Package Outline Unit: mm

32PIN QFP (CERAMIC)



SONY CODE	QFP-32C-L01
EIAJ CODE	XQFP023-G-0000-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g