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SEMICONDUCTOR TM

74ALVCH162244
Low Voltage 16-Bit Buffer/Line Driver with Bushold and 26Ω Series Resistor in Outputs

General Description

The ALVCH162244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The ALVCH162244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level

The 74ALVCH162244 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCH162244 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with output capability up to 3.6V.

The 74ALVCH162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.
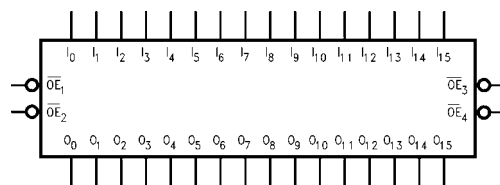
Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- 26Ω series resistors in outputs
- t_{PD}
    - 4.2 ns max for 3.0V to 3.6V V_{CC}
    - 4.9 ns max for 2.3V to 2.7V V_{CC}
    - 7.6 ns max for 1.65V to 1.95V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD performance:
    - Human body model > 2000V
    - Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Description
74ALVCH162244T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
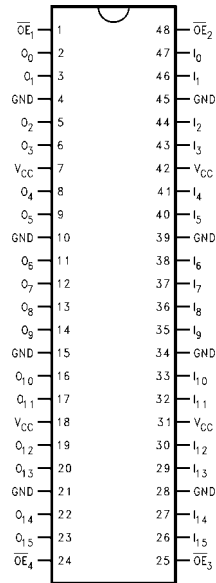
Logic Symbol

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{15}	Bushold Inputs
O_0–O_{15}	Outputs

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Connection Diagram

Pin		Pin	
$\overline{OE}_1$	1	48	$\overline{OE}_2$
O_0	2	47	I_0
O_1	3	46	I_1
GND	4	45	GND
O_2	5	44	I_2
O_3	6	43	I_3
V_{CC}	7	42	V_{CC}
O_4	8	41	I_4
O_5	9	40	I_5
GND	10	39	GND
O_6	11	38	I_6
O_7	12	37	I_7
O_8	13	36	I_8
O_9	14	35	I_9
GND	15	34	GND
O_{10}	16	33	I_{10}
O_{11}	17	32	I_{11}
V_{CC}	18	31	V_{CC}
O_{12}	19	30	I_{12}
O_{13}	20	29	I_{13}
GND	21	28	GND
O_{14}	22	27	I_{14}
O_{15}	23	26	I_{15}
$\overline{OE}_4$	24	25	$\overline{OE}_3$

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74ALVCH162244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation.The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

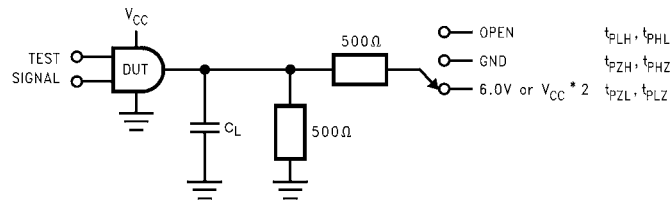**Note 2:** I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		V
			2.3 - 2.7	1.7		
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	V
			2.3 - 2.7		0.7	
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −2 mA	1.65	1.2		
		I_{OH} = −4 mA	2.3	1.9		
		I_{OH} = −6 mA	2.3	1.7		
			3	2.4		
		I_{OH} = −8 mA	2.7	2		
		I_{OH} = −12 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	V
		I_{OL} = 2 mA	1.65		0.45	
		I_{OL} = 4 mA	2.3		0.4	
		I_{OL} = 6 mA	2.3		0.55	
			3		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3		0.8	
I_{OH}	High Level Output Current		1.65		−2	mA
			2.3		−6	
			2.7		−8	
			3.0		−12	
I_{OL}	Low Level Output Current		1.65		2	mA
			2.3		6	
			2.7		8	
			3		12	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V$_{CC}$ (V)	Min	Max	Units
I$_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	V$_{IN}$ = 0.58V	1.65	25		μA
		V$_{IN}$ = 1.07V	1.65	−25		
		V$_{IN}$ = 0.7V	2.3	45		
		V$_{IN}$ = 1.7V	2.3	−45		
		V$_{IN}$ = 0.8V	3.0	75		
		V$_{IN}$ = 2.0V	3.0	−75		
		0 < V$_O$ ≤ 3.6V	3.6		±500	
I$_{OZ}$	3-STATE Output Leakage	0 ≤ V$_O$ ≤ 3.6V	3.6		±10	μA
I$_{CC}$	Quiescent Supply Current	V$_I$ = V$_{CC}$ or GND, I$_O$ = 0	3.6		40	μA
ΔI$_{CC}$	Increase in I$_{CC}$ per Input	V$_{IH}$ = V$_{CC}$ − 0.6V	3 - 3.6		750	μA

AC Electrical Characteristics

Symbol	Parameter	T$_A$ = −40°C to +85°C, R$_L$ = 500Ω								Units
		C$_L$ = 50 pF				C$_L$ = 30 pF				
		V$_{CC}$ = 3.3V ± 0.3V		V$_{CC}$ = 2.7V		V$_{CC}$ = 2.5V ± 0.2V		V$_{CC}$ = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t$_{PHL}$, t$_{PLH}$	Propagation Delay	1.0	4.2		4.7	1.0	4.9	1.5	7.6	ns
t$_{PZL}$, t$_{PZH}$	Output Enable Time	1.0	5.6		6.7	1.0	6.8	1.5	9.8	ns
t$_{PLZ}$, t$_{PHZ}$	Output Disable Time	1.0	5.5		5.7	1.0	6.3	1.5	7.2	ns

Capacitance

Symbol	Parameter		Conditions	T$_A$ = +25°C		Units
				V$_{CC}$	Typical	
C$_{IN}$	Input Capacitance	Control	V$_I$ = 0V or V$_{CC}$	3.3	3	pF
		Data	V$_I$ = 0V or V$_{CC}$	3.3	6	
C$_{OUT}$	Output Capacitance		V$_I$ = 0V or V$_{CC}$	3.3	7	pF
C$_{PD}$	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C$_L$ = 50 pF	3.3	19	pF
				2.5	16	
		Outputs Disabled	f = 10 MHz, C$_L$ = 50 pF	3.3	5	
				2.5	4	

AC Loading and Waveforms

74ALVCH162244

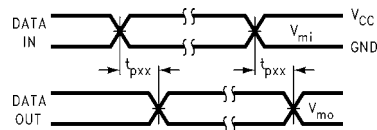| TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V; V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V; 1.8 ± 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit
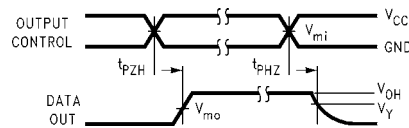

FIGURE 2. Waveform for Inverting and Non-Inverting Functions

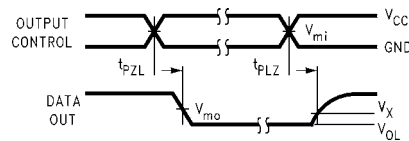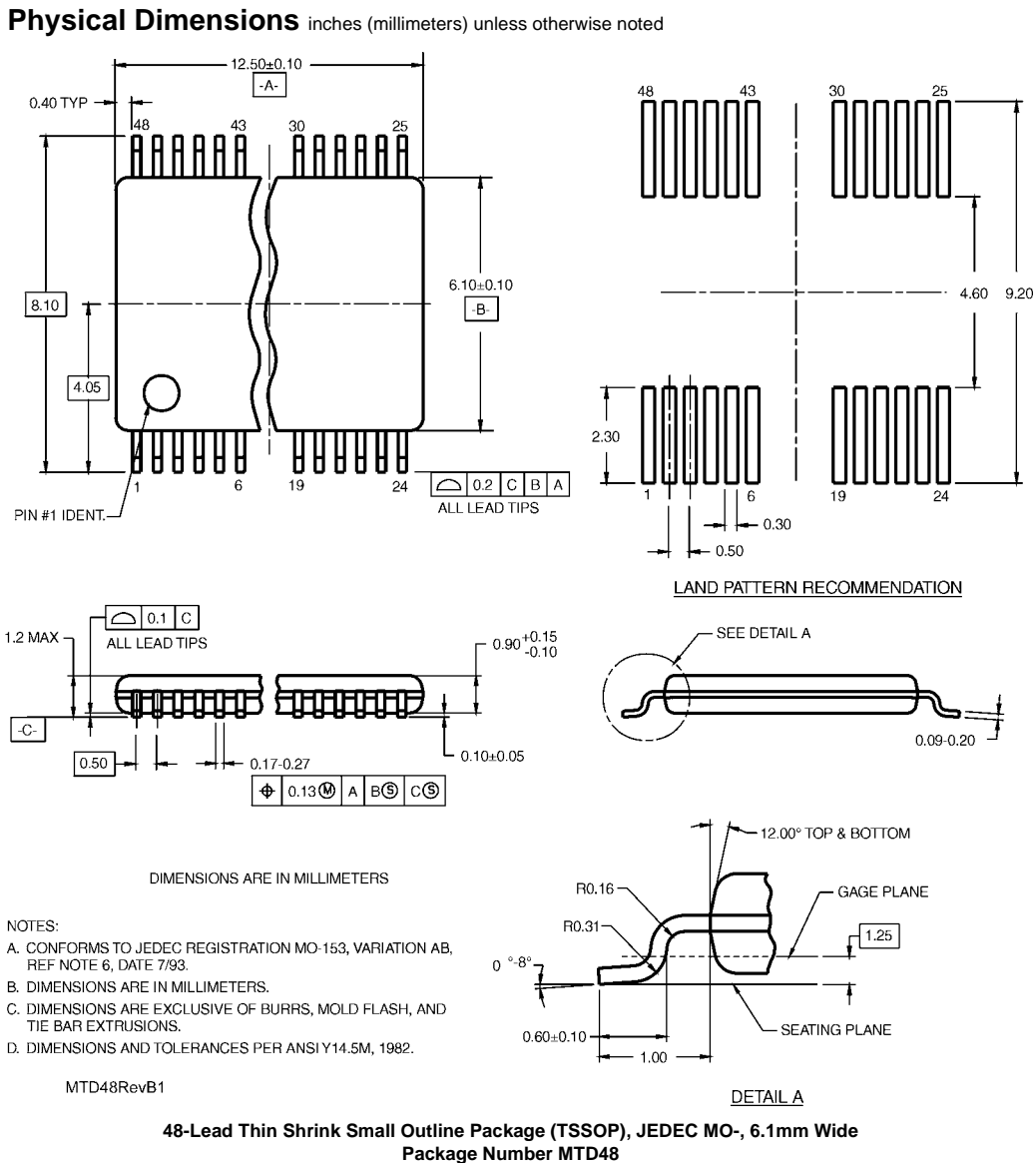**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	V_{CC}/2	V_{CC}/2
V_{mo}	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.15V
V_Y	V_{OH} −0.3V	V_{OH} −0.15V	V_{OH} −0.15V

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Physical Dimensions inches (millimeters) unless otherwise noted

12.50±0.10
-A-

0.40 TYP

48   43   30   25

8.10

4.05

6.10±0.10
-B-

PIN #1 IDENT.

1   6   19   24

△ 0.2 C B A
ALL LEAD TIPS

48   43   30   25

4.60   9.20

2.30

1   6   19   24

0.30

0.50

LAND PATTERN RECOMMENDATION

△ 0.1 C
ALL LEAD TIPS

1.2 MAX

-C-

0.50   0.17-0.27

$0.90^{+0.15}_{-0.10}$

0.10±0.05

⊕ 0.13 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

1.25

0 °–8°

0.60±0.10

1.00

SEATING PLANE

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

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