

# 1.2A, High Efficiency Stepdown DC/DC Converter

November 1994

## FEATURES

- **High Efficiency: Up to 95%**
- Current Mode Operation for Excellent Line and Load Transient Response
- **Internal 0.3Ω Power Switch ( $V_{IN} = 10V$ )**
- Short-Circuit Protection
- Low Dropout Operation: 100% Duty Cycle
- Low-Battery Detector
- Low 160μA Standby Current at Light Loads
- Active-High Micropower Shutdown:  $I_Q < 15\mu A$
- Peak Inductor Current Independent of Inductor Value
- Available in 14-pin SO Package

## APPLICATIONS

- Distributed Power Systems
- Stepdown Converters
- Inverting Converters
- Memory Backup Supply
- Portable Instruments
- Battery-Powered Equipment
- Cellular Telephones

## DESCRIPTION

The LTC<sup>®</sup>1265 is a monolithic step-down current mode DC/DC converter featuring Burst Mode™ operation at low output current. The LTC1265 incorporates a 0.3Ω switch ( $V_{IN} = 10V$ ) allowing up to 1.2A of output current.

Under no load condition, the converter draws only 160μA. In shutdown it typically draws a mere 5μA making this converter ideal for current sensitive applications. In dropout the internal P-channel MOSFET switch is turned on continuously maximizing the life of the battery source. The LTC1265 incorporates automatic power saving Burst Mode operation to reduce gate charge losses when the load currents drop below the level required for continuous operation.

The inductor current is user-programmable via an external current sense resistor. Operation up to 700kHz permits the use of small surface mount inductors and capacitors.

For applications requiring higher output currents, see the LTC1148 data sheet. For applications requiring less than 450mA, see the LTC1174 data sheet.

LTC and LT are registered trademarks of Linear Technology Corporation. Burst Mode is a registered trademark of Linear Technology Corporation.

## TYPICAL APPLICATION

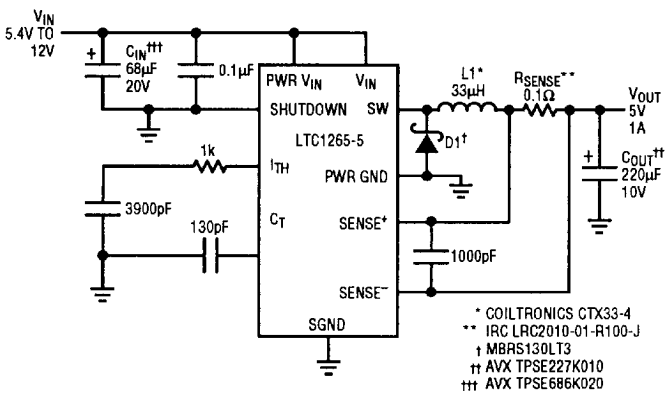
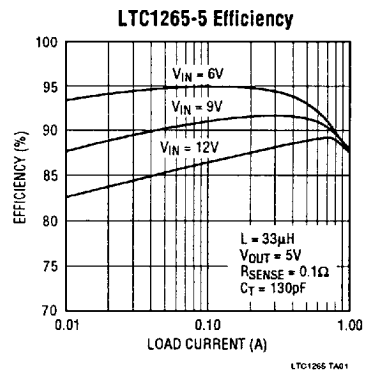


Figure 1. High Efficiency Step-Down Converter





**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 10\text{V}$ ,  $V_{SHUTDOWN} = 0\text{V}$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_8 - V_7$	Current Sense Threshold Voltage	LTC1265: $V_{SENSE^-} = 5\text{V}$ , $V_g = V_{OUT}/4 + 25\text{mV}$ (Forced) $V_{SENSE^-} = 5\text{V}$ , $V_g = V_{OUT}/4 - 25\text{mV}$ (Forced) LTC1265-3.3: $V_{SENSE^-} = V_{OUT} + 100\text{mV}$ (Forced) $V_{SENSE^-} = V_{OUT} - 100\text{mV}$ (Forced) LTC1265-5: $V_{SENSE^-} = V_{OUT} + 100\text{mV}$ (Forced) $V_{SENSE^-} = V_{OUT} - 100\text{mV}$ (Forced)	●	130	150	170	mV
$R_{ON}$	ON Resistance Of Switch		●	0.3	0.60	$\Omega$	
$I_5$	$C_T$ Pin Discharge Current	$V_{OUT}$ in Regulation, $V_{SENSE^-} = V_{OUT}$ $V_{OUT} = 0\text{V}$		50	70	90	$\mu\text{A}$
$t_{OFF}$	Switch Off-Time (Note 3)	$C_T = 390\text{pF}$ , $I_{LOAD} = 800\text{mA}$	●	4	5	6	$\mu\text{s}$
$V_{IH}$	Shutdown Pin High	Min Voltage at Pin 10 for Device to be in Shutdown		1.2		V	
$V_{IL}$	Shutdown Pin Low	Max Voltage at Pin 10 for Device to be Active			0.75	V	
$I_{10}$	Shutdown Pin Input Current	$V_{SHUTDOWN} = 8\text{V}$			0.5	$\mu\text{A}$	

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formulas:

LTC1265CN, LTC1265CN-3.3, LTC1265CN-5:

$$T_J = T_A + (P_D \times 80^\circ\text{C/W})$$

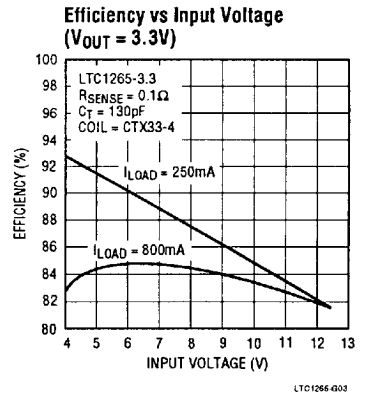
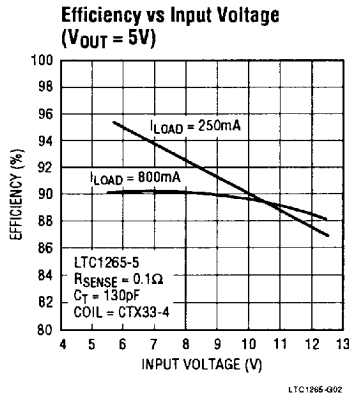
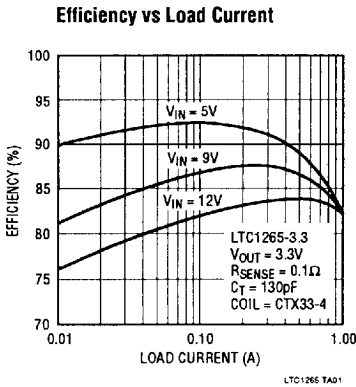
LTC1265CS, LTC1265CS14-3.3, LTC1265CS-5:

$$T_J = T_A + (P_D \times 110^\circ\text{C/W})$$

**Note 2:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

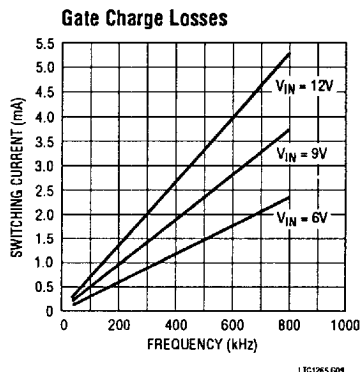
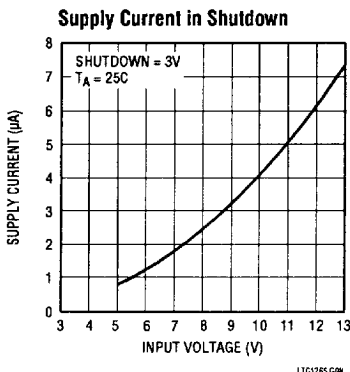
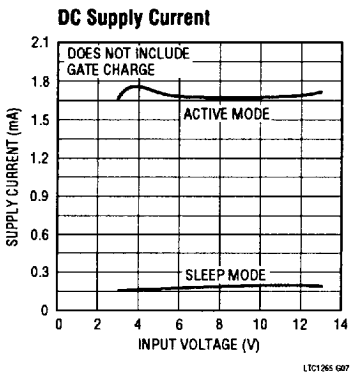
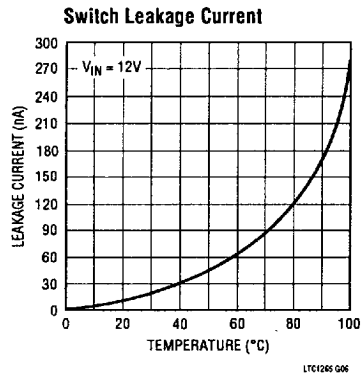
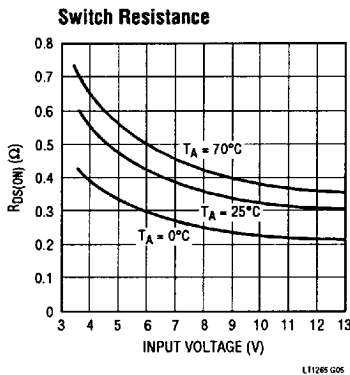
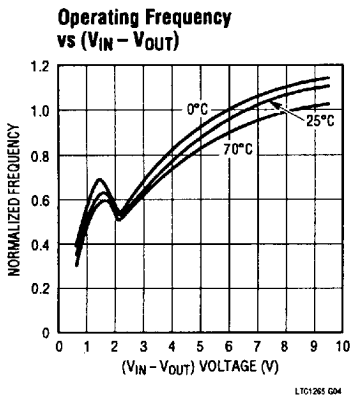
**Note 3:** In applications where  $R_{SENSE}$  is placed at ground potential, the off-time increases by approximately 40%.

**TYPICAL PERFORMANCE CHARACTERISTICS**



5518468 0011882 91T

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**Pin 1, 13 ( $PWR V_{IN}$ ):** Supply for the Power MOSFET and its Driver. Must decouple this pin properly to ground. Must always tie pins 1 and 13 together.

**Pin 2 ( $V_{IN}$ ):** Main Supply for all the control circuitry in the LTC1265.

**Pin 3 ( $LB_{OUT}$ ):** Open Drain Output of the Low-Battery Comparator. This pin will sink current when pin 4 ( $LB_{IN}$ ) goes below 1.25V. During shutdown, this pin is high impedance.

**Pin 4 ( $LB_{IN}$ ):** The (-) Input of the Low-Battery Comparator. The (+) Input is connected to a reference voltage of 1.25V.

**Pin 5 ( $C_T$ ):** External capacitor  $C_T$  from pin 5 to ground sets the switch off-time. The operating frequency is dependent on the input voltage and  $C_T$ .

**Pin 6 ( $I_{TH}$ ):** Feedback Amplifier Decoupling Point. The current comparator threshold is proportional to pin 6 voltage.

**Pin 7 ( $SENSE^-$ ):** Connect to the (-) Input of the current comparator. For LTC1265-3.3 and LTC1265-5, it also connects to an internal resistive divider which sets the output voltage.

**Pin 8 (SENSE<sup>+</sup>):** The (+) Pin to the Current Comparator. A built-in offset between pins 7 and 8 in conjunction with  $R_{SENSE}$  sets the current trip threshold.

**Pin 9 (N/C,  $V_{FB}$ ):** For the LTC1265 adjustable version, this pin serves as the feedback pin from an external resistive divider used to set the output voltage. On the LTC1265-3.3 and LTC1265-5 versions, this pin is not used.

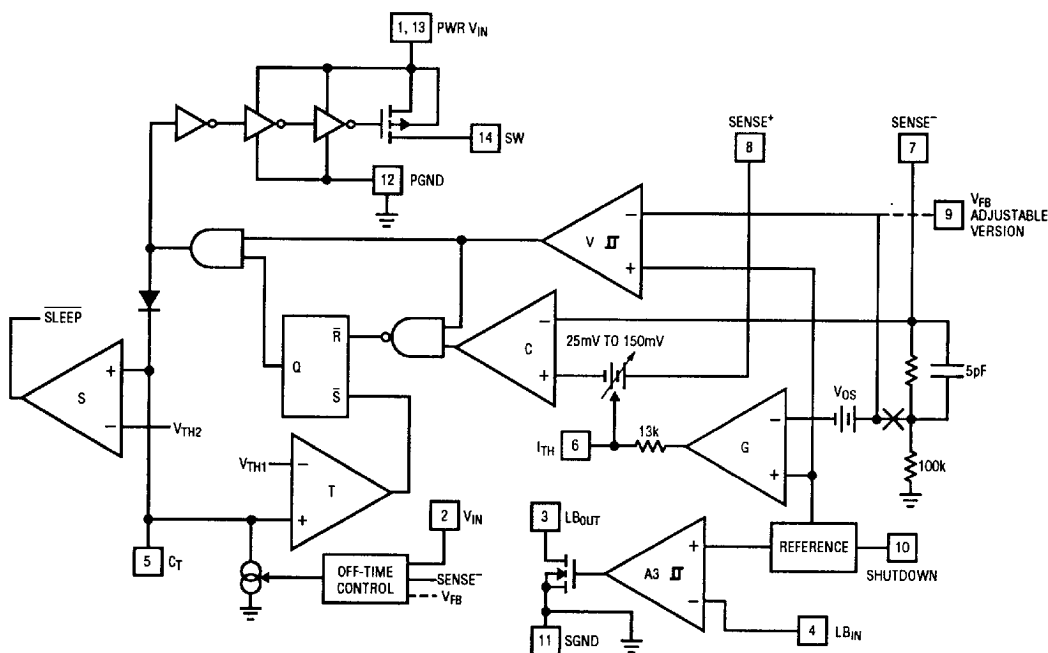
**Pin 10 (Shutdown):** Pulling this pin HIGH keeps the internal switch off and puts the LTC1265 in micropower shutdown. Do not float this pin.

**Pin 11 (SGND):** Small-Signal Ground. Must be routed separately from other grounds to the (-) terminal of  $C_{OUT}$ .

**Pin 12 (PGND):** Switch Driver Ground. Connects to the (-) terminal of  $C_{IN}$ .

**Pin 14 (SW):** Drain of the P-Channel MOSFET Switch. Cathode of the Shottky diode must be connected close to this pin.

## FUNCTIONAL DIAGRAM (Pin 9 connection shown for LTC1265-3.3 and LTC1265-5; change create LTC1265)



## OPERATION (Refer to Functional Diagram)

The LTC1265 uses a constant off-time architecture to switch its internal P-channel power MOSFET. The off-time is set by an external timing capacitor at  $C_T$  (pin 5). The operating frequency is then determined by the off-time and the difference between  $V_{IN}$  and  $V_{OUT}$ .

The output voltage is set by an internal resistive divider (LTC1265-3.3 and LTC1265-5) connected to Sense<sup>-</sup> (pin 7) or an external divider returned to  $V_{FB}$  (pin 9 for LTC1265). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V.

## OPERATION (Refer to Functional Diagram)

To optimize efficiency, the LTC1265 automatically switches between continuous and Burst Mode operation. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

When the load is heavy, the LTC1265 is in continuous operation. During the switch ON time, current comparator C monitors the voltage between pins 7 and 8 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches the comparator's threshold value, its output signal will change state, setting the flip flop and turning the internal P-channel MOSFET off. The timing capacitor connected to pin 5 is now allowed to discharge at a rate determined by the off-time controller.

When the voltage on the timing capacitor has discharged past  $V_{TH1}$ , comparator T trips, sets the flip flop and causes the switch to turn on. Also, the timing capacitor is recharged. The indicator current will again ramp up until the current comparator C trips. The cycle then repeats.

When the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (pin 6) to increase the current comparator threshold, thus tracking the load current.

When the load is relatively light, the LTC1265 automatically goes into Burst Mode operation. The current loop is interrupted when the output voltage reaches the desired

regulated value. The hysteretic voltage comparator V trips when  $V_{OUT}$  is above the desired output voltage, shutting off the switch and causing the capacitor to discharge. This capacitor discharges past  $V_{TH1}$  until its voltage drops below  $V_{TH2}$ . Comparator S then trips and a sleep signal is generated. The circuit now enters into sleep mode with the power MOSFET turned off. In sleep mode, the LTC1265 is in standby and the load current is supplied by the output capacitor. All unused circuitry is shut off, reducing quiescent current from 2mA to 160 $\mu$ A. When the output capacitor discharges by the amount of the hysteresis of the comparator V, the P-channel switch turns on again and the process repeats itself. During Burst Mode the peak inductor's current is set at  $25mV/R_{SENSE}$ .

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset  $V_{OS}$  is incorporated in the gain stage. This prevents the current from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture, the operating frequency is a function of the voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as  $V_{IN}$  drops below  $V_{OUT} + 1.5V$ . In dropout the P-channel MOSFET is turned on continuously (100% duty cycle) providing low dropout operation with  $V_{OUT} \cong V_{IN}$ .

## APPLICATIONS INFORMATION

The basic LTC1265 application circuit is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of  $R_{SENSE}$ . Once  $R_{SENSE}$  is known,  $C_T$  and L can be chosen. Next, the Schottky diode D1 is selected followed by  $C_{IN}$  and  $C_{OUT}$ .

### $R_{SENSE}$ Selection for Output Current

$R_{SENSE}$  is chosen based on the required output current. With the current comparator monitoring the voltage developed across  $R_{SENSE}$ , the threshold of the comparator

determines the inductor's peak current. Depending on the load current condition, the threshold of the comparator lies between  $25mV/R_{SENSE}$  and  $150mV/R_{SENSE}$ . The maximum output current of the LTC1265 is:

$$I_{OUT(MAX)} = \frac{150mV}{R_{SENSE}} - \frac{I_{RIPPLE}}{2} \text{ (A)}$$

where  $I_{RIPPLE}$  is the inductor's peak-to-peak ripple current.

At a relatively light load, the LTC1265 is in Burst Mode operation. In this mode the inductor's peak current is set

## APPLICATIONS INFORMATION

at  $25\text{mV}/R_{\text{SENSE}}$ . To fully benefit from Burst Mode operation, the inductor current should be continuous during burst periods. Hence, the inductors peak-to-peak ripple current must not exceed  $25\text{mV}/R_{\text{SENSE}}$ .

To account for light and heavy load conditions, the  $I_{\text{OUT(MAX)}}$  is then given by:

$$I_{\text{OUT(MAX)}} = \frac{150\text{mV}}{R_{\text{SENSE}}} - \frac{25\text{mV}}{2 \times R_{\text{SENSE}}} \quad (\text{A})$$

$$= \frac{137.5\text{mV}}{R_{\text{SENSE}}} \quad (\text{A})$$

Solving for  $R_{\text{SENSE}}$  and allowing a margin of variations in the LTC1265 and extended component values yields:

$$R_{\text{SENSE}} = \frac{100\text{mV}}{I_{\text{OUT(MAX)}}} \quad (\Omega) \quad (1)$$

The LTC1265 is rated with a capability to supply a maximum of 1.2A of output current. Therefore, the minimum value of  $R_{\text{SENSE}}$  that can be used is  $0.083\Omega$ . A graph for selecting  $R_{\text{SENSE}}$  versus maximum output is given in Figure 2.

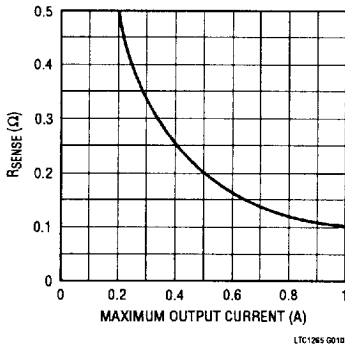


Figure 2. Selecting  $R_{\text{SENSE}}$

Under short-circuit condition, the peak inductor current is determined by:

$$I_{\text{SC(PK)}} = \frac{150\text{mV}}{R_{\text{SENSE}}} \quad (\text{A})$$

In this condition, the LTC1265 automatically extends the off-time of the P-channel MOSFET to allow the inductor's

current to decay far enough to prevent any current build-up. The resulting ripple current causes the average short-circuit current to be approximately  $I_{\text{OUT(MAX)}}$ .

### $C_T$ and L Selection for Operating Frequency

The LTC1265 uses a constant off-time architecture with  $t_{\text{OFF}}$  determined by an external capacitor  $C_T$ . Each time the P-channel MOSFET turns on, the voltage on  $C_T$  is reset to approximately 3.3V. During the off-time,  $C_T$  is discharged by a current which is proportional to  $V_{\text{OUT}}$ . The voltage on  $C_T$  is analogous to the current in inductor L, which likewise, decays at a rate proportional to  $V_{\text{OUT}}$ . Thus the inductor value must track the timing capacitor value.

The value of  $C_T$  is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3 \times 10^4 \times f} \left( \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}} + V_D} \right) \quad (\text{F}) \quad (2)$$

where  $V_D$  is the drop across the Schottky diode.

As the operating frequency is increased the gate charge losses will reduce efficiency. The complete expression for operating frequency is given by:

$$f \approx \frac{1}{t_{\text{OFF}}} \left( 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) \quad (\text{Hz})$$

where:

$$t_{\text{OFF}} = 1.3 \times 10^4 \times C_T \times \left( \frac{V_{\text{REG}}}{V_{\text{OUT}}} \right) \quad (\text{sec})$$

$V_{\text{REG}}$  is the desired output voltage (i.e. 5V, 3.3V).  $V_{\text{OUT}}$  is the measured output voltage. Thus  $V_{\text{REG}}/V_{\text{OUT}} = 1$  in regulation.

Note that as  $V_{\text{IN}}$  decreases, the frequency decreases. When the input-to-output voltage differential drops below 1.5V, the LTC1265 reduces  $t_{\text{OFF}}$  by increasing the discharge current in  $C_T$ . This prevents audible operation prior to dropout. (See shelving effect shown in "Operating Frequency" curve under Typical Performance Characteristics.)

## APPLICATIONS INFORMATION

To maintain continuous inductor current at light load, the inductor must be chosen to provide no more than 25mV/ $R_{SENSE}$  of peak-to-peak ripple current. This results in the following expression for L:

$$L \geq 5.2 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG} \quad (3)$$

Using an inductance smaller than the above value will result in the inductor's current being discontinuous. A consequence of this is that the LTC1265 will delay entering Burst Mode operation and efficiency will be degraded at low currents.

### Inductor Core Selection

With the value of L selected, the type of inductor must be chosen. Basically, there are two kinds of losses in an inductor; core and copper losses.

Core losses are dependent on the peak-to-peak ripple current and core material. However it is independent of the physical size of the core. By increasing the inductance, the inductor's peak-to-peak ripple current will decrease, therefore reducing core loss. Utilizing low core loss material, such as molypermalloy or KoolM $\mu$ <sup>®</sup> will allow user to concentrate on reducing copper loss and preventing saturation.

Although higher inductance reduces core loss, it increases copper loss as it requires more windings. When space is not at a premium, larger wire can be used to reduce the wire resistance. This also prevents excessive heat dissipation.

### CATCH DIODE SELECTION

Losses in the catch diode depend on forward drop and switching times. Therefore Schottky diodes are a good choice for low drop and fast switching times.

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages, the diode conducts most of the time. As  $V_{IN}$  approaches  $V_{OUT}$ , the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output

is short circuited. Under this condition, the diode must safely handle  $I_{SC(PK)}$  at close to 100% duty cycle. Most LTC1265 circuits will be well served by either a 1N5818 or a MBRS130LT3 Schottky Diode. An MBRS0520 is a good choice for  $I_{OUT(MAX)} \leq 500mA$ .

### $C_{IN}$

In continuous mode, the input current of the converter is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor must be used. In addition, the capacitor must handle a high RMS current. The  $C_{IN}$  RMS current is given by:

$$I_{RMS} \approx \frac{I_{OUT} [V_{OUT} (V_{IN} - V_{OUT})]^{1/2}}{V_{IN}} \quad (A_{RMS}) \quad (4)$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst case is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. **Do not underspecify this component.** An additional 0.1 $\mu$ F ceramic capacitor is also required on PWR  $V_{IN}$  for high frequency decoupling.

### $C_{OUT}$

The selection of  $C_{OUT}$  is based upon the effective series resistance (ESR) for proper operation of the LTC1265. The required ESR of  $C_{OUT}$  is:

$$ESR_{C_{OUT}} < 50mV/I_{RIPPLE}$$

where  $I_{RIPPLE}$  is the ripple current of the inductor. For the case where the  $I_{RIPPLE}$  is 25mV/ $R_{SENSE}$ , the required ESR of  $C_{OUT}$  is:

$$ESR_{C_{OUT}} < 2R_{SENSE} \quad (5)$$

To avoid overheating, the output capacitor must be sized to handle the ripple current generated by the inductor. The worst case RPM ripple current in the output capacitor is given by:

$$I_{RMS} \approx \frac{150mV}{2 \times R_{SENSE}} \quad (A_{RMS})$$



## APPLICATIONS INFORMATION

Generally, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating far exceeds the  $I_{RIPPLE(P-P)}$  requirement.

ESR is a direct function of the volume of the capacitor. Manufacturers such as Nichicon, AVX and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolyte and dry tantalum capacitors are both available in surface mount configurations. In case of tantalum, it is critical that the capacitors are both available in surface mount configuration and are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Consult the manufacturer for other specific recommendations.

When the capacitance of  $C_{OUT}$  is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1265 would normally be in continuous operation. The effect will be most pronounced with low value of  $R_{SENSE}$  and can be improved at higher frequencies with lower values of L.

### Low-Battery Detection

The low-battery comparator senses the input voltage through an external resistive divider. This divided voltage connects to the (-) input of a voltage comparator (pin 4) which is compared with a 1.25V reference voltage. Neglecting pin 4 bias current, the following expression is used for setting the trip limit:

$$V_{LB\_TRIP} = 1.25 \left( 1 + \frac{R4}{R3} \right)$$

The output, pin 3, is an N-channel open drain which goes low when the battery voltage is below the threshold set by R3 and R4. In shutdown, the comparator is disabled and pin 3 is in a high impedance state.

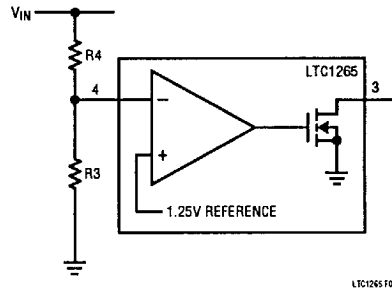


Figure 3. Low Battery Comparator

### LTC1265 ADJUSTABLE APPLICATIONS

The LTC1265 develops a 1.25V reference voltage between the feedback (pin 9) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.25 \left( 1 + \frac{R2}{R1} \right)$$

For most applications a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1265.

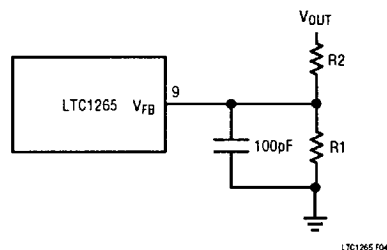


Figure 4. LTC1265 Adjustable Configuration

## APPLICATIONS INFORMATION

### Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1265. These items are also illustrated graphically in the layout diagram of Figure 5. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1265 signal ground (pin 11) must return to the (-) plate of  $C_{OUT}$ . The power ground (pin 12) returns to the anode of the Schottky diode, and the (-) plate of  $C_{IN}$ , whose leads should be as short as possible.
2. Does the (+) plate of the  $C_{IN}$  connect to the power  $V_{IN}$  (pin 1, 13) as close as possible? This capacitor provides the AC current to the internal P-channel MOSFET and its driver.
3. Is the input decoupling capacitor ( $0.1\mu\text{F}$ ) connected closely between power  $V_{IN}$  (pin 1, 13) and power ground (pin 12)? This capacitor carries the high frequency peak currents.
4. Is the Schottky diode closely connected between the power ground (pin 12) and switch (pin 14)?
5. Does the LTC1265 Sense<sup>-</sup> (pin 7) connect to a point close to  $R_{SENSE}$  and the (+) plate of  $C_{OUT}$ ? In adjustable applications, the resistive divider, R1, and R2, must be connected between the (+) plate of  $C_{OUT}$  and signal ground.
6. Are the Sense<sup>-</sup> and Sense<sup>+</sup> leads routed together with minimum PC trace spacing? The  $100\text{pF}$  capacitor between pins 7 and 8 should be as close as possible to the LTC1265.
7. Is Shutdown (pin 10) actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

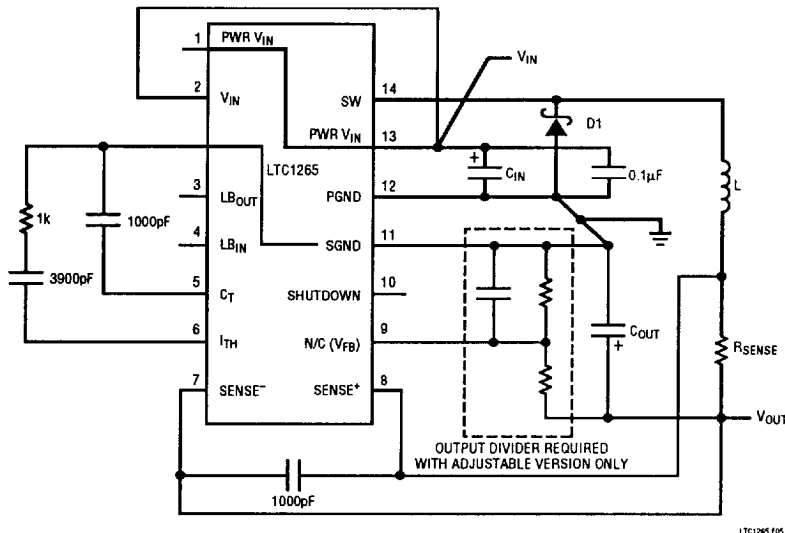


Figure 5. LTC1265 Layout Diagram (See Board Layout Checklist)

## APPLICATIONS INFORMATION

### Troubleshooting Hints

Since efficiency is critical to LTC1265 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. As the LTC1265 is highly tolerant of poor layout, the output voltage will still be regulated. Therefore, monitoring the output voltage will not tell you whether you have a good or bad layout. The waveform to monitor is the voltage on the timing capacitor pin 5.

In continuous mode the voltage on the  $C_T$  pin is a sawtooth with approximately  $0.9V_{P-P}$  swing. This voltage should never dip below 2V as shown in Figure 6a.

When the load currents are low ( $I_{LOAD} < I_{BURST}$ ) Burst Mode operation occurs. The voltage on  $C_T$  pin now falls to ground for periods of time as shown in Figure 6b. During this time the LTC1265 is in sleep mode with quiescent current reduced to  $160\mu A$ .

The inductor current should also be monitored. If the circuit is poorly decoupled, the inductor's peak current will be haphazard as in Figure 7a. A well decoupled LTC1265 has a clean inductor current as in Figure 7b.

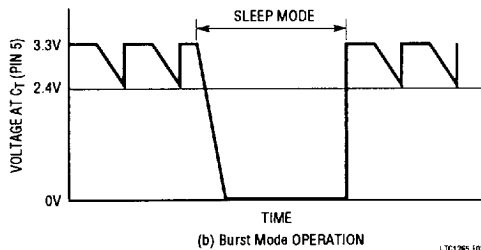
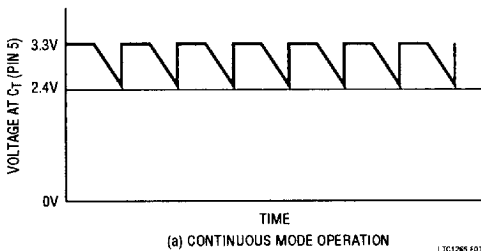
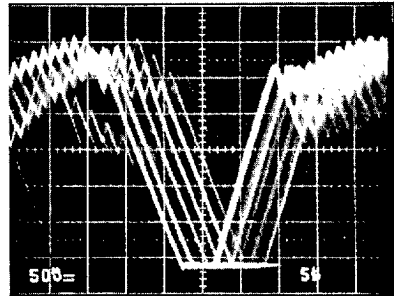
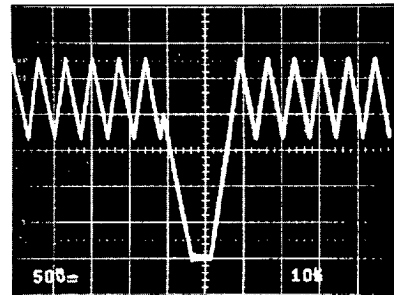


Figure 6.  $C_T$  Waveforms



(a) Poorly Decoupled LTC1265



(b) Well Decoupled LTC1265

Figure 7. Inductor's Waveform

## APPLICATIONS INFORMATION

### Design Example

As a design example, assume  $V_{IN} = 5V$ ,  $V_{OUT} = 3.3V$ ,  $I_{MAX} = 0.8A$ , and  $f = 250kHz$ . With this information we can easily calculate all the important components.

From (1),

$$R_{SENSE} = 100mV/0.8 = 0.125\Omega$$

From (2) and assuming  $V_D = 0.4V$ ,

$$C_T \cong 100pF$$

Using (3), the value of inductor is:

$$L \geq 5.2 \times 10^5 \times 0.125 \times 105pF \times 3.3V = 22\mu H$$

For the catch diode, a MBRS130LT3 or 1N5818 will be sufficient in this application.

$C_{IN}$  will require an RMS current rating of at least 0.4A at temperature, and  $C_{OUT}$  will require an ESR of (from 5):

$$ESR_{COUT} < 0.25\Omega$$

The inductor's ripple current is given by:

$$I_{RIPPLE} \cong \left( \frac{V_{OUT}}{L} \right) t_{OFF} = 0.2A$$

At light loads the inductor's peak current is at:

$$I_{PEAK} = 25mV/0.125 = 0.2A$$

Therefore, at load current less than 0.1A the LTC1265 will be in Burst Mode. Figure 8 shows the complete circuit and Figure 9 shows the efficiency curve with the above calculated component values.

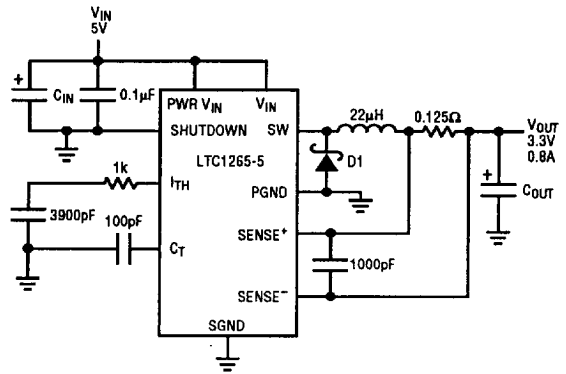


Figure 8. Design Example Circuit

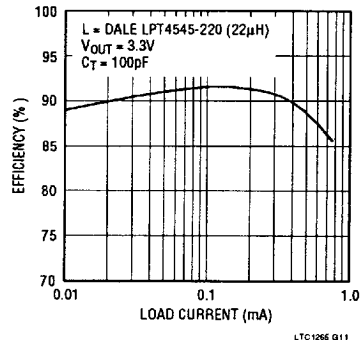
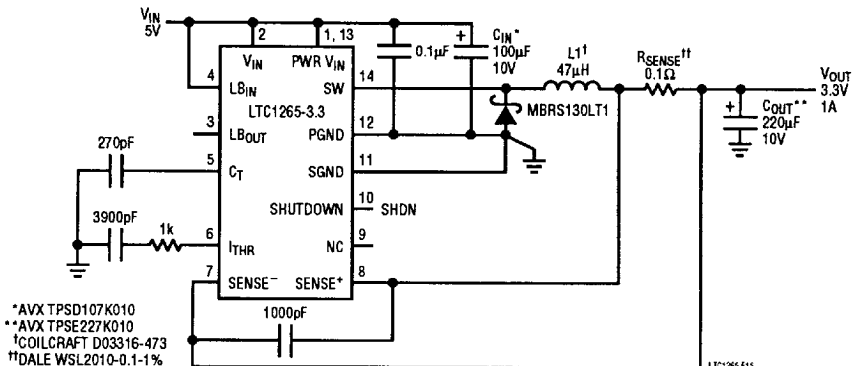


Figure 9. Design Example Efficiency Curve

TYPICAL APPLICATIONS

High Efficiency 5V to 3.3V Converter



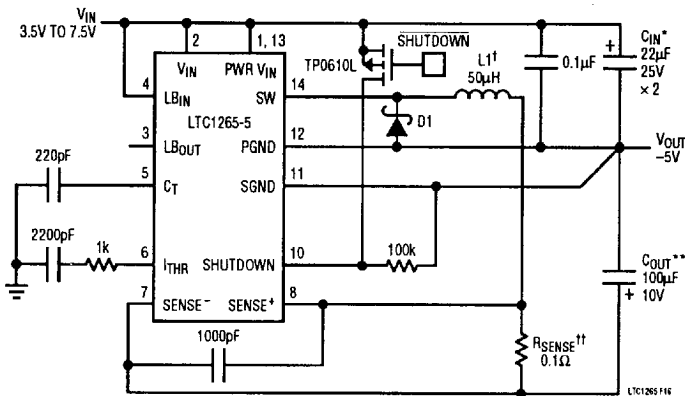
Positive-to-Negative (-5V) Converter

\*AVX TPSD226K025  
 \*\*AVX TPSD107K010  
 †L1 SELECTION

MANUFACTURER	PART NO.
COILCRAFT	CTX50-4
COILTRONICS	D03316-473
DALE	LPT4545-500LA
SUMIDA	CD74-470

††IRC LRC2010-01-R100-J  
 D1= MBR5130LT3

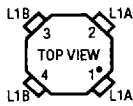
V <sub>IN</sub> (V)	I <sub>OUT</sub> (MAX) (mA)
3.5	360
4.0	430
5.0	540
6.0	630
7.0	720
7.5	740



TYPICAL APPLICATIONS

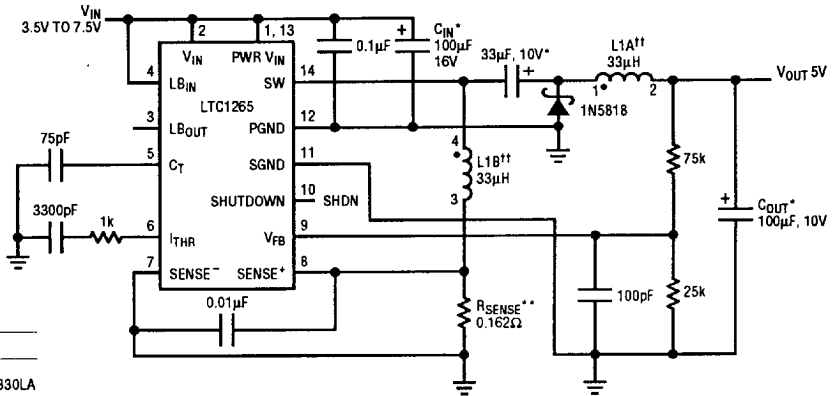
5V Buck-Boost Converter

V <sub>IN</sub> (V)	I <sub>OUT</sub> (MAX) (mA)
3.5	240
4.0	275
5.0	365
6.0	490
7.0	610
7.5	665



\*SANYO OS-CON CAPACITOR  
 \*\*IRC LRC2010-01-R162-J  
 †L1A, L2A SELECTION

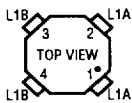
MANUFACTURER	PART NO.
COILTRONICS	CTX33-4
DALE	LPT4545-330LA



LTC1265 F09

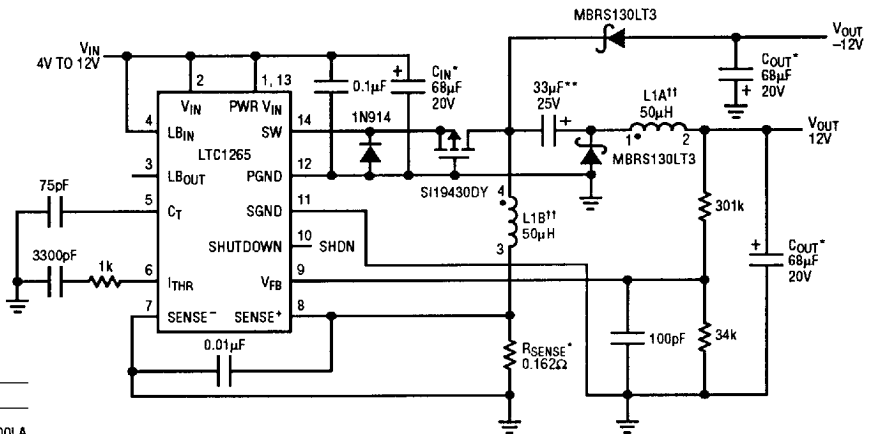
9V to 12V and -12V Outputs

V <sub>IN</sub> (V)	I <sub>OUT</sub> (MAX) (mA)
4.0	40
5.0	60
6.0	80
7.0	100
8.0	115
9.0	130
10.0	150
11.0	165
12.0	180



\*AVX TPSE686K020  
 \*\*AVX TPSE336K025  
 †IRC LRC2010-01-R162-J  
 ††L1A, L2A SELECTION

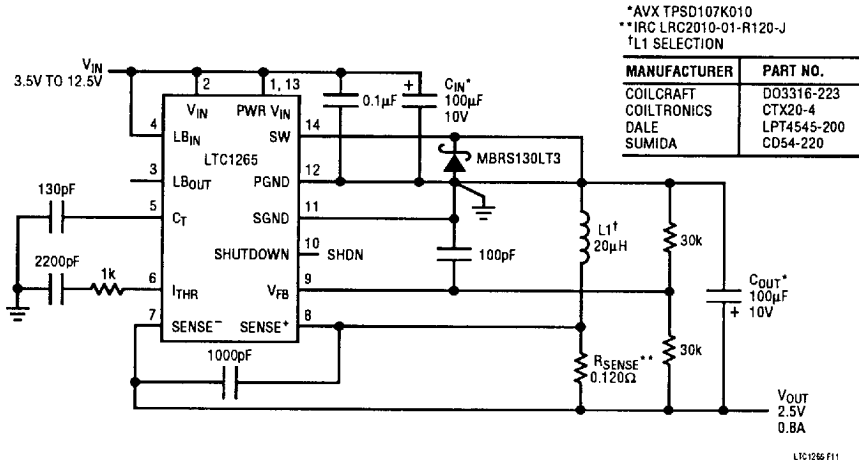
MANUFACTURER	PART NO.
COILTRONICS	CTX50-4
DALE	LPT4545-500LA



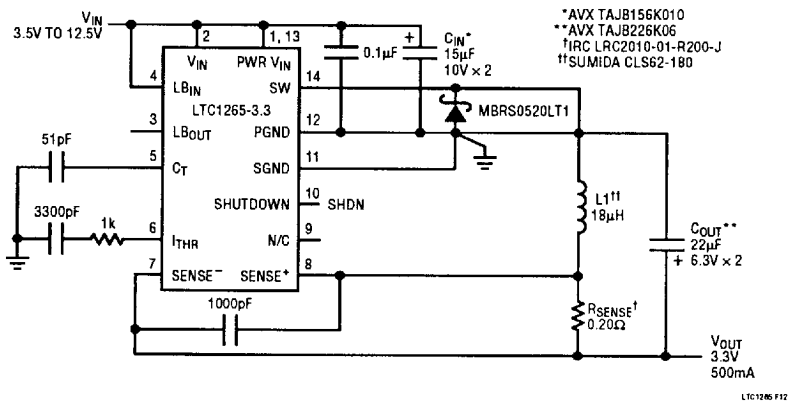
LTC1265 F10

TYPICAL APPLICATIONS

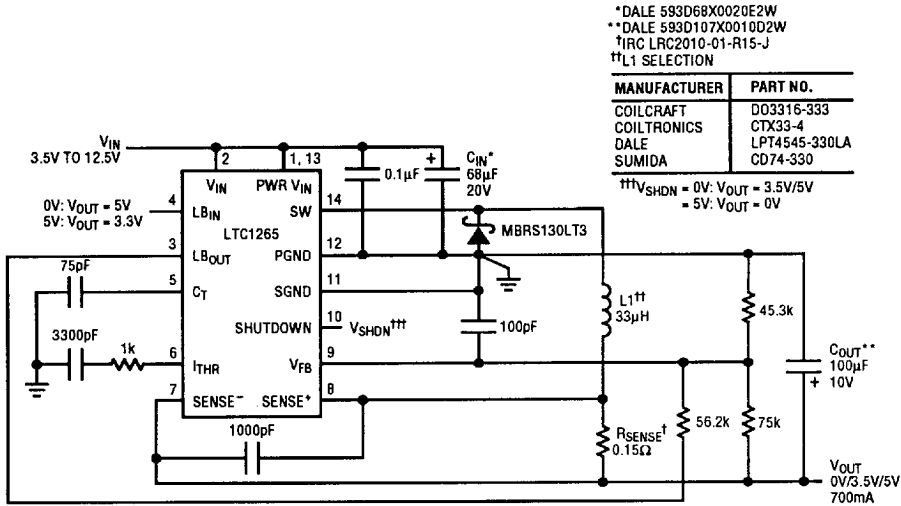
5V-to-2.5V Converter



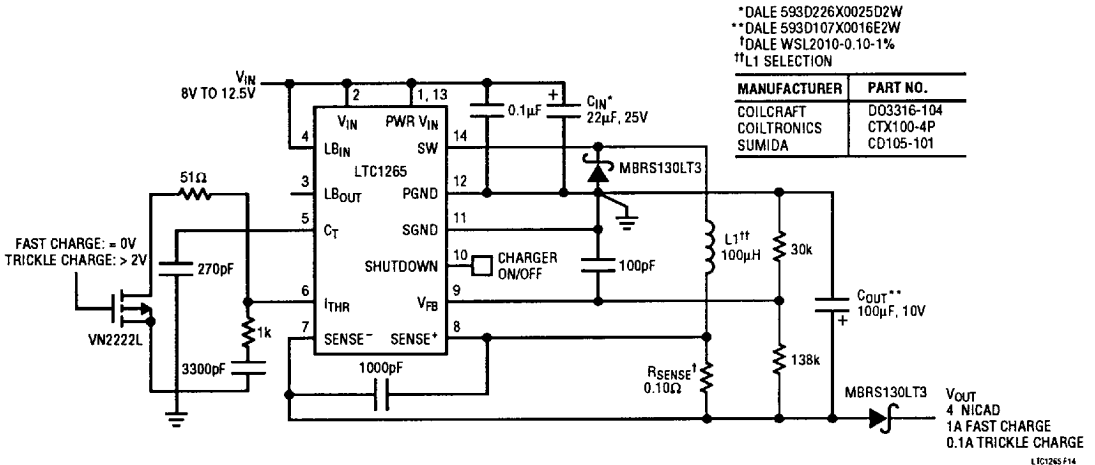
2.5mm Max. Height 5V-to-3.3V (500mA)



## Logic Selectable 0V/3.3V/5V 700mA Regulator



## 4-NiCad Battery Charger



5518468 0011895 578

**16** Linear Technology Corporation  
 1630 McCarthy Blvd., Milpitas, CA 95035-7487  
 (408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LTGP 1184 6K • PRINTED IN USA  
  
 © LINEAR TECHNOLOGY CORPORATION 1994

50183