PD - 96101

International
IOR Rectifier

AUTOMOTIVE MOSFET

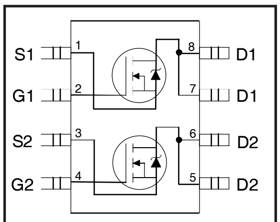
IRF7103QPbF

Typical Applications
- Anti-lock Braking Systems (ABS)
- Electronic Fuel Injection
- Power Doors, Windows & Seats

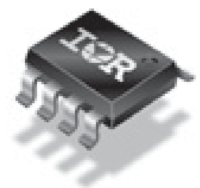
Benefits
- Advanced Process Technology
- Dual N-Channel MOSFET
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Repetitive Avalanche Allowed up to Tjmax
- Automotive [Q101] Qualified
- Lead-Free

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max (mΩ)	I_D
50V	130@V_{GS} = 10V	3.0A
	200@V_{GS} = 4.5V	1.5A



Top View


SO-8

Description
Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.
The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	3.0	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	2.5	
I_{DM}	Pulsed Drain Current ①	25	
P_D @T_C = 25°C	Power Dissipation③	2.4	W
	Linear Derating Factor	16	mW/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy④	22	mJ
I_{AR}	Avalanche Current①	See Fig.16c, 16d, 19, 20	A
E_{AR}	Repetitive Avalanche Energy⑥		mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	12	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

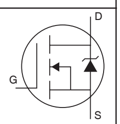
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	——	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	——	50	

07/23/07

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	50	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.057	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	130	mΩ	V_{GS} = 10V, I_D = 3.0A ②
		——	——	200		V_{GS} = 4.5V, I_D = 1.5A ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	——	3.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	3.4	——	——	S	V_{DS} = 15V, I_D = 3.0A
I_{DSS}	Drain-to-Source Leakage Current	——	——	2.0	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	25		V_{DS} = 40V, V_{GS} = 0V, T_J = 55°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	10	15	nC	I_D = 2.0A
Q_{gs}	Gate-to-Source Charge	——	1.2	——		V_{DS} = 40V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	2.8	——		V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	5.1	——	ns	V_{DD} = 25V ②
t_r	Rise Time	——	1.7	——		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	——	15	——		R_G = 6.0Ω
t_f	Fall Time	——	2.3	——		R_D = 25Ω
C_{iss}	Input Capacitance	——	255	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	69	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	29	——		ƒ = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	3.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	12		
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J = 25°C, I_S = 1.5A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	——	35	53	ns	T_J = 25°C, I_F = 1.5A
Q_{rr}	Reverse Recovery Charge	——	45	67	nC	di/dt = 100A/μs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400μs; duty cycle ≤ 2%.

③ Surface mounted on 1 in square Cu board

④ Starting T_J = 25°C, L = 4.9mH R_G = 25Ω, I_{AS} = 3.0A. (See Figure 12).

⑤ I_{SD} ≤ 2.0A, di/dt ≤ 155A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

⑥ Limited by T_{Jmax} , see Fig.16c, 16d, 19, 20 for typical repetitive avalanche performance.

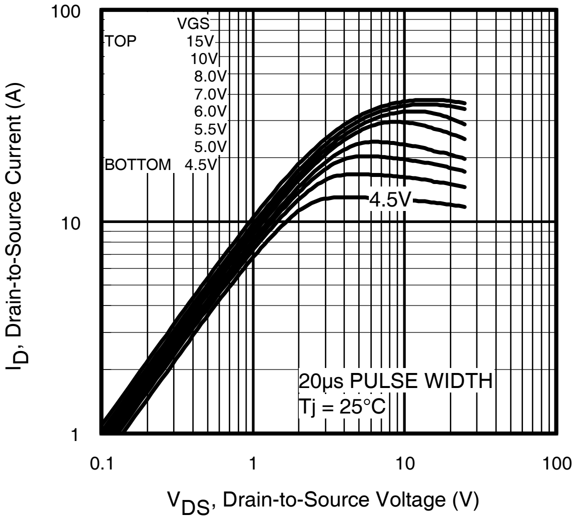


Fig 1. Typical Output Characteristics

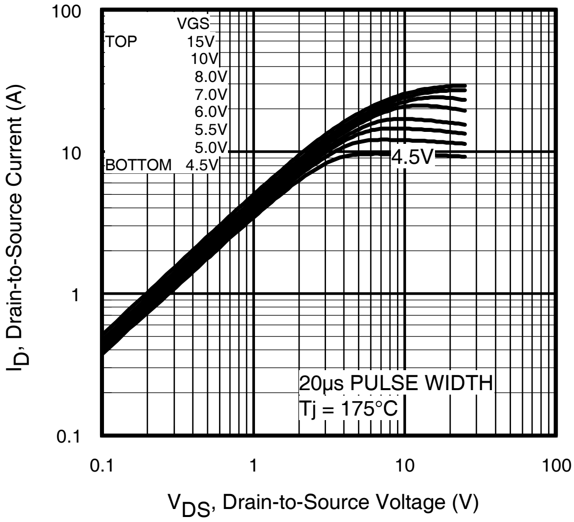


Fig 2. Typical Output Characteristics

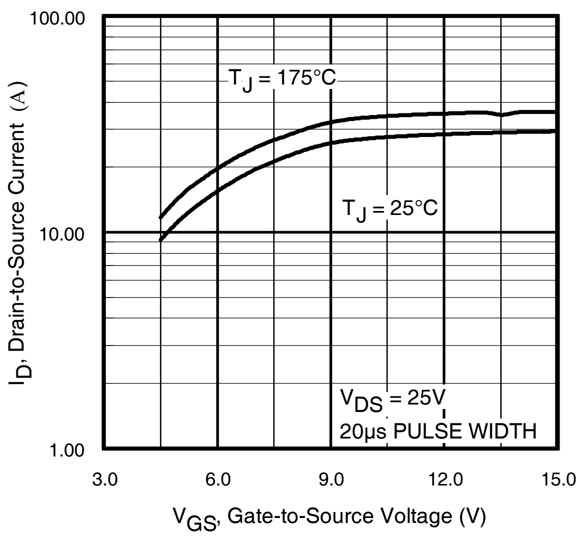


Fig 3. Typical Transfer Characteristics

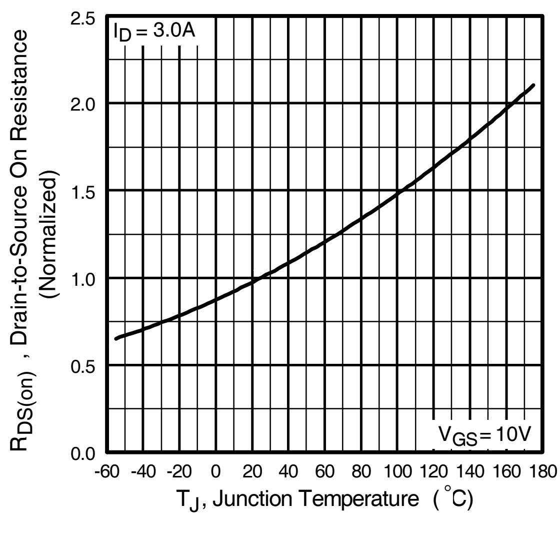


Fig 4. Normalized On-Resistance Vs. Temperature

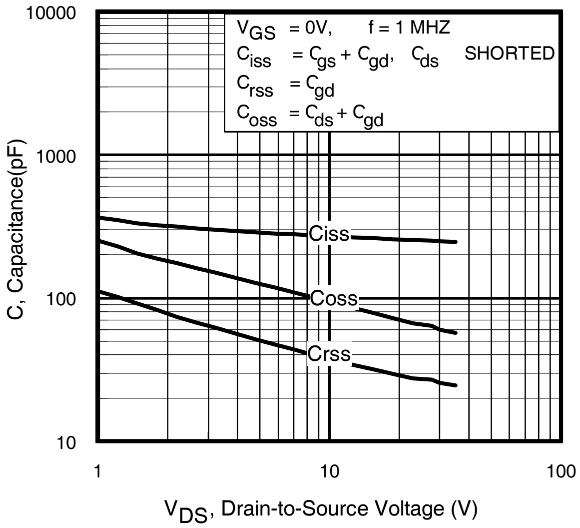


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

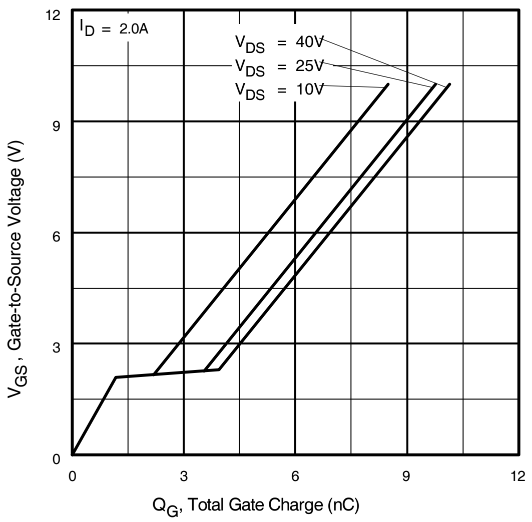


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

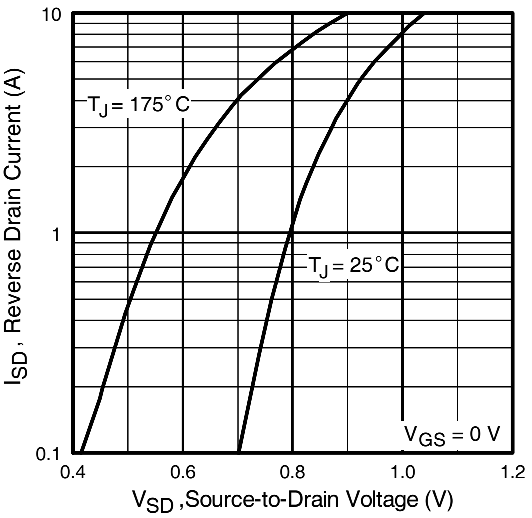


Fig 7. Typical Source-Drain Diode Forward Voltage

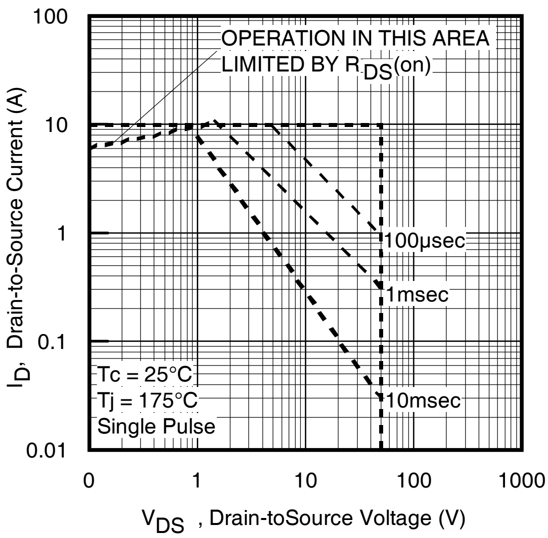


Fig 8. Maximum Safe Operating Area

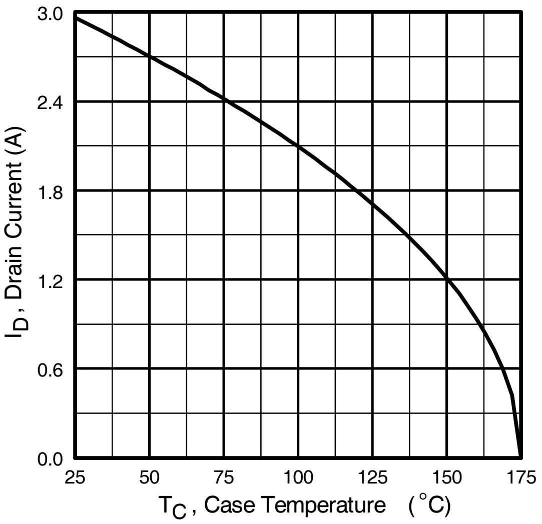


Fig 9. Maximum Drain Current Vs. Case Temperature

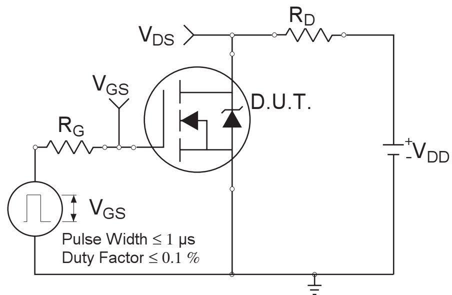


Fig 10a. Switching Time Test Circuit

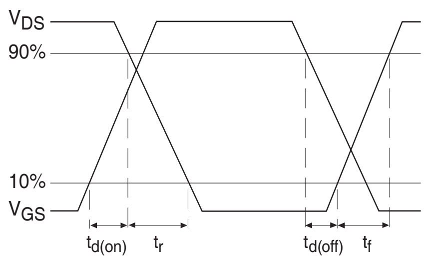


Fig 10b. Switching Time Waveforms

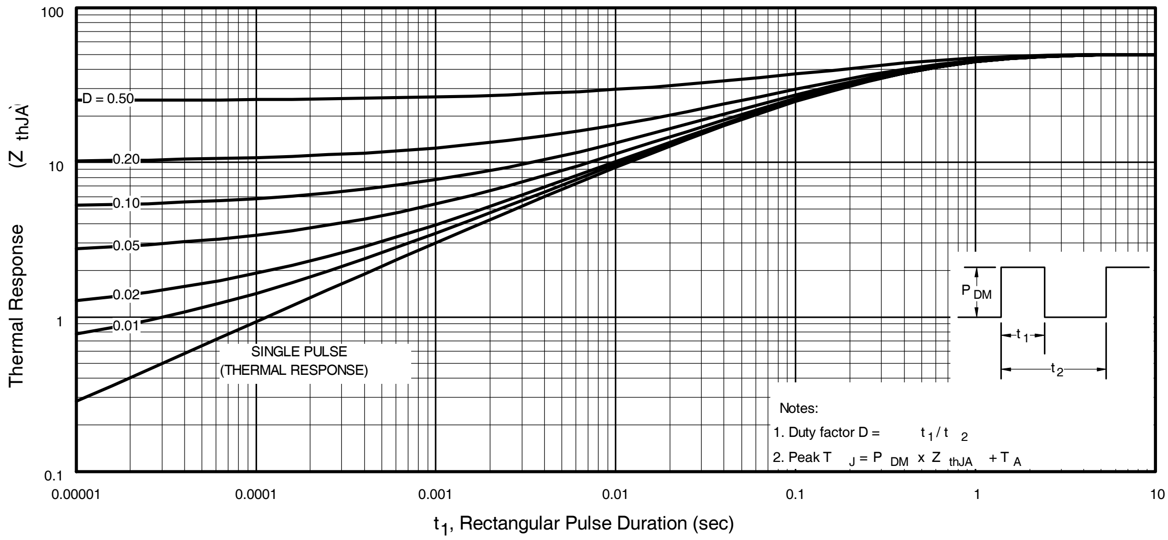


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

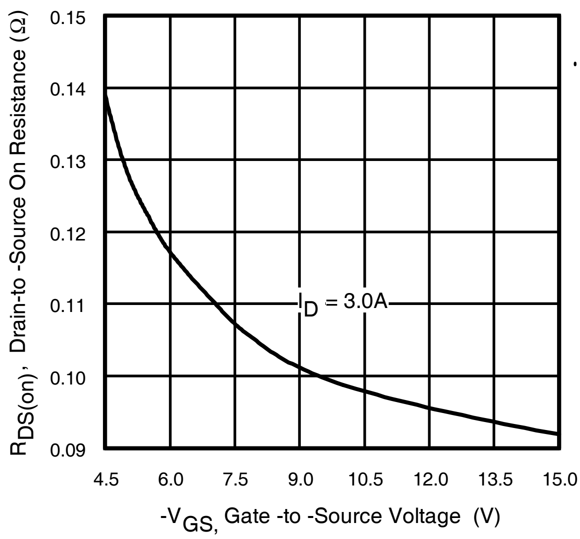


Fig 12. Typical On-Resistance Vs. Gate Voltage

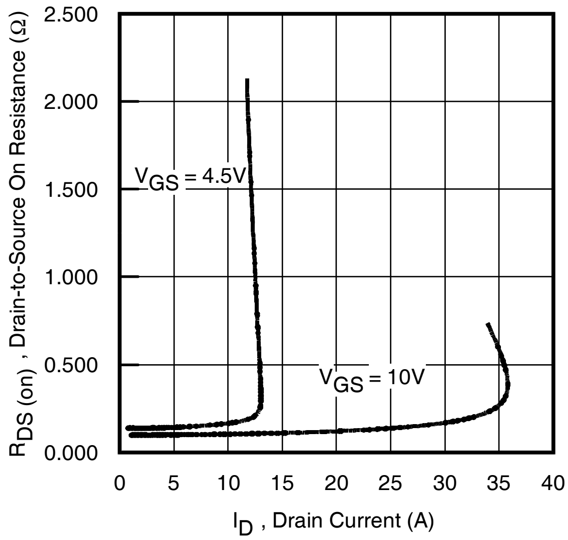


Fig 13. Typical On-Resistance Vs. Drain Current

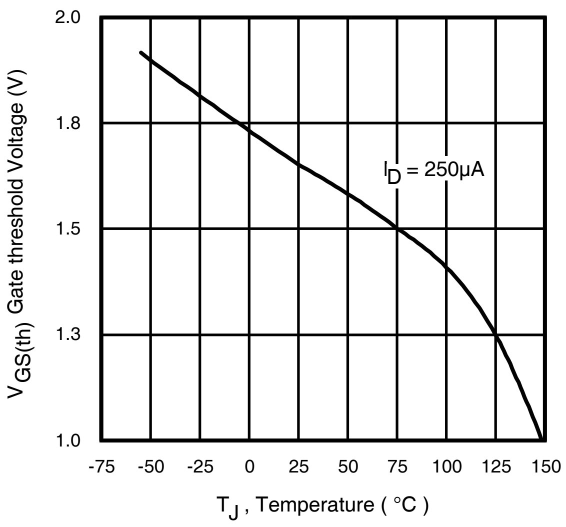


Fig 14. Typical Threshold Voltage Vs. Junction Temperature

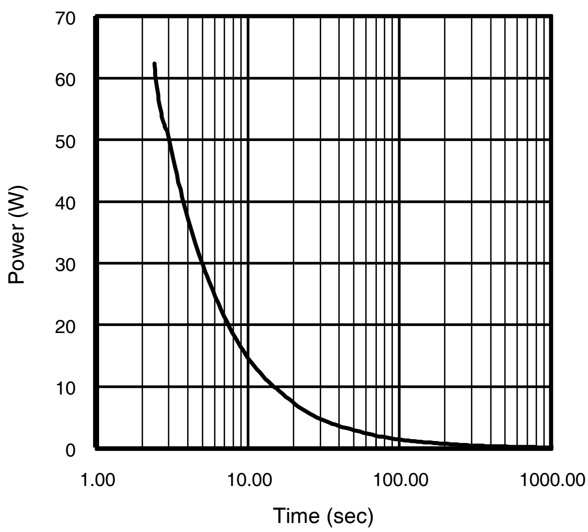


Fig 15. Typical Power Vs. Time

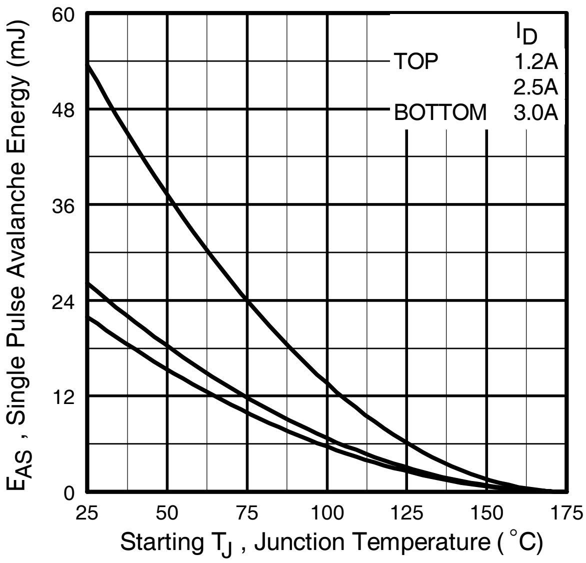


Fig 16a. Maximum Avalanche Energy Vs. Drain Current

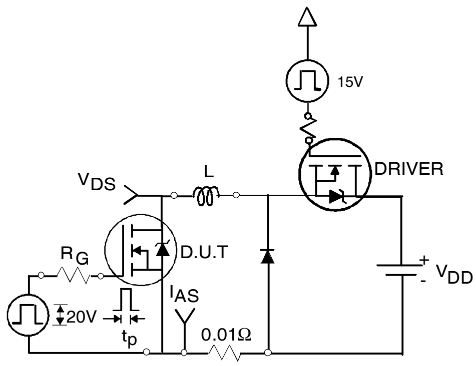


Fig 16c. Unclamped Inductive Test Circuit

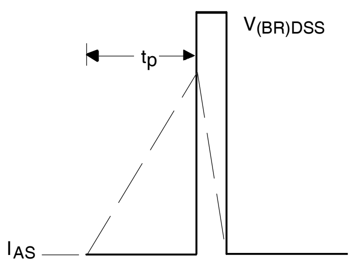


Fig 16d. Unclamped Inductive Waveforms

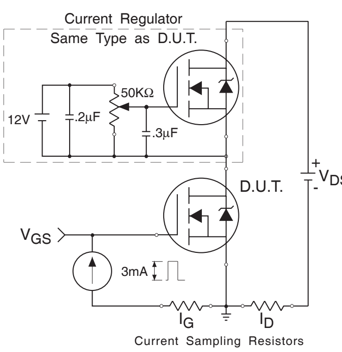


Fig 17. Gate Charge Test Circuit

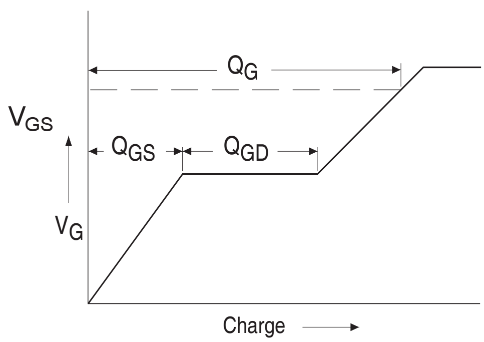


Fig 18. Basic Gate Charge Waveform

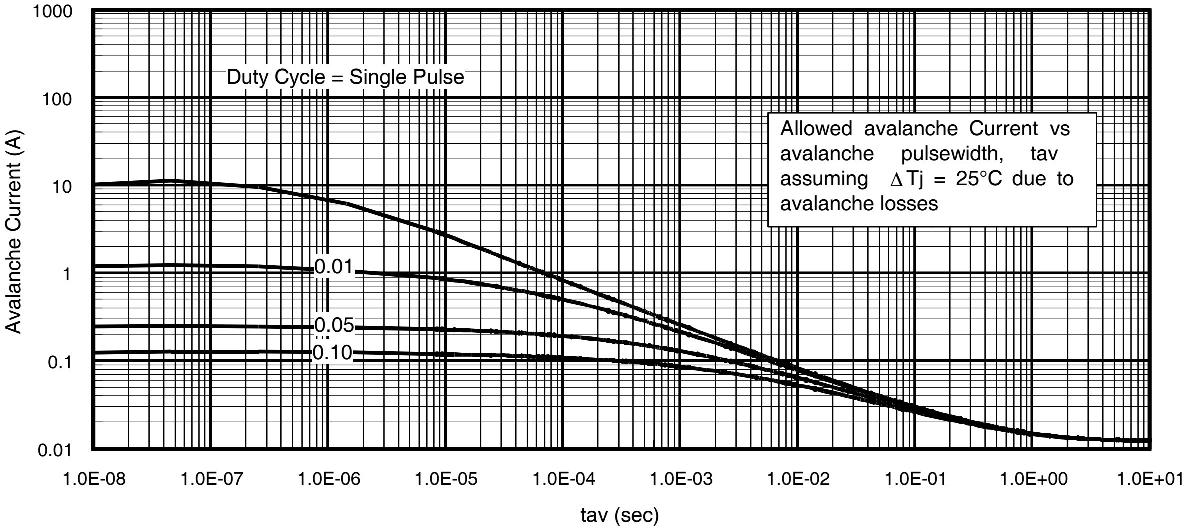


Fig 19. Typical Avalanche Current Vs.Pulsewidth

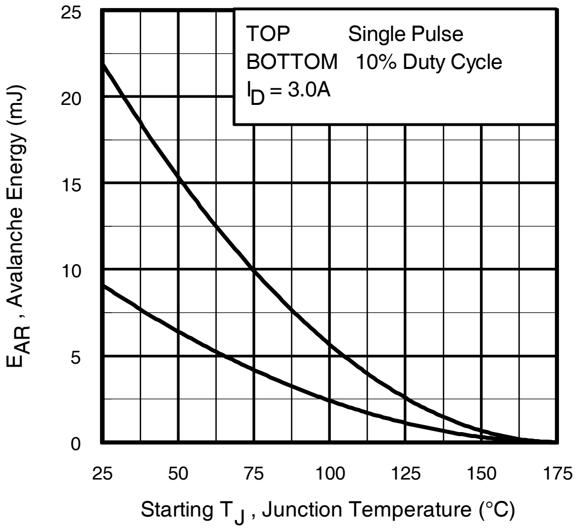


Fig 20. Maximum Avalanche Energy Vs. Temperature

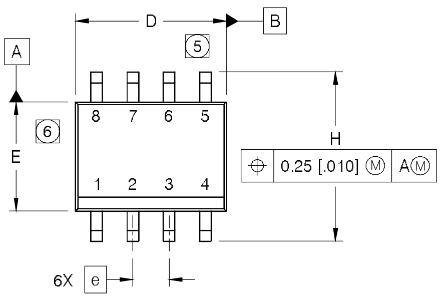
Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

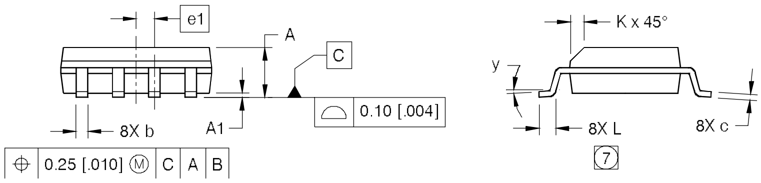
$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

SO-8 Package Outline

Dimensions are shown in millimeters (inches)



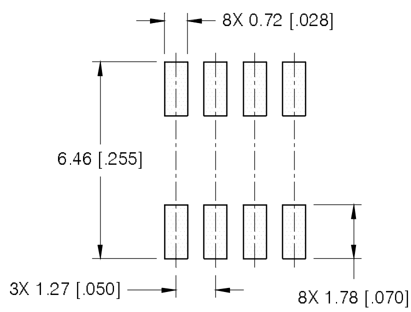
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

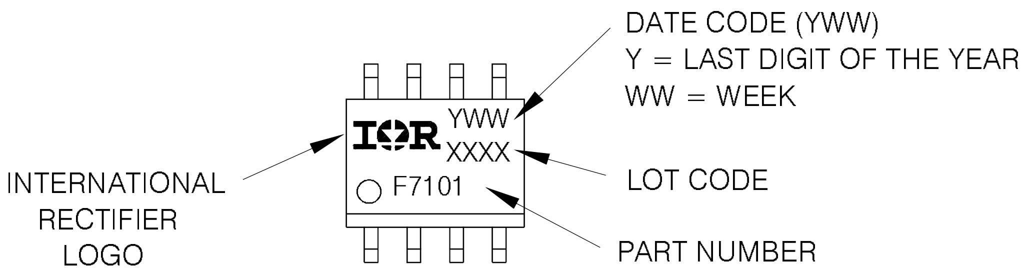
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



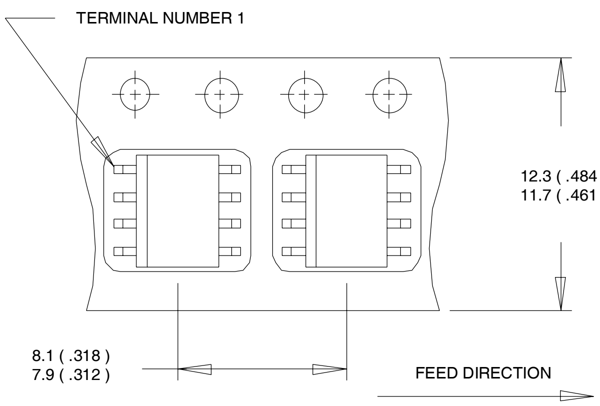
SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

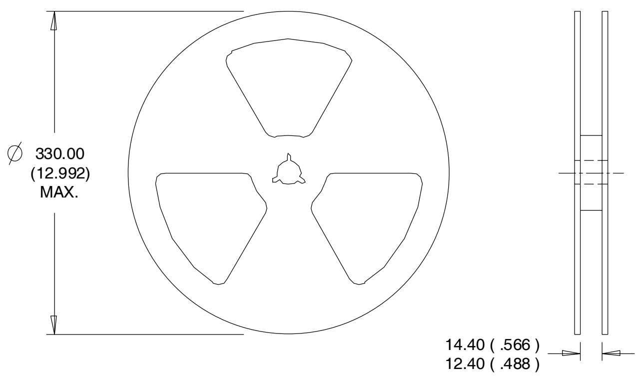


Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

SO-8 Tape and Reel



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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