PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS855011

## LOW SKEW, 1-TO-2 DIFFERENTIAL-TO-2.5V/3.3V CML FANOUT BUFFER



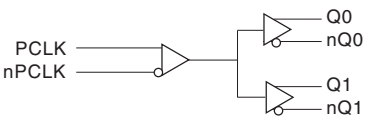
## GENERAL DESCRIPTION

The ICS855011 is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V CML Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS855011 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS855011 ideal for those clock distribution applications demanding well defined performance and repeatability.

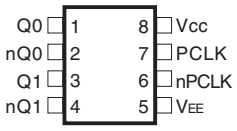
## FEATURES

- 2 differential 2.5V/3.3V CML outputs
- 1 differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >3GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 5ps (typical)
- Part-to-part skew: TBD
- Propagation delay: 242ps (typical)
- Operating voltage supply range: $V_{CC}$ = 2.375V to 3.8V, $V_{EE}$ = 0V
- -40°C to 85°C ambient operating temperature

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS855011**
**8-Lead SOIC**
3.90mm x 4.90mm x 1.37mm package body
**M Package**
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. CML interface levels. |
| 3, 4 | Q1, nQ1 | Output | | Differential output pair. CML interface levels. |
| 5 | $V_{EE}$ | Power | | Negative supply pin. |
| 6 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 7 | PCLK | Input | Pulldown | Non-inverting LVPECL differential clock input. |
| 8 | $V_{CC}$ | Power | | Positive supply pin. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 75 | | KΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 75 | | KΩ |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V (CML mode, $V_{EE}$ = 0) |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5 V |
| Outputs, $I_O$ | |
| Continuous Current | 20mA |
| Surge Current | 40mA |
| Operating Temperature Range, TA | -40°C to +85°C |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient) | 112.7°C/W (0 lfpm) |

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC}$ = 2.375V TO 3.8V; $V_{EE}$ = 0V

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 2.375 | 3.3 | 3.8 | V |
| $I_{EE}$ | Power Supply Current | | | 50 | | mA |

**TABLE 3B. LVPECL DC CHARACTERISTICS,** $V_{CC}$ = 2.375V TO 3.8V; $V_{EE}$ = 0V

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | PCLK | $V_{CC} = V_{IN}$ = 3.8V | | | 150 | µA |
| | | nPCLK | $V_{CC} = V_{IN}$ = 3.8V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | PCLK | $V_{CC}$ = 3.8V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nPCLK | $V_{CC}$ = 3.8V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.3 | | 1 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is $V_{CC}$ + 0.3V.

**TABLE 3C. CML DC CHARACTERISTICS,** $V_{CC}$ = 2.375V TO 3.8V; $V_{EE}$ = 0V

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ - 0.020 | $V_{CC}$ - 0.010 | $V_{CC}$ | V |
| $V_{OUT}$ | Output Voltage Swing | | 325 | 400 | | mV |
| $V_{DIFF\_OUT}$ | Differential Output Voltage Swing | | 650 | 800 | | mV |
| $R_{OUT}$ | Output Source Impedance | | 40 | 50 | 60 | Ω |

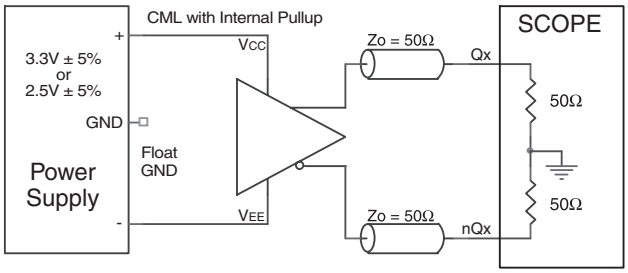
NOTE 1: Outputs terminated with 100Ω across differential output pair.

**TABLE 4. AC CHARACTERISTICS,** $V_{CC}$ = 0V; $V_{EE}$ = -3.8V TO -2.375V OR $V_{CC}$ = 2.375 TO 3.8V; $V_{EE}$ = 0V

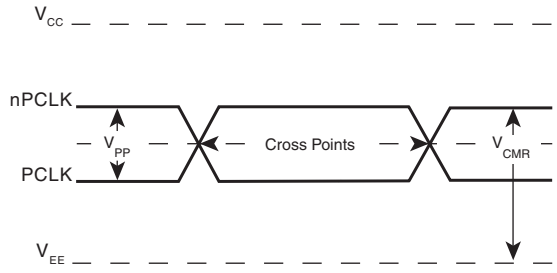
| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | >3 | | GHz |
| $t_{PD}$ | Propagation Delay; (Differential); NOTE 1 | | | 242 | | ps |
| *t*sk(o) | Output Skew; NOTE 2, 4 | | | 5 | | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | TBD | | ps |
| $t_R$/$t_F$ | Output Rise/Fall Time | 20% to 80% | | 140 | | ps |
| odc | Output Duty Cycle | | | 50 | | ps |

All parameters characterized at ≤ 1GHz unless otherwise noted.
$R_L$ = 100Ω after each output pair.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

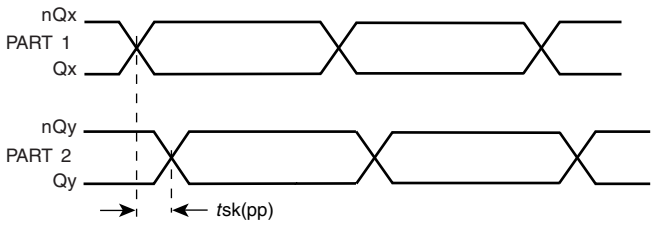
# PARAMETER MEASUREMENT INFORMATION



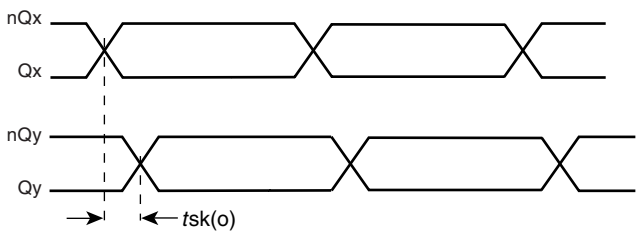

## OUTPUT LOAD AC TEST CIRCUIT



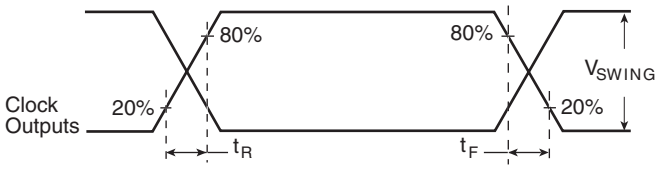

## DIFFERENTIAL INPUT LEVEL



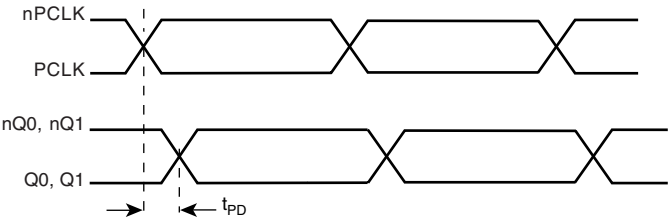

## PART-TO-PART SKEW



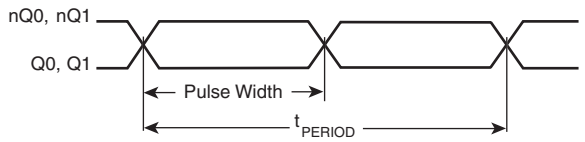

## OUTPUT SKEW




## OUTPUT RISE/FALL TIME




## PROPAGATION DELAY




$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

## OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

# APPLICATION INFORMATION

## WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 1* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

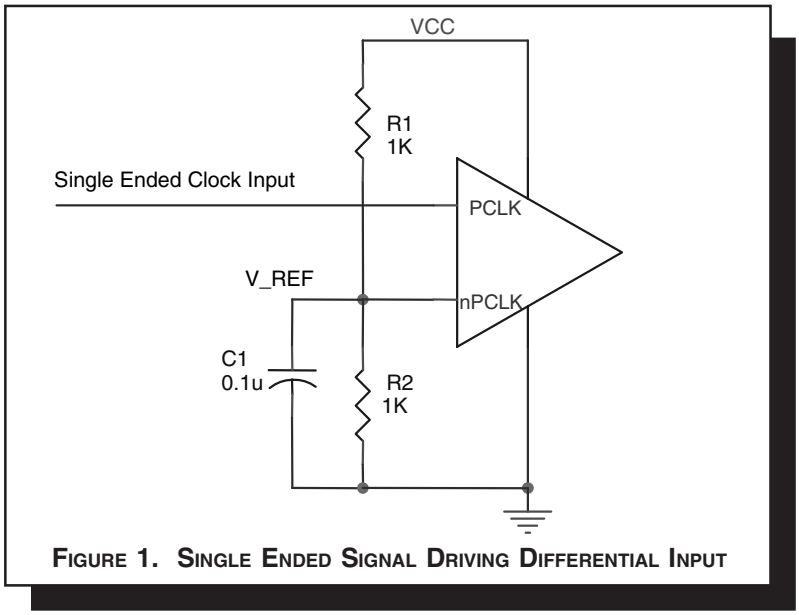



FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

## LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both $V_{SWING}$ and $V_{OH}$ must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

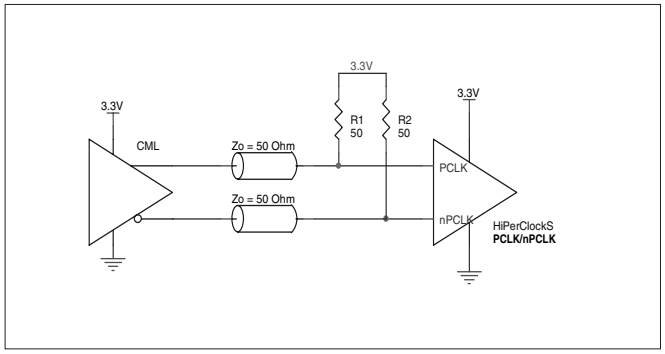



**FIGURE 2A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN OPEN COLLECTOR CML DRIVER**

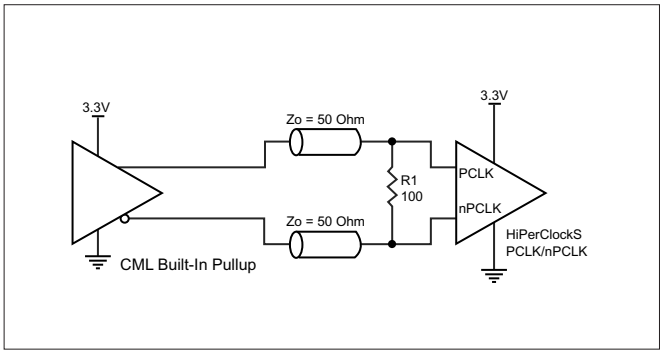



**FIGURE 2B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**

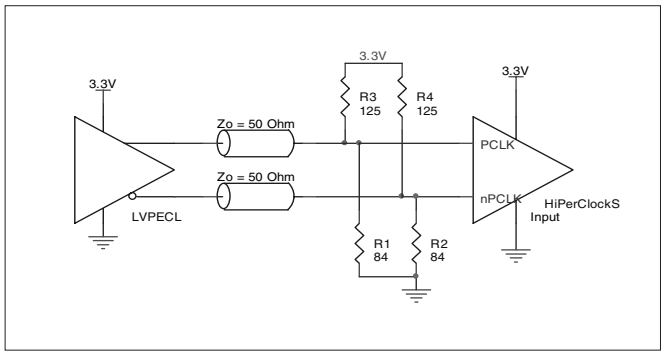



**FIGURE 2C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**

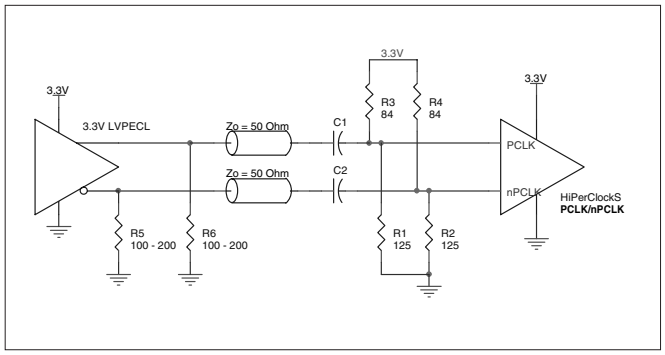



**FIGURE 2D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**

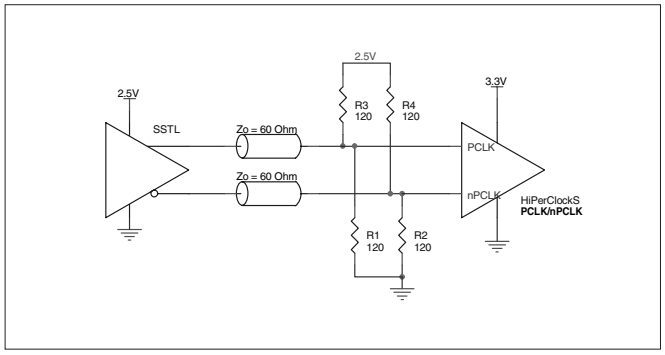



**FIGURE 2E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**

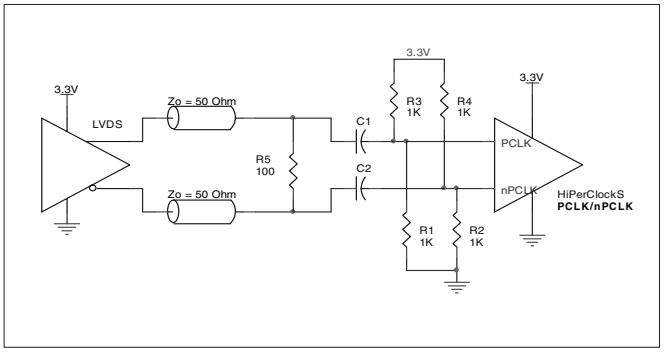



**FIGURE 2F. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**

# RELIABILITY INFORMATION

**TABLE 6. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | 0 | 200 | 500 |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS855011 is: 109

## PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

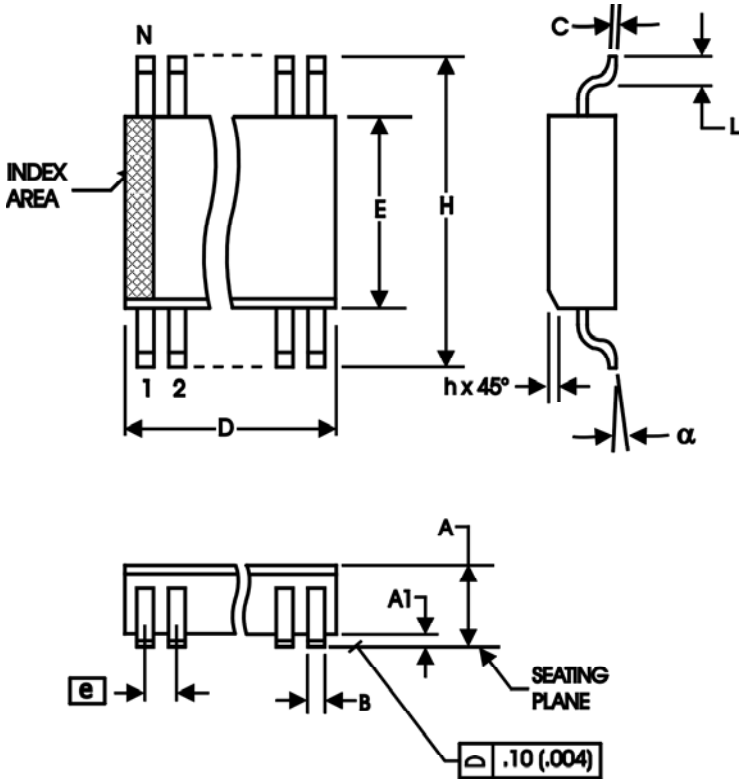



**TABLE 7. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | MINIMUN | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Reference Document: JEDEC Publication 95, MS-012

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS855011AM | 855011A | 8 lead SOIC | 96 per tube | -40°C to 85°C |
| ICS855011AMT | 855011A | 8 lead SOIC on Tape and Reel | 2500 | -40°C to 85°C |