For DSC/TABLET/Mobile Phones

USB Switching Charger IC Integrating a USB Adapter Automatic Detection Function

BD7168GU

● Overview

● High-efficient step-down switching charger IC integrating a USB adapter automatic detection function, a 28V OVP, and a 40-mΩ Pch-FET between SYSTEM and Battery for single-cell Li-ion Batteries for mobile appliances

● Features

- A 28V OVP and a controller of protection for minus voltage are integrated.
- A USB adapter automatic detection function based on D+ and D- detection is integrated.
- Set values can be changed via I2C communication.
- A 1-MHz synchronous current-mode step-down DC/DC converter, which permits small external parts to be attached, is integrated.
- The USB input current limit can be set at 100 mA, 500 mA, 900 mA, or 1500 mA with I2C and an external terminal.
- A current detection register is integrated, and external FETs and diodes are not required.
- The switch between SYSTEM and VBAT contains a 40-mΩ Pch FET.
- A battery assist function is integrated, which automatically supplied electric power from the battery in case of insufficient USB input electric power.
- A ultra-miniature WL-CSP is adopted, which measures 3.2 x 3.2 mm and has a 0.5-mm pitch.

● Application

- Digital still cameras, tablet PC, mobile phones, smart cell phones

● Application c

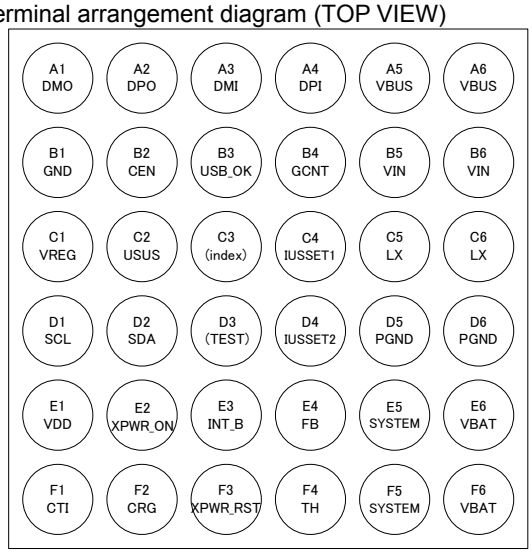
● **Package**

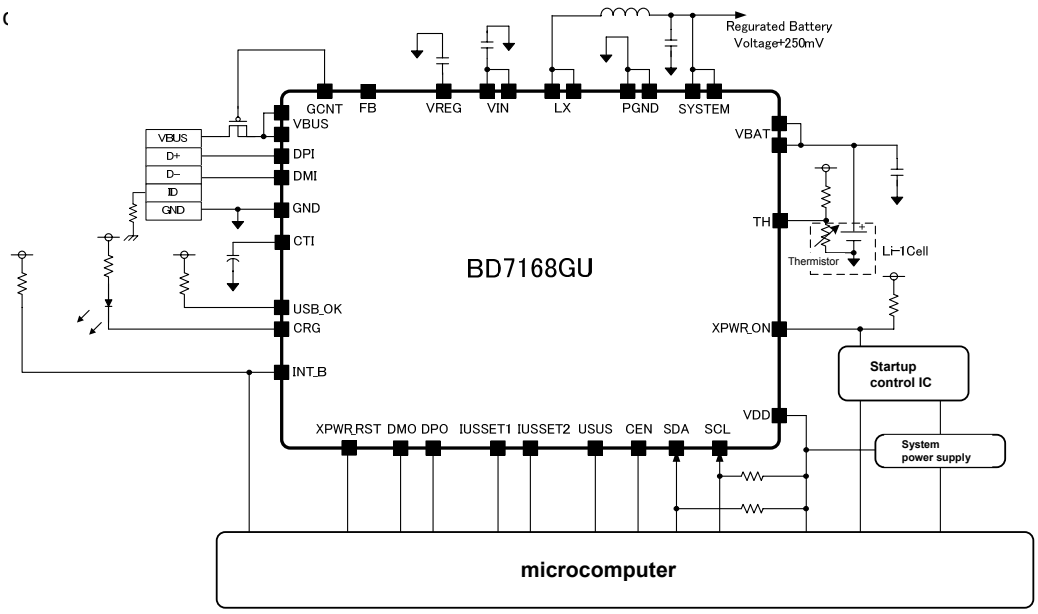
- VCSP85H3 3.20mm x 3.20mm x 1.0mm

● Operation conditions

- Input voltage range; 3.895～6.0V
- Output voltage range; 0～5.5V
- Output current; 2.0A(max)
- Switching frequency; 1.0MHz(typ.)
- High-side FET(Pch)ON resistance; 125mΩ(typ.)
- Low-side FET(Nch)ON resistance; 100mΩ(typ.)

● Terminal arrangement diagram (TOP VIEW)



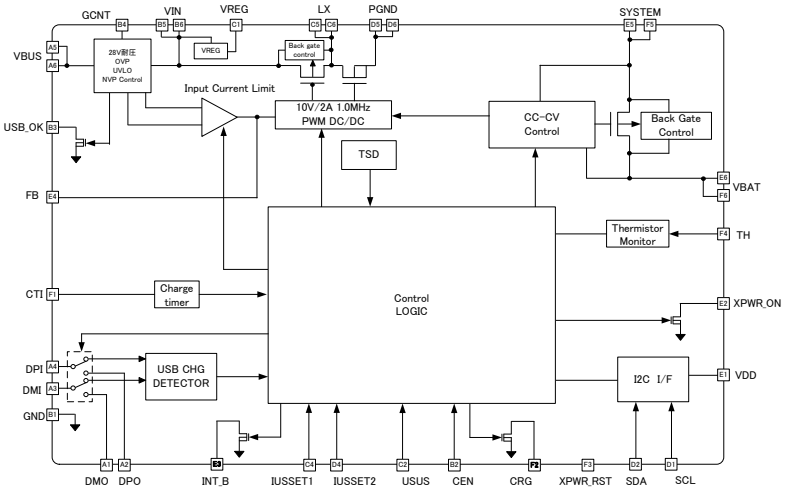


○Product structure : Silicon monolithic integrated circuit ○This product is not designed

About this document

The Japanese version of this document is the formal data sheet. If you find differences from the Japanese data sheet, please have priority over this data sheet.

● **Block diagram**



● Description of terminals

No	Symbol	Description	State of terminal When unused
A5,A6	VBUS	USB supply voltage terminal.VBUS can supply 1.42A(max) to SYSTEM.VBUS current limit is selected by DP, DM I2C or external terminal regarding to power supply you use.	OPEN
B5,B6	VIN	DC/DC input terminal. Please connect capacitance(4.7μF) between VIN and GND.	OPEN
C1	VREG	Internal power supply output terminal. Please connect capacitance(1μF) between VREG and GND.	Capacitor
C5、C6	LX	DC/DC inductor connection terminal.Please connect inductor between LX and SYSTEM.	OPEN
D5,D6	PGND	Power ground terminal	GND
E5,F5	SYSTEM	System power supply output terminal.When VBAT < 3.0V ,SYSTEM voltage is kept 3.25V.In case of 3.0V<VBAT<4.2V , SYSTEM voltage is VBAT+250mV. Please connect capacitor (10μ F) between SYSTEM and GND.	Capacitor
E6,F6	VBAT	Battery connection terminal.Please connects to Li+ battery of one cell. When you use a normal power supply, battery is charged from SYSTEM. If VBUS dosen't exist or SYSTEM current is over the input current limits,VBAT supply current to SYSTEM.	-
F4	TH	Thermistor connection terminal for battery temperature detection. Please connect thermistor (NTC) between TH and GND. Please connect resistance (equal to resistance of thermistor at 25℃) between TH and VREG. If thermistor resistance value is over the limit of the high temperature or low temperature, charge stops. If TH is connected GND, the temperature sensor of thermistor is DISENABLE.	GND
B2	CEN	Charge enable input terminal.If you connect CEN to GND, charge of battery is ENABLE. And in case of CEN at high, charge of battery is DISENABLE.	OPEN or GND
C2	USUS	USB suspend input terminal. If USUS is high, charge stops.	OPEN or GND
F2	CRG	Charge state output terminal (open drain)	OPEN or GND
F3	XPWR_RST	This terminal stops the system startup pulse output.	OPEN or GND
F1	CTI	Cap connection terminal for charge timer clock.Please connect capacitor (1000pF) between CTI and GND.	Capacitor
C4	IUSSET1	Input current limit/control terminals.If IUSSET1,2 are L, current limit of USB is 90mA. In case of IUSSET1=H , IUSSET2=L, the current limit is 480mA.In case of IUSSET1=L, IUSSET2=H ,the current limit is 860mA. And, in case of IUSSET1, 2=H, the current limit is 1420mA.	OPEN or GND
D4	IUSSET2		
B1	GND	Ground terminal.GND is ground connection for inner circuit...	GND
E2	XPWR_ON	Pulse output terminal for USB input detection. If VBAT is over 3.2V, 400msec pulse is generated.	OPEN or GND
A4	DPI	USB D+ signal input terminal	OPEN or GND
A3	DMI	USB D- signal input terminal	OPEN or GND
A2	DPO	USB D+ signal output terminal	OPEN or GND
A1	DMO	USB D- signal output terminal	OPEN or GND
E1	VDD	Power supply terminal for I2C	GND
D2	SDA	Data input/output terminal for I2C	GND
D1	SCL	Clock input terminal for I2C	GND
E4	FB	DC/DC feedback output terminal	OPEN
B3	USB_OK	USB power state output terminal (open drain) When a normal power supply is detected, output of open drain is L.	OPEN or GND
E3	INT_B	Interrupting signal terminal	OPEN or GND
B4	GCNT	External PMOS gate control terminal	OPEN or GND
D3	TEST	TEST terminal. Please use in open state.	OPEN

● Absolute maximum rating (Ta = 25℃)

Item	Symbol	Rated value	Unit	Comment
Supply voltage	VBUS	-0.3～28	V	
	VIN	-0.3～10		
	SYSTEM	-0.3～7		
	LX	-0.3～10		
	VBAT	-0.3～7		
	VDD	-0.3～4.5		
Control input terminal	CEN,USUS,IUSSET1,2, DPI,DMI, DPO,DMO,TH, XPWR_RST	-0.3～7	V	
	GCNT	-1.0～28		
I2C input terminal	SCL,SDA	-0.3～4.5	V	
Output terminal	CRG,XPWR_ON,USB_OK INT_B	-0.3～7	V	
Power dissipation (Ta≦25℃)	Pd	1.25 *1	W	
Operating temperature range	Topr	-30～+85	℃	
Storage temperature range	Tstg	-55～+125	℃	
Junction temperature	Tjmax	150	℃	

*1 When a 50 × 50 × 1.75-mm four-layer substrate made of glass epoxy is implemented (Ta = 25℃)

● Operation conditions

Item	Symbol	Standard value			Unit
		MIN	TYP	MAX	
Supply voltage	VBUS	3.42	-	6.0	V
	VBAT	-	-	4.35	V
	VDD	1.5	-	3.6	V
Control input terminal	CEN,USUS IUSSET1,2, DPI,DPO DMI,DMO TH, XPWR_RST	-0.3	-	5.5	V
I2C INPUT TERMINAL	SCL SDA	-0.3	-	3.6	V
Output terminal	CRG INT_B USB_OK, XPWR_ON	-0.3	-	5.5	V

■ **Entire system**

● Electric characteristics (VBUS = 5.0 V, VBAT = 3.6 V, and Ta = 25℃unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
【Entire system】						
VBAT leakage current 1	IBAT_L1	-	0.05	1	μA	USB OPEN 時
VBAT leakage current 2	IBAT_L2	-	10	20	uA	CHARGE Disenable
VBUS leakage current	IBUS_L	-	1.5	2.5	mA	USB SUSPEND
VREG output voltage	VREG	3.1	3.225	3.35	V	IVREG=1mA
VREG UVLO detection voltage	VREG_UVLO	2.375	2.5	2.625	V	VREG↓detection
VREG UVLO hysteresis	VREG_UVLO_hys	50	100	200	mV	VREG↑detection
VREG UVLOD detection voltage	VREG_UVLOD	1.8	1.9	2.0	V	VREG↓detection
VREG UVLOD hysteresis	VREG_UVLOD_hys	50	100	200	mV	VREG↑detection
INT_B output Low voltage	VINT_L	-	-	0.4	V	IINT_B = 5mA
INT_B leakage current	IINT_L	-	-	1	μA	VINT_B = 5V
【Control unit】						
IUSET1,2 control voltage L	VUSET_L	-	-	0.4	V	
IUSET1,2 control voltage H	VUSET_H	1.6	-	-	V	
CEN control voltage L	VCEN_L	-	-	0.4	V	CHARGE Enable
CEN control voltage H	VCEN_H	1.6	-	-	V	CHARGE Disenable
USUS control voltage L	VUSUS_L	-	-	0.4	V	CHARGE Enable
USUS control voltage H	VUSUS_H	1.6	-	-	V	CHARGE Disenable
XPWR_RST control voltage L	VXPWRR_L	-	-	0.4	V	
XPWR_RST control voltage H	VXPWRR_H	1.6	-	-	V	

■ **OVP unit**

● Electric characteristics (VBUS = 5.0 V, VBAT = 3.6 V, and Ta = 25℃ unless otherwise specified)

Item	Symbol	Standard value			Standard value	Standard value
		Minimum	Minimum	Minimum		
【OVP unit】						
VBUS UVLO detection voltage	VBUS_UVLO	3.52	3.7	3.88	V	VBUS↓detection
VBUS UVLO hysteresis	VBUS_UVLOhys	150	200	250	mV	VBUS↑detection
VBUS OVP detection voltage	VBUS_OVP	5.7	5.85	6.0	V	VBUS↑detection
VBUS OVP hysteresis	VBUS_OVPhys	50	100	150	mV	VBUS↓detection
Output voltage startup time	TVBUS_ON	-	5	10	msec	
Output voltage OFF time	TVBUS_OFF	-	1	5	μsec	
VBUS -VIN ON resistance	RON_VBUS	60	125	250	mΩ	
VBUS-VIN leakage current	Ileak_VBUS	-	-	1	μA	VBUS→VIN leak current
USBOK output Low voltage	VUSBOK_ON	-	-	1.0	V	IUSBOK =1mA
USBOK leakage current	IUSBOKL	-	-	1	μA	
【NVP unit (A clamper for a protection of -28V PMOS VGS】						
Clamp voltage	VZ	8	11	14	V	
Pull down resistance	RPD	10	20	30	kΩ	

◎Radiation-resistant design is not adopted.

■ Charger detector / Analog SW unit

● Electric characteristics (VBUS = 5.0 V, VBAT = 3.6 V, Ta = 25℃, and CTI = 1000 pF unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
【USB charger detector】						
VDAT_SRC voltage (D+ output voltage)	VDAT_SRC	0.5	0.6	0.7	V	Io=0～200μA
RCD resistance (D+ pull-up resistance)	RCD	52	69	86	kΩ	
VDATA_REF voltage (D- detection voltage)	VDAT_REF	0.3	0.35	0.4	V	At the time of the DM terminal rise
VLGC voltage (D- detection voltage)	VLGC	1.2	1.4	1.6	V	At the time of the DM terminal rise
D- sink current	IDAT_SINK	50	100	150	μA	V(DM) = 0.6V
Detection voltage for BCS-compliant PORT (D+ detection voltage)	VTL	VBUS ×0.22	VBUS ×0.27	VBUS ×0.32	V	BCS-compliant PORT: SDP, CDP, DCP
Detection voltage for pull-up PORT(D+ detection voltage)	VTM	VBUS ×0.48	VBUS ×0.53	VBUS ×0.58	V	
DPPD resistance (D+ pull-down resistance)	VTH	VBUS ×0.75	VBUS ×0.80	VBUS ×0.85	V	Pull-up PORT: PS2, UART
VDAT_SRC voltage (D+ output voltage)	RDPPD	333	667	1000	kΩ	
【USBSW (DP, DM) unit】						
SW ON resistance	RON_USBSW	－	3	6	Ω	VIN=3.3V or 0V
Leakage current in OFF	IIOFF_USB	-3	－	3	μA	VIN=3.3V or 0V VB=OPEN
SW capacitance	CSW	－	6	－	pF	USBSW ON
USBSW startup time	TUPUSB	－	－	1	ms	USBSW OFF→ON

◎Radiation-resistant design is not adopted.

■ **DC/DC unit**

Recommended operation range

Item	Symbol	Standard value			Unit
		MIN	TYP	MAX	
Power voltage	VIN	-	5	10	V
External circuit constant	CVIN	2.2	4.7	-	μF
	Lx	2.2	4.7	10	μH
	CSYSTEM	2.2	4.7	10	μF
	RFB	1	4.7	10	kΩ
	CFB	0.47	1	2	μF

● Electric characteristic (VBUS = 5.0 V, VBAT = 3.6 V, and Ta = 25℃ unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
【DC/DC unit】						
VIN UVLO detection voltage	VIN_UVLO	3.14	3.36	3.58	V	VIN↓ detection
VIN UVLO hysteresis	VIN_UVLOhys	50	100	150	mV	VIN↑ detection
VBUS_VIN uvlo voltage difference	DiffUVLO	160	-	-	mV	VBUS_UVLO-VIN_UVLO Voltage defference
VBUS input current limit value1	IUSB1	80	90	100	mA	IUSSET1="L",IUSSET2="L"
VBUS input current limit value2	IUSB2	460	480	500	mA	IUSSET1="H",IUSSET2="L"
VBUS input current limit value3	IUSB3	650	690	730	mA	IUSSET[2:0]=03h
VBUS input current limit value4	IUSB4	820	860	900	mA	IUSSET1="L",IUSSET2="H"
VBUS input current limit value5	IUSB5	1340	1420	1500	mA	IUSSET1="H",IUSSET2="H"
Minimum system output voltage	VSYS_MIN	VREG-0.015	VREG+0.025	VREG+0.065	V	When VBAT = 2.5 V
VBAT-system output voltage	VSYSdiff	210	250	290	mV	When VBAT = 3.6 V
Soft start time	Tdcdc_ss	-	4	8	msec	System rise time
High-side FET ON resistance	Ron_high	62.5	125	250	mΩ	
High-side FET leakage current	Ileak_high	-	-	1	μA	VIN→LX leak current
High-side FET reverse current	Irev_high	-	-	1	μA	LX→VIN leak current
Low-side FET ON resistance	Ron_low	50	100	200	mΩ	
Low-side FET leakage current	Ileak_low	-	-	1	μA	LX→GND leak current
Oscillation frequency	Fosc	0.9	1	1.1	MHz	
SCP timer latch time	Tscp	-	22	44	msec	
Short circuit detection voltage	VSCP	1.8	2	2.2	V	
Short circuit detection hysteresis	VSCP_hys	-	0.1	0.2	V	
High-side・FET backflow detection voltage	Vrev_hith	0	40	80	mV	Voltage difference between VIN and VBAT
REGA stop delay time	Tregstp	10	20	40	msec	REGA stop time after VBUS uvlo detection

◎Radiation-resistant design is not adopted.

● **Output voltage**

The output voltage of the DC/DC unit is shown in the figure below. When V_{BAT} < 3.0 V, V_{SYSTEM} = 3.25 V will be output. When V_{BAT} > 3.0 V, V_{BAT} + 0.25 V will be output.

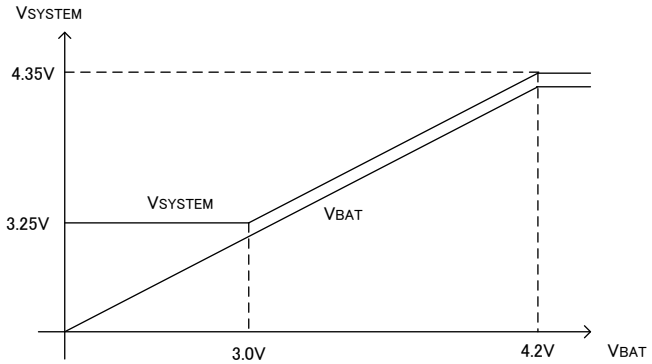


Figure 1. System output voltage

■ **Charger unit**

Recommended operation range

Item	Symbol	Standard value			Unit
		MIN	TYP	MAX	
Power voltage	SYSTEM	0	VBAT+0.25	5.5	V
	VBAT	0	-	5.5	V
External circuit constant	CTI	100	1000	10000	pF
	CRG pull-up resistance	10	100	-	kΩ
	TH pull-up resistance	-	10	-	kΩ

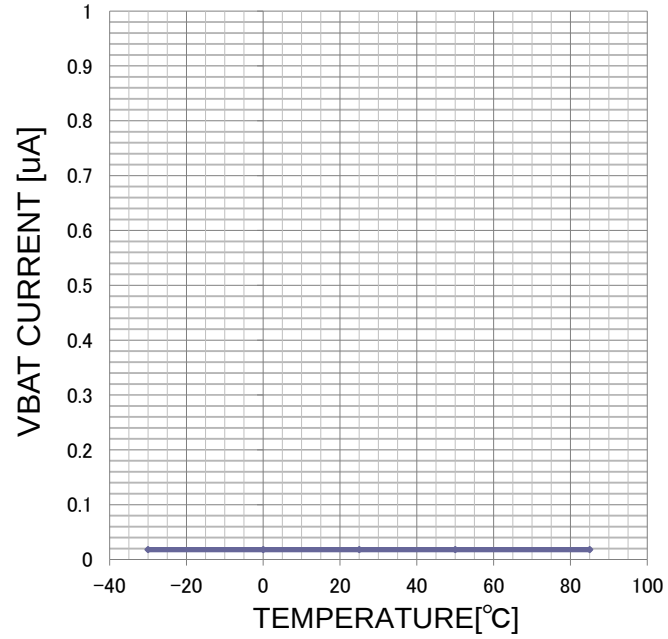
● Electric characteristics (VBUS = 5.0 V, VBAT = 3.6 V, Ta = 25℃, and CTI = 1000 pF unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
【Charger unit】						
Fast Charge Current	IBATCHG	300	400	500	mA	
Pre Charge Current	IBATPRE	36	60	84	mA	
Tricle charge current	ITRICLE	-	IBATPRE/2	IBATPRE	mA	
Tricle charge Detect Voltage	Vtricle	1.35	1.5	1.65	V	VBAT ↓ detection
Tricle charge Detect Voltage hysteresis	Vtricle_hys	50	100	200	mV	VBAT ↑ detection
Fast-charge detect voltage	VPRE	2.716	2.8	2.884	V	VBAT ↑ detection
Fast-charge hysteresis	VPREHYS	100	200	300	mV	When VBAT is lowering
Full charge voltage	VSTOP	4.170	4.2	4.230	V	IVBAT = 0mA
Charge restart voltage	VRECHG	4.05	4.1	4.15	V	When VBAT = 4.2 V
Over-voltage detection voltage	VOVP	4.3	4.35	4.4	V	
Charge termination current	ITOPOFF	60	80	100	mA	
ON resistance between SYSTEM and VBAT	RON_VBAT	20	40	60	mΩ	
Pre-charge safety timer value	TPRE	108	120	132	min	
Fast charge safety timer value	TFAST	540	600	660	min	
Temperature safety timer value	THTPRO	108	120	132	min	Time is detected at a temperature of 58℃ or over.
Fast charge safety timer value at low temperature	TLTPRO	1296	1440	1584	min	Time is detected at a temperature of 2 to 10℃ or below.
Charge end delay time	TTOPOFF	13	15	17	sec	
CRG output low voltage	VCRG_L, VFLT_L	-	-	0.4	V	ICRG = 5mA
CRG leakage current	ICRG_L, IFLT_L	-	-	1	μA	VCRG = 5V
CRG flickering frequency	TCRG	0.48	0.6	0.72	Hz	When Temp Error1,2
FLT flickering frequency	TFLG	4.8	6	7.2	Hz	When Batt Error
XPWR_ON output low voltage	VXPWR_L	-	-	0.4	V	IXPWR_ON = 5mA
XPWR_ON leakage current	IXPWR_L	-	-	1	μA	VXPWR_ON = 5V
XPWR_ON ON time	Txpwr_on	320	400	480	msec	
XPWR_ON ON output detection voltage	VTH_XPWR	3.1	3.2	3.3	V	VBAT ↑ detection
TH threshold voltage HOT1	VTH_HOT1	VREG ×0.315	VREG ×0.329	VREG ×0.344	V	When 45±2℃ detection β(25/50) = 3370 K is used
TH threshold voltage HOT2	VTH_HOT2	VREG ×0.281	VREG ×0.294	VREG ×0.308	V	When 50±2℃ detection β(25/50) = 3370 K is used
TH threshold voltage HOT3	VTH_HOT3	VREG ×0.234	VREG ×0.245	VREG ×0.256	V	When 58±2℃ detection β(25/50) = 3370 K is used
TH threshold voltage COLD1	VTH_COLD1	VREG ×0.626	VREG ×0.646	VREG ×0.665	V	When 10±2℃ detection β(25/50) = 3370 K is used
TH threshold voltage COLD2	VTH_COLD2	VREG ×0.702	VREG ×0.720	VREG ×0.738	V	When 2±2℃ detection β(25/50) = 3370 K is used
TH threshold disenable voltage	VTH_Dis	VREG ×0.02	VREG ×0.035	VREG ×0.05	V	
Battery open detection voltage	VTH_BATOPN	VREG ×0.92	VREG ×0.95	VREG ×0.98	V	

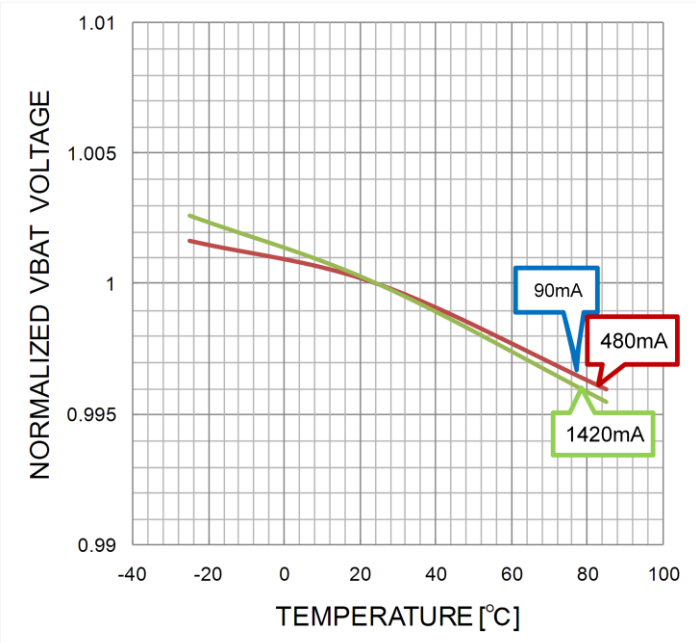
◎Radiation-resistant design is not adopted.

● Reference data

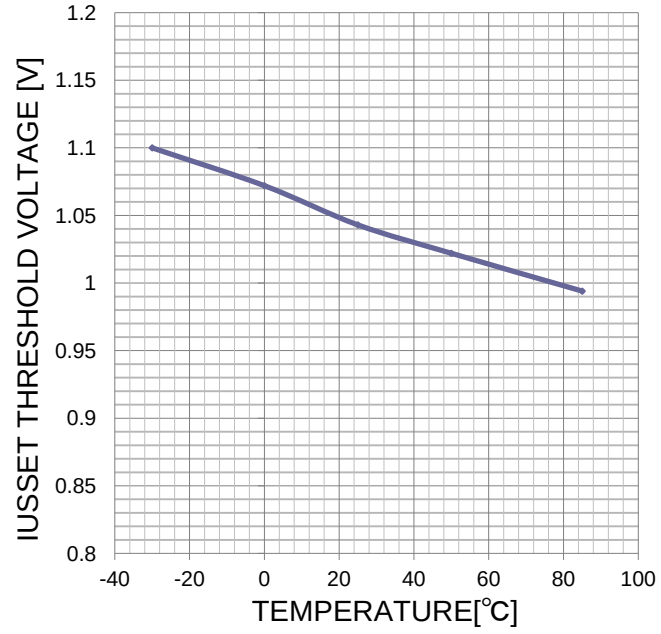
VBAT INPUT CURRENT VS. TEMPERATURE



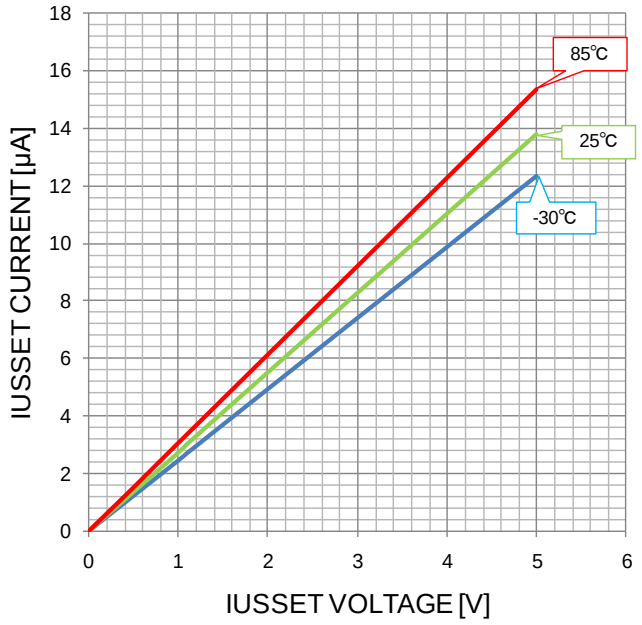
NORMALIZED FULL VOLTAGE VS. TEMPERATURE



IUSSET THRESHOLD VOLTAGE VS. TEMPERATURE

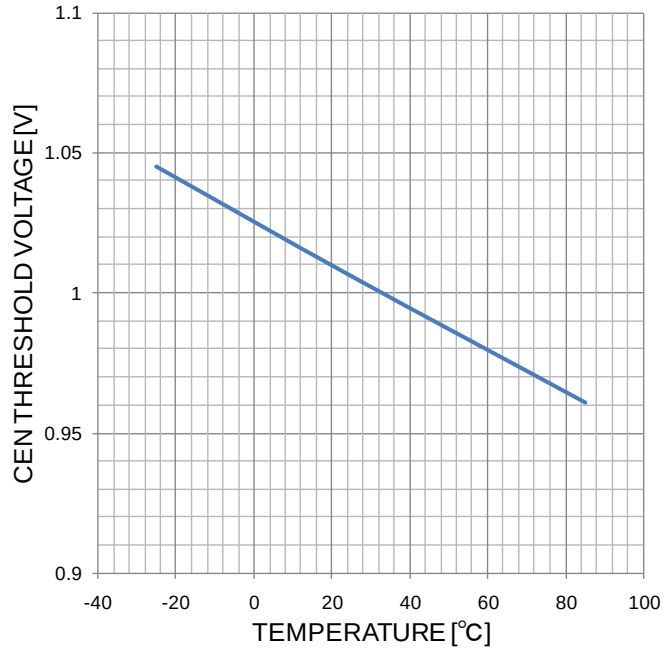


IUSSET CURRENT VS. IUSSET VOLTAGE

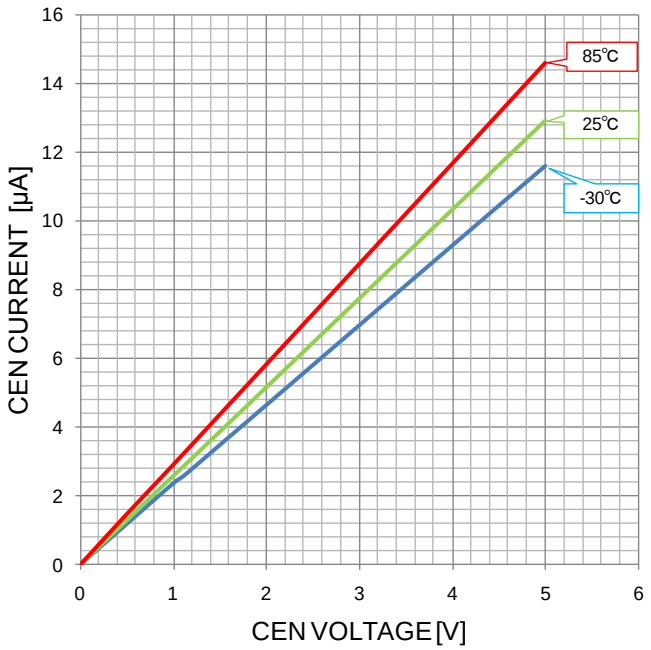


● Reference data

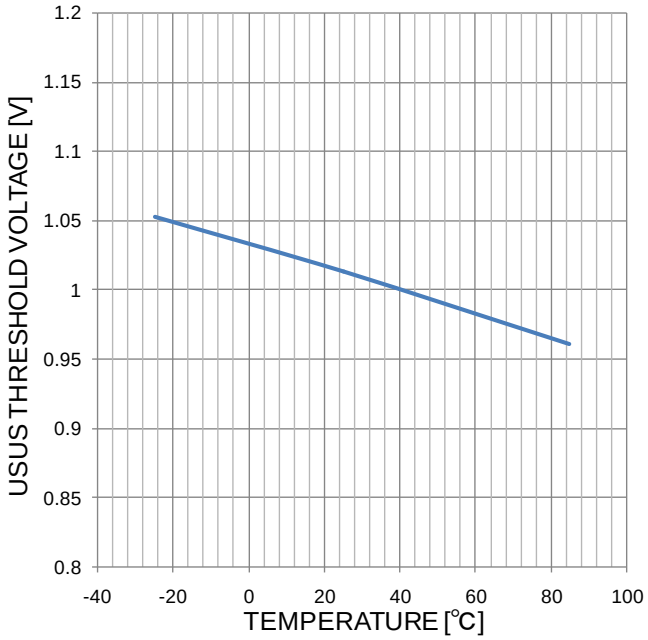
CEN THRESHOLD VOLTAGE VS. TEMPERATURE



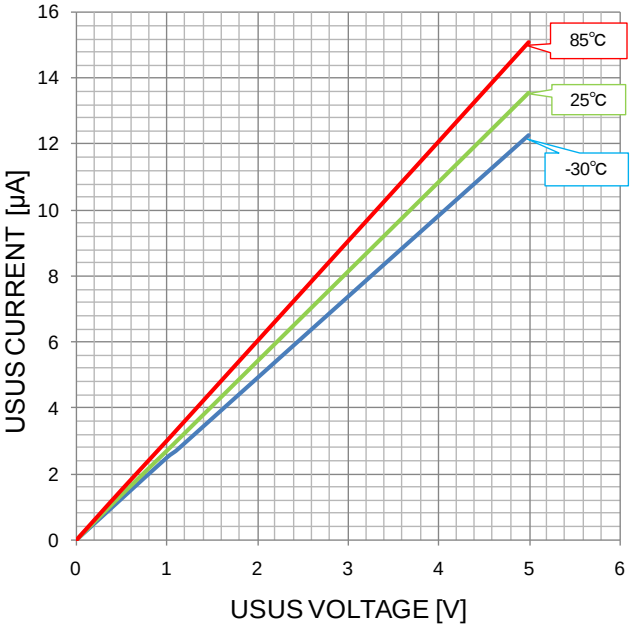
CEN CURRENT VS. CEN VOLTAGE



USUS THRESHOLD VOLTAGE VS. TEMPERATURE

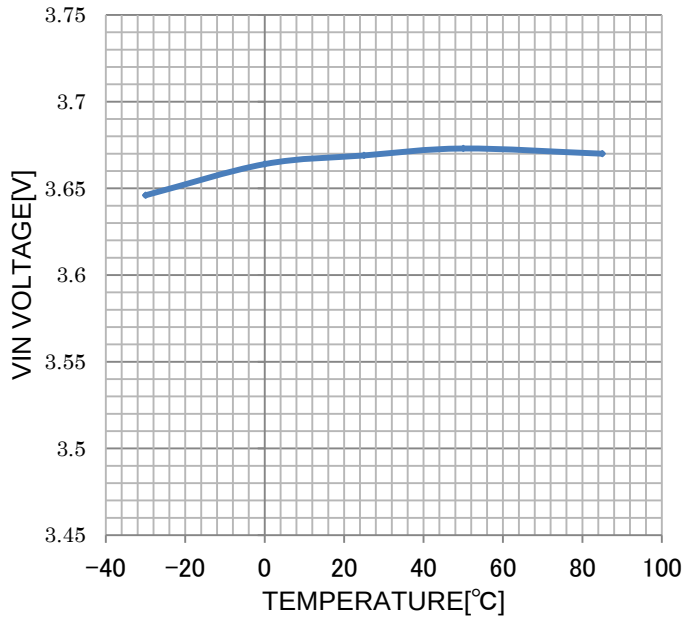


USUS CURRENT VS. USUS VOLTAGE

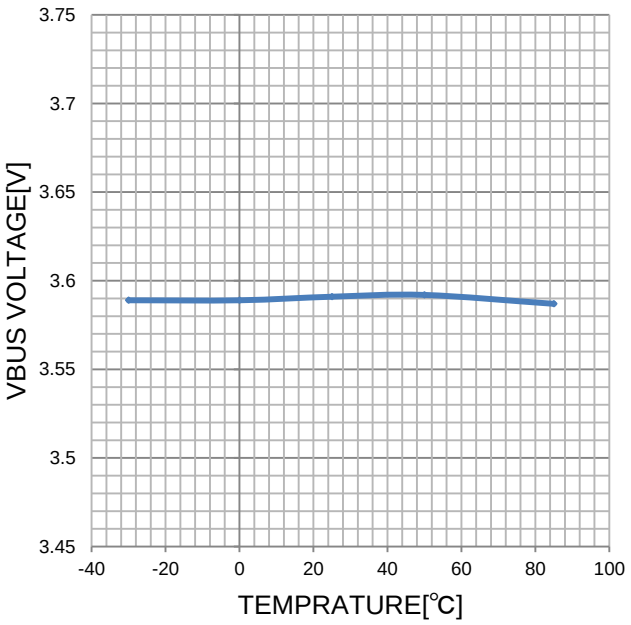


● Reference data

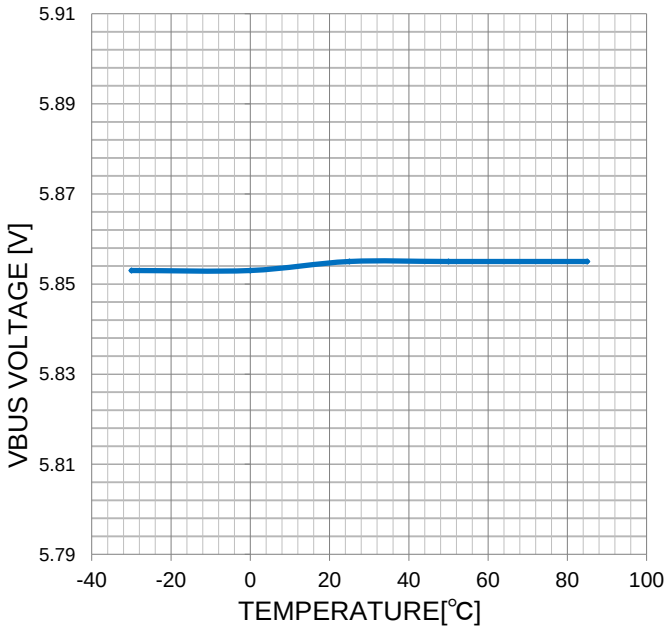
VIN_UVLO VOLTAGE VS. TEMPERATURE



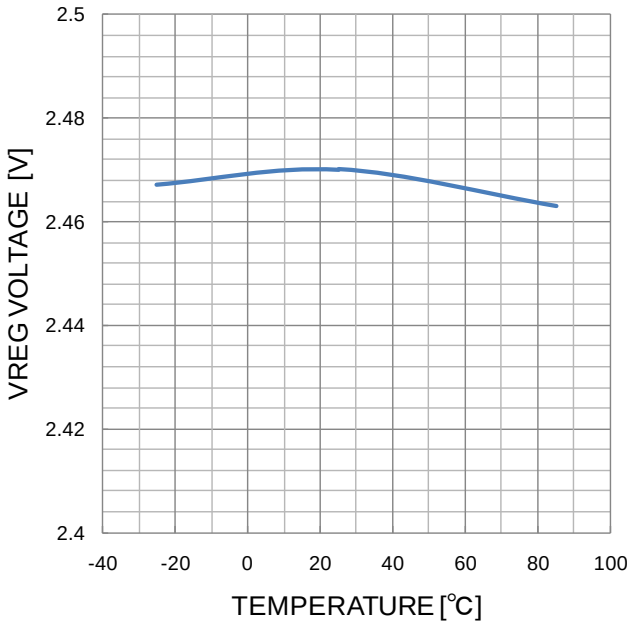
VBUS_UVLO VOLTAGE VS. TEMPERATURE



VBUS_OVP VOLTAGE VS. TEMPERATURE

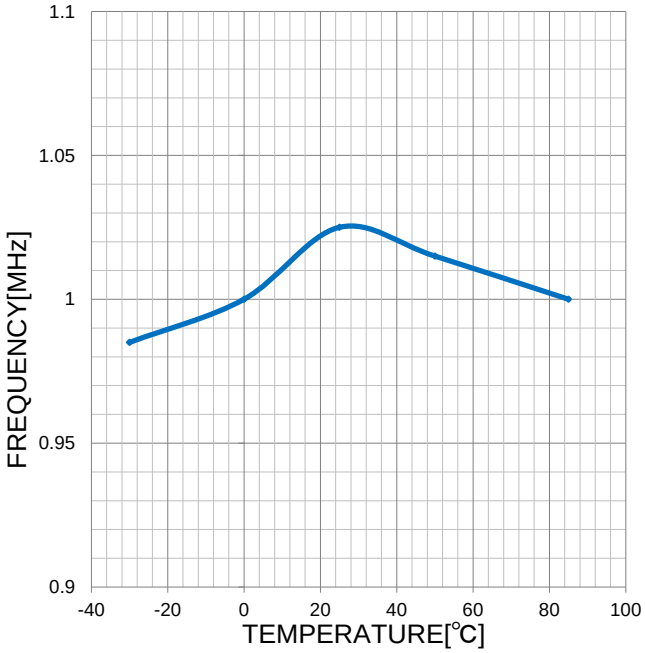


VREG_UVLO VOLTAGE VS. TEMPERATURE

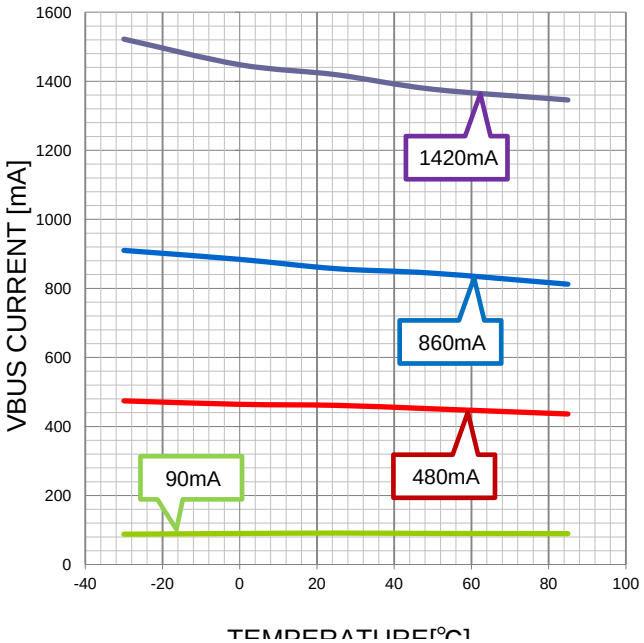


● Reference data

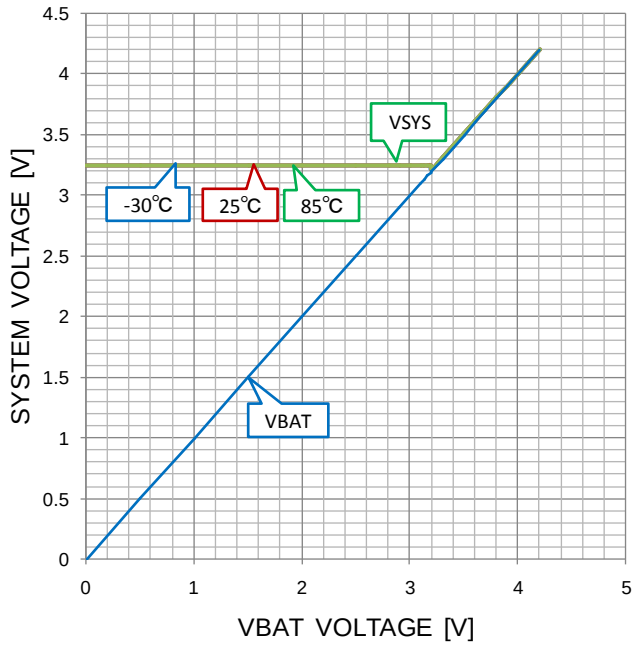
DCDC_CLK FREQUENCY VS. TEMPERATURE



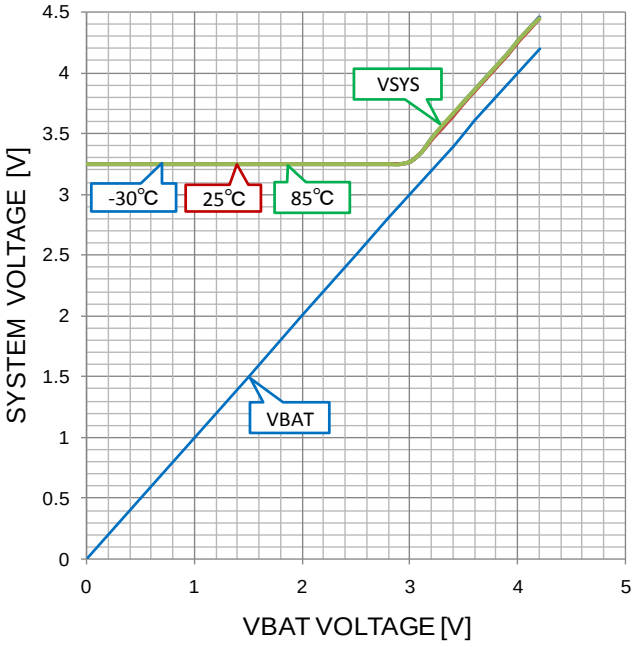
INPUT CURRENT LIMIT VS. TEMPERATURE



SYSTEM VOLTAGE VS. VBAT VOLTAGE (100mA LIMIT)

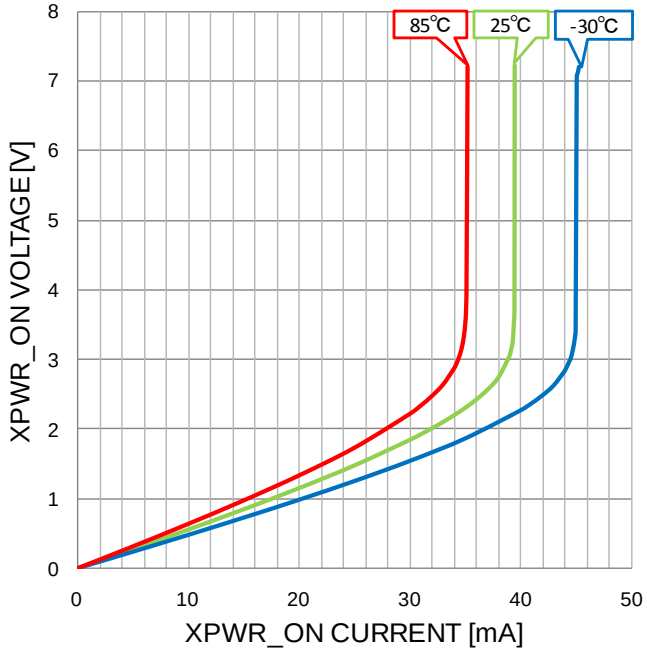


SYSTEM VOLTAGE VS. VBAT VOLTAGE (460mA LIMIT)

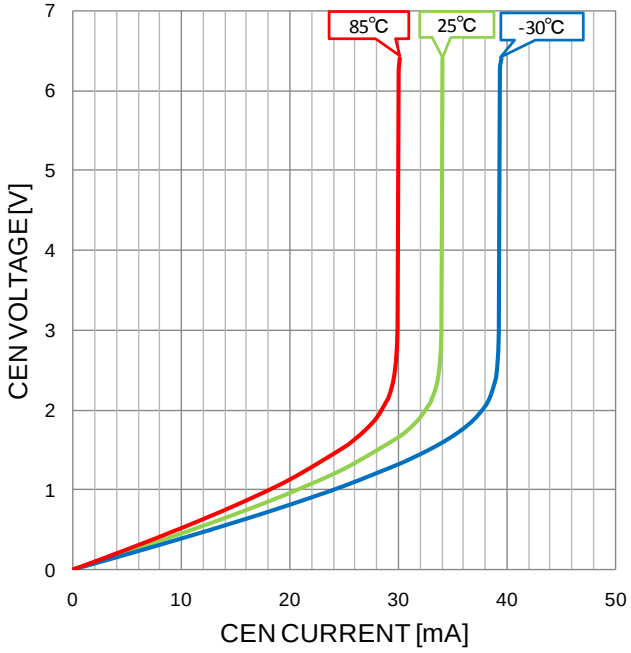


● Reference data

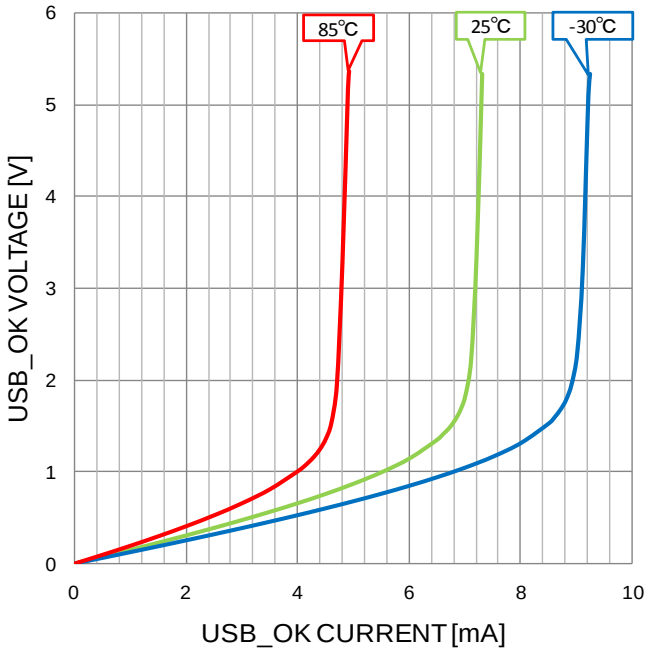
XPWR_ON CURRENT VS. XPWR_ON VOLTAGE



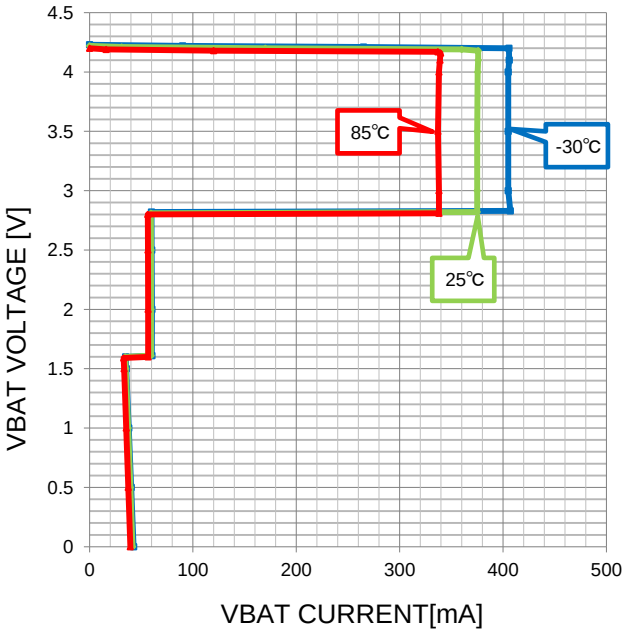
CEN CURRENT VS. CEN VOLTAGE



USB_OK CURRENT VS.USB_OK VOLTAGE

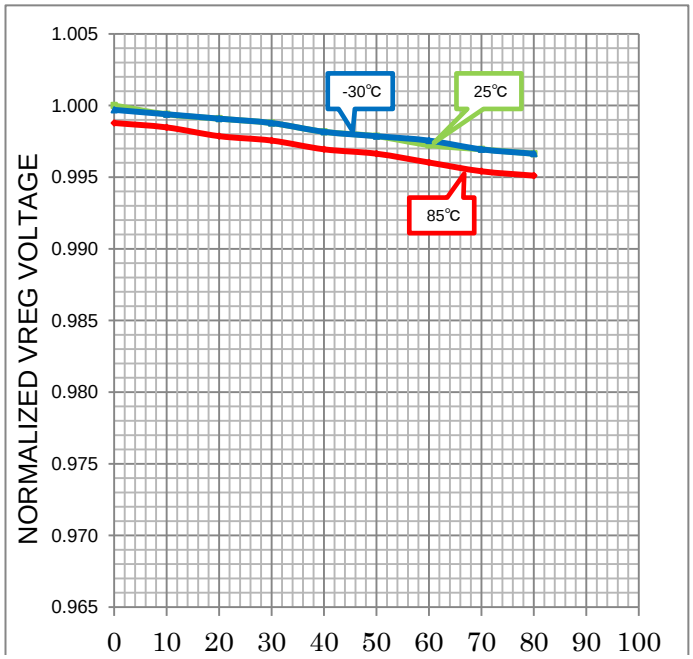


CC-CV CHARACTERISTIC

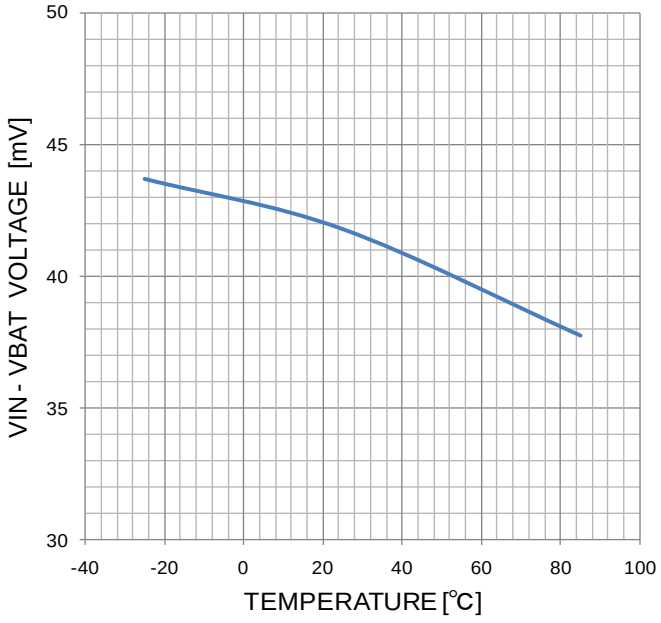


● Reference data

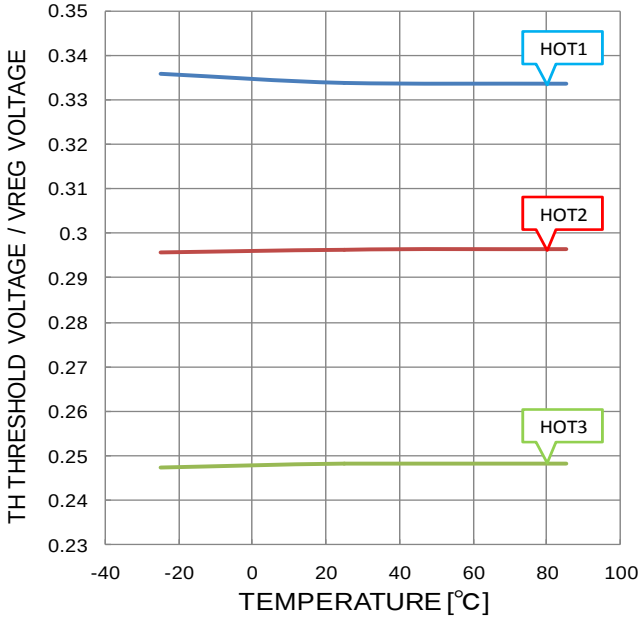
VREG LOAD REGURATION



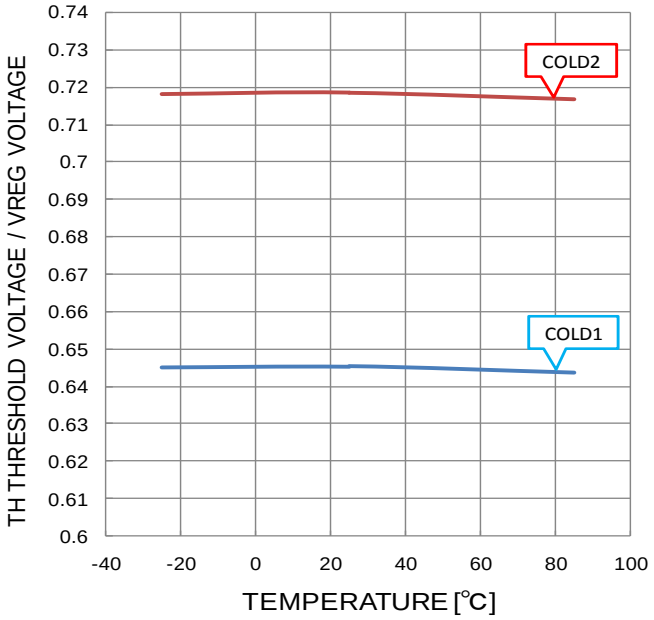
HIGH SIDE FET BACKGATE CONTROL VOLTAGE VS. TEMPERATURE



TH THRESHOLD VOLTAGE / VREG VOLTAGE VS. TEMPERATURE (HOT)

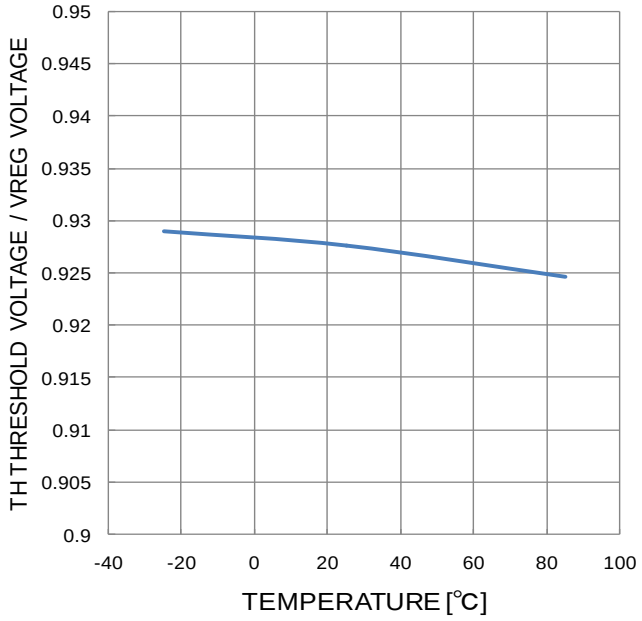


TH THRESHOLD VOLTAGE / VREG VOLTAGE VS. TEMPERATURE (COLD)

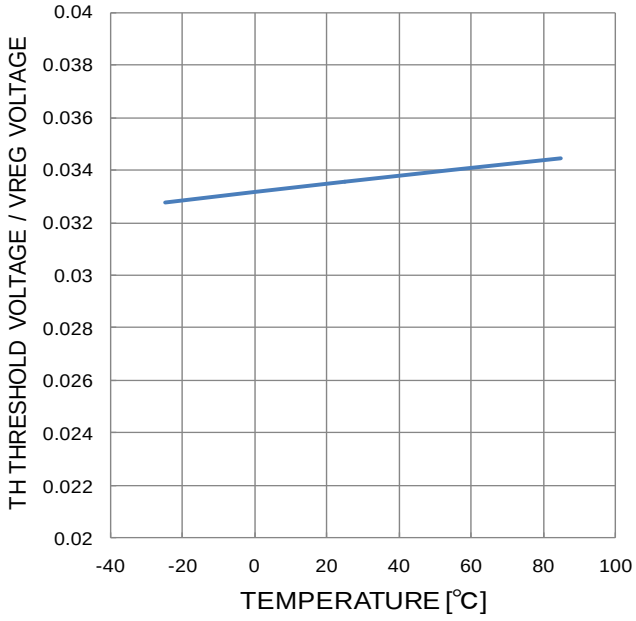


● Reference data

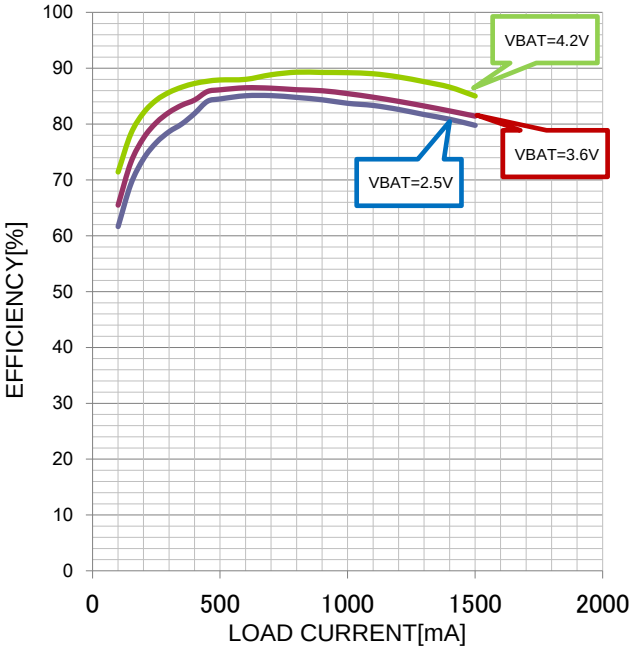
TH THRESHOLD VOLTAGE / VREG VOLTAGE VS. TEMPERATURE (BATOPN)



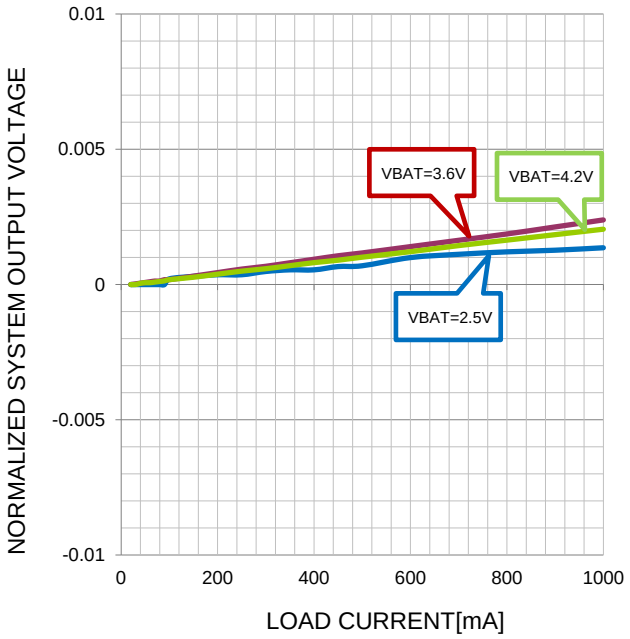
TH THRESHOLD VOLTAGE / VREG VOLTAGE VS. TEMPERATURE (DisEN)



BATTERY CHARGER EFFICIENCY

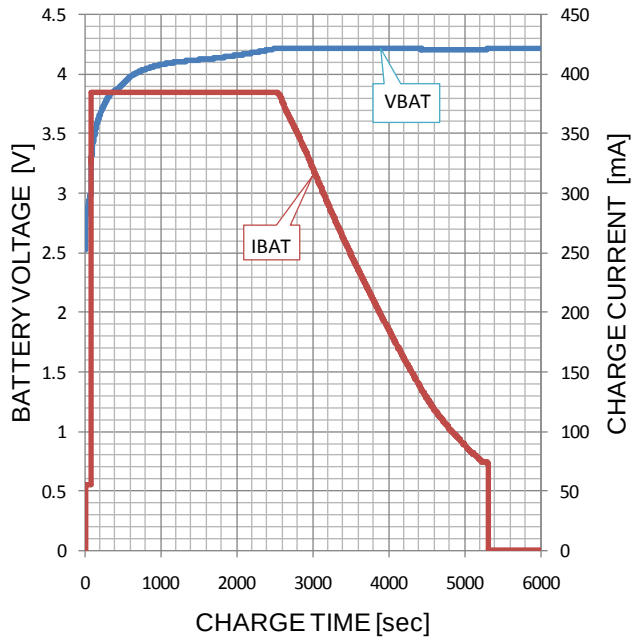


SYSTEM LOAD REGULATION

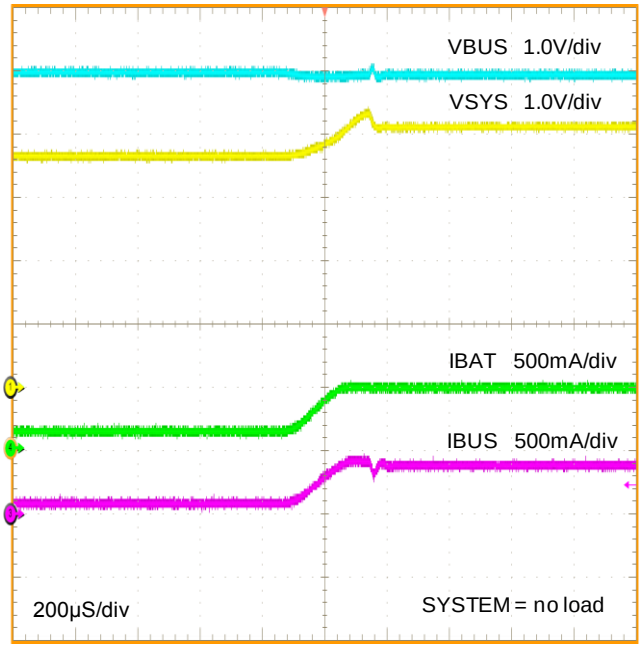


● Reference data

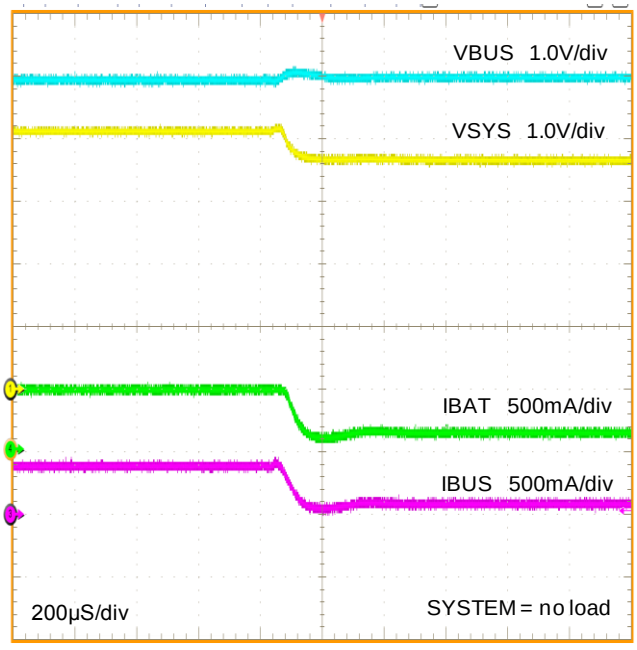
CHARGE CHARACTERISTIC



INPUT CURRENT LIMIT CHANGE FROM 90mA TO 480mA

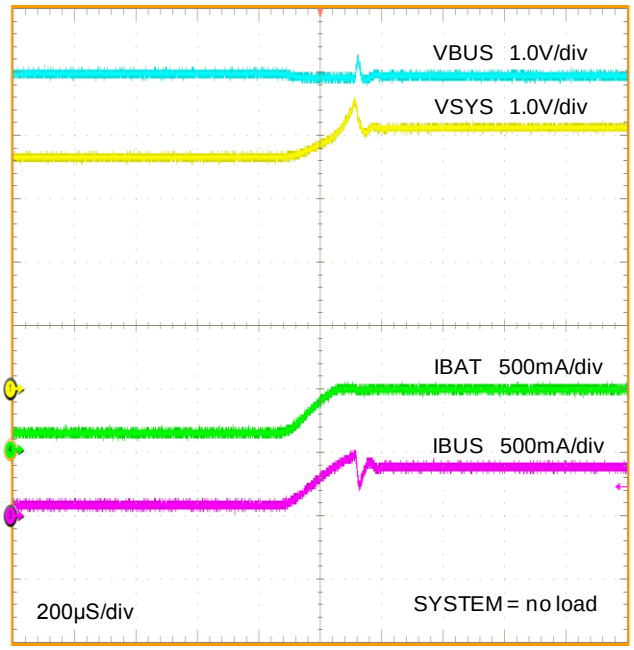


INPUT CURRENT LIMIT CHANGE FROM 480mA TO 90mA

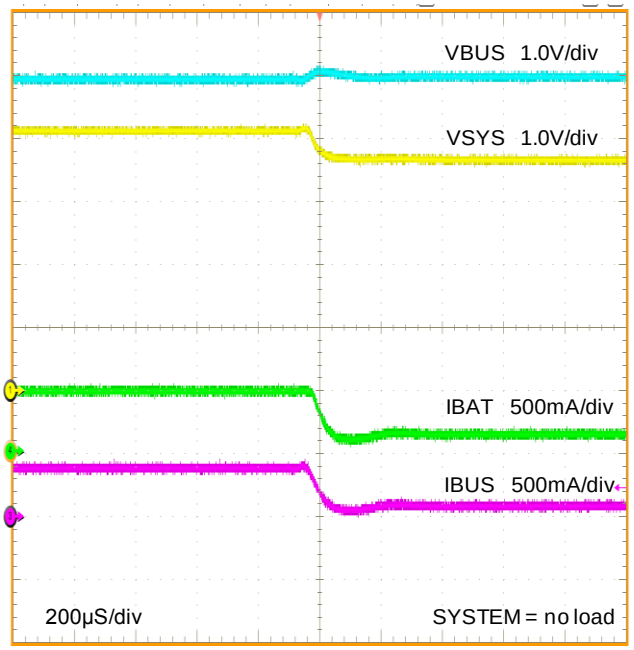


● Reference data

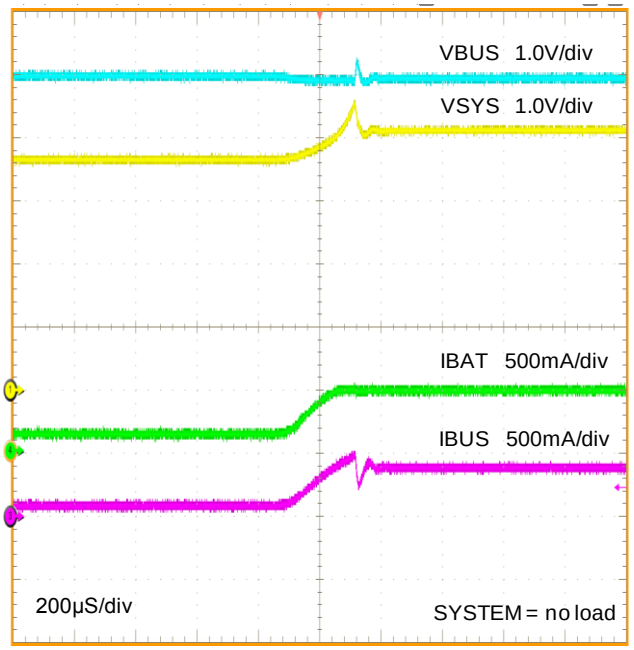
INPUT CURRENT LIMIT CHANGE FROM 90mA TO 860mA



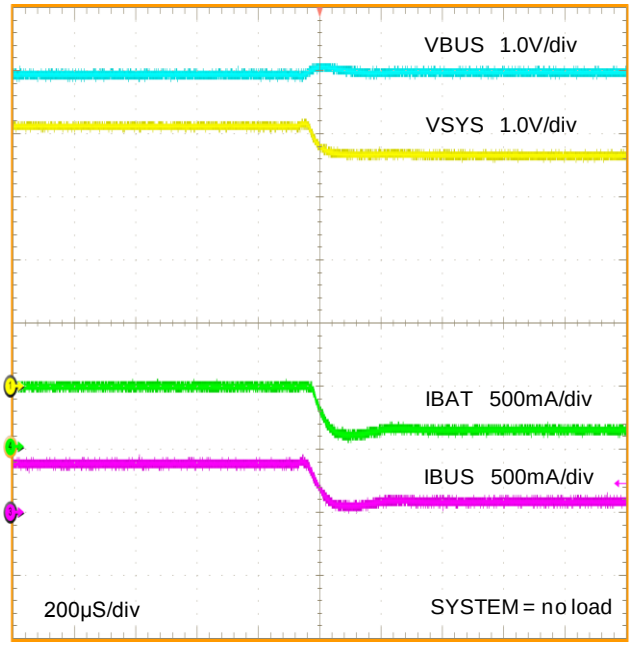
INPUT CURRENT LIMIT CHANGE FROM 860mA TO 90mA



INPUT CURRENT LIMIT CHANGE FROM 90mA TO 1420mA

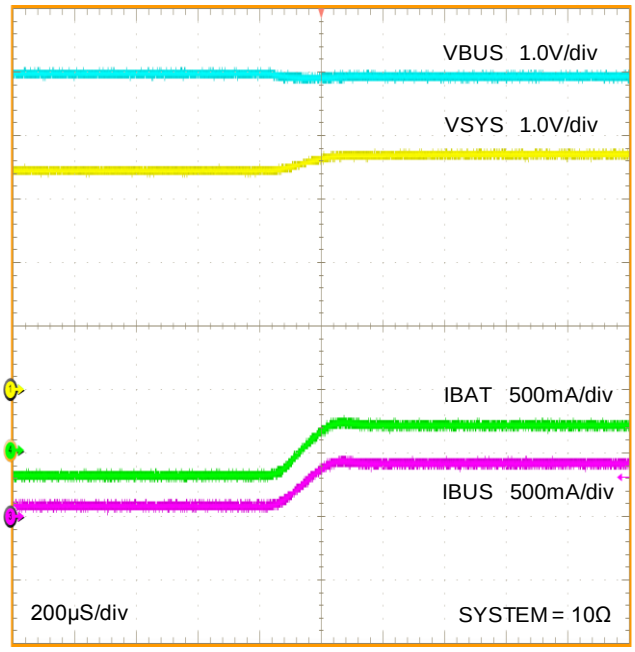


INPUT CURRENT LIMIT CHANGE FROM 1420mA TO 90mA

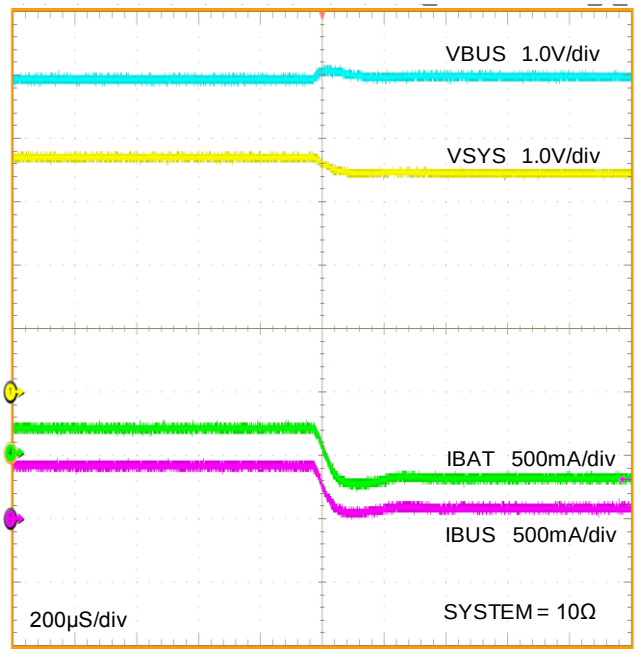


● Reference data

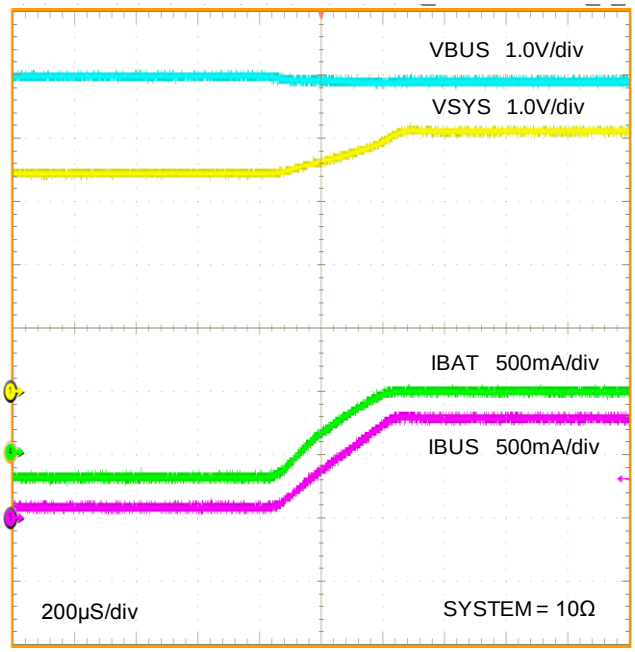
INPUT CURRENT LIMIT CHANGE FROM 90mA TO 480mA



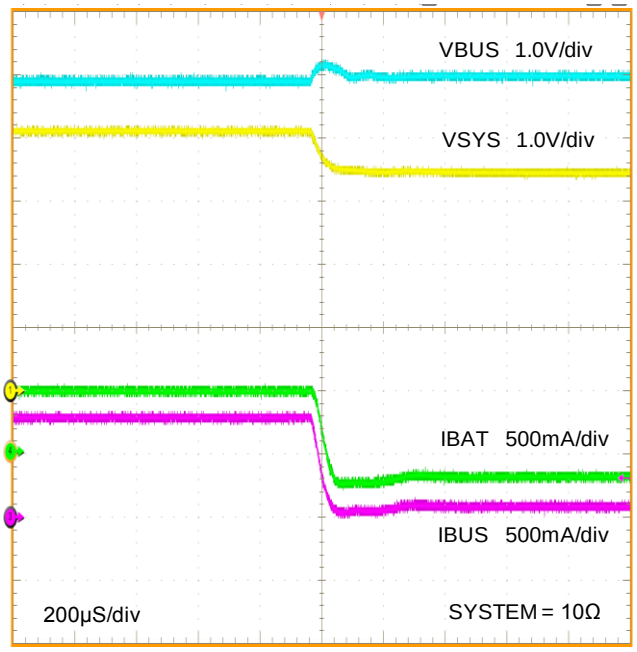
INPUT CURRENT LIMIT CHANGE FROM 480mA TO 90mA



INPUT CURRENT LIMIT CHANGE FROM 90mA TO 860mA

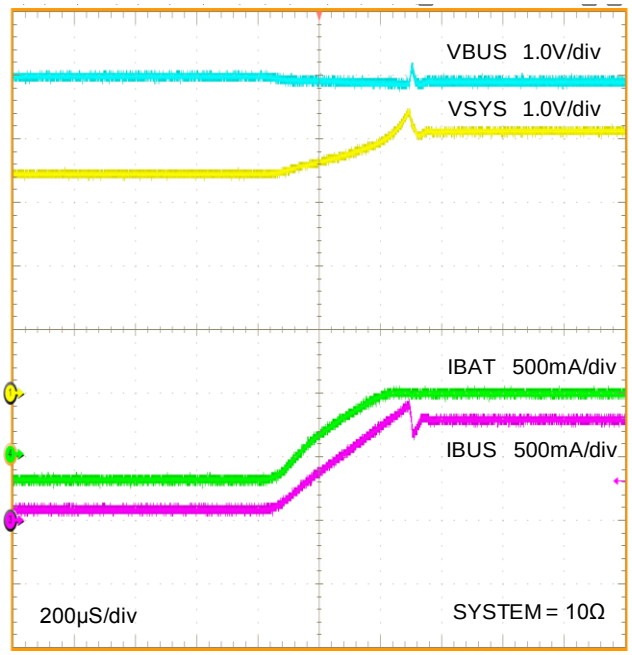


INPUT CURRENT LIMIT CHANGE FROM 860mA TO 90mA

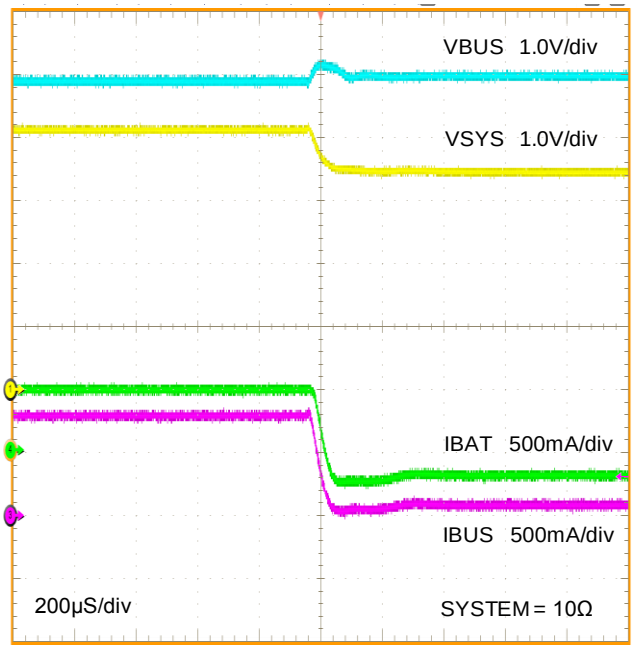


● Reference data

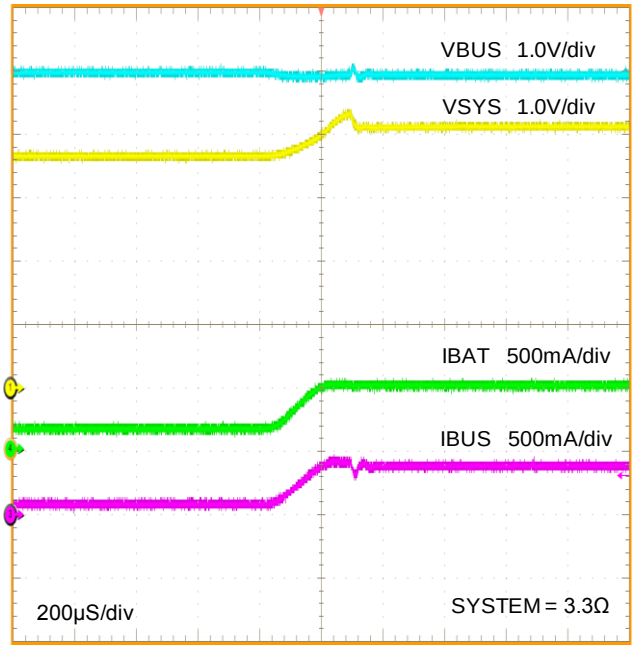
INPUT CURRENT LIMIT CHANGE FROM 90mA TO 1420mA



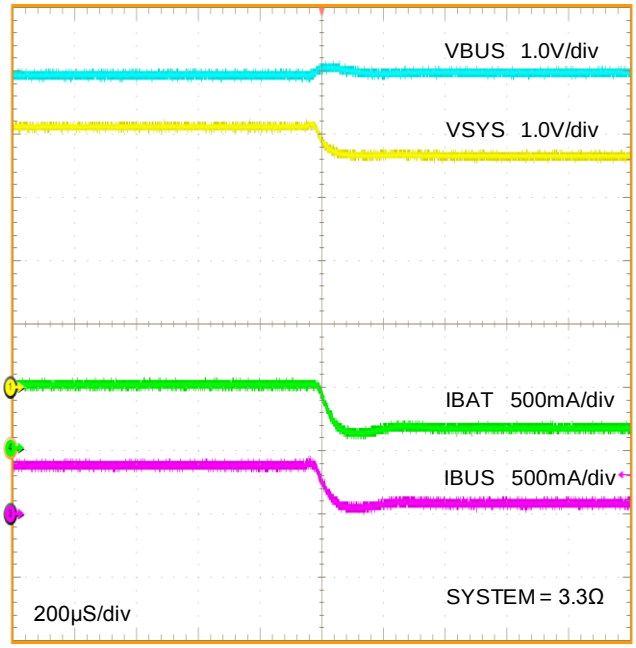
INPUT CURRENT LIMIT CHANGE FROM 1420mA TO 90mA



INPUT CURRENT LIMIT CHANGE FROM 90mA TO 480mA

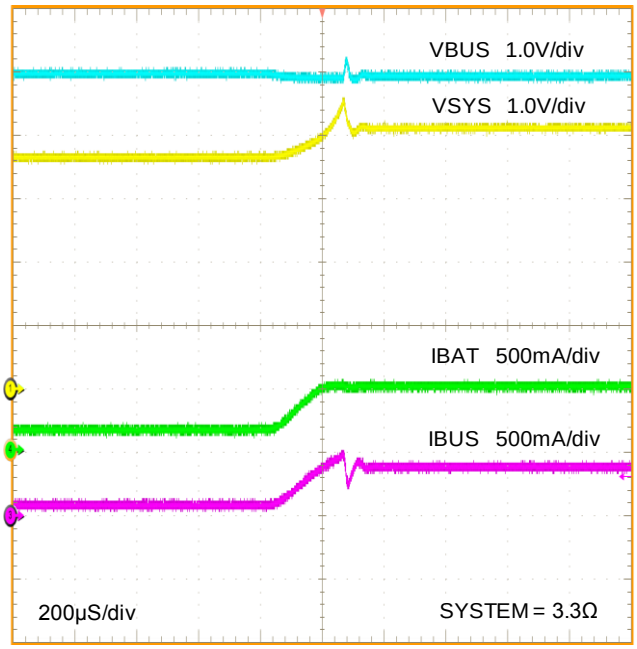


INPUT CURRENT LIMIT CHANGE FROM 480mA TO 90mA

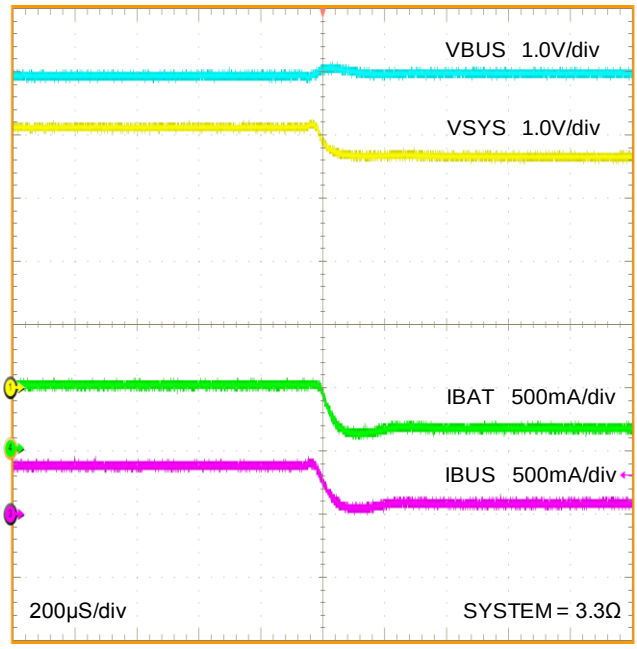


● Reference data

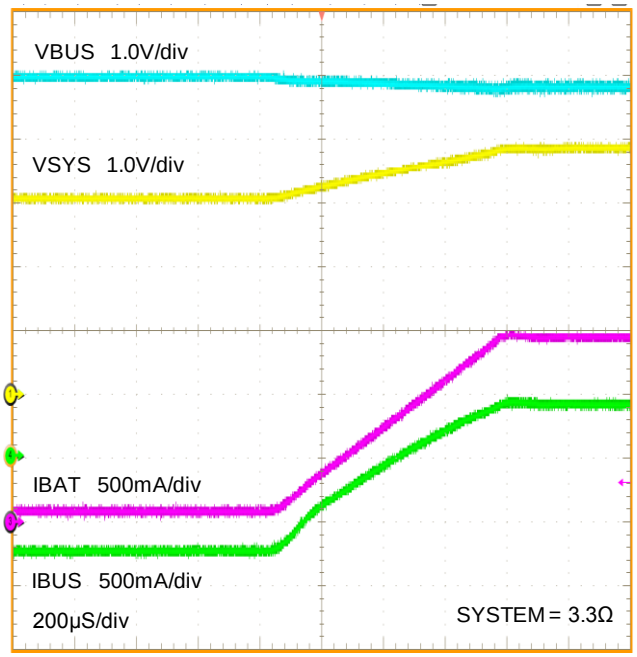
INPUT CURRENT LIMIT CHANGE FROM 90mA TO 860mA



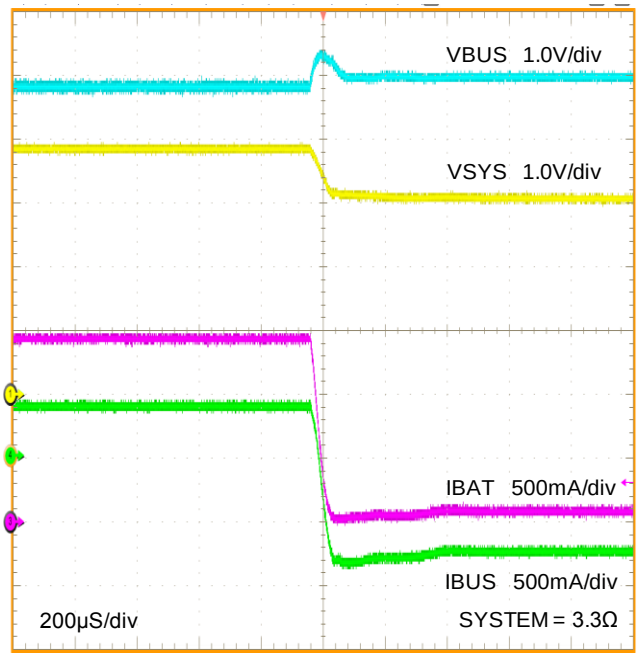
INPUT CURRENT LIMIT CHANGE FROM 860mA TO 90mA



INPUT CURRENT LIMIT CHANGE FROM 90mA TO 1420mA

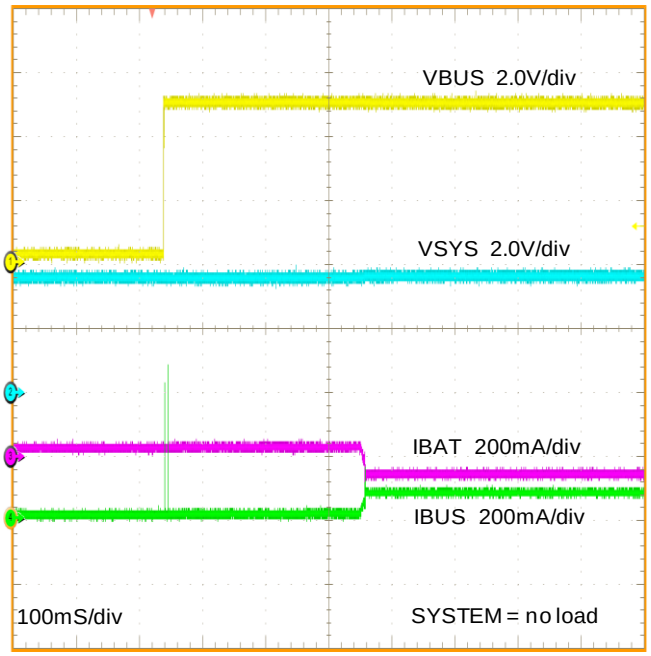


INPUT CURRENT LIMIT CHANGE FROM 1420mA TO 90mA

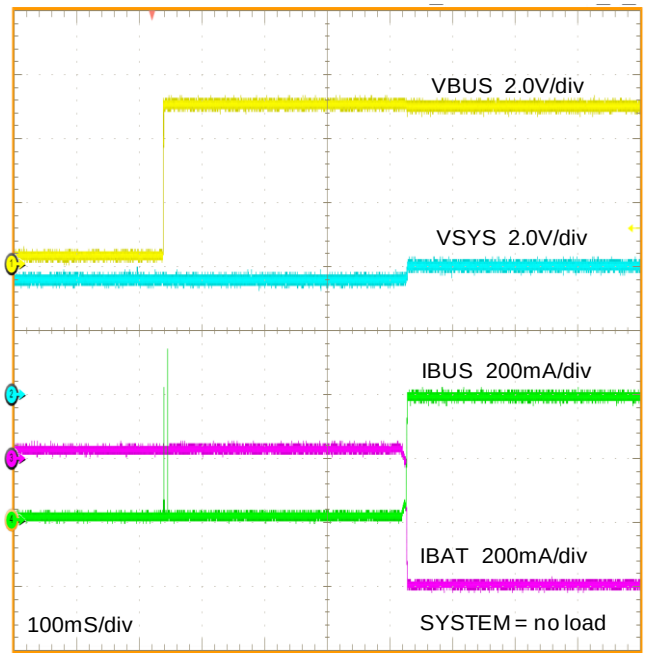


● Reference data

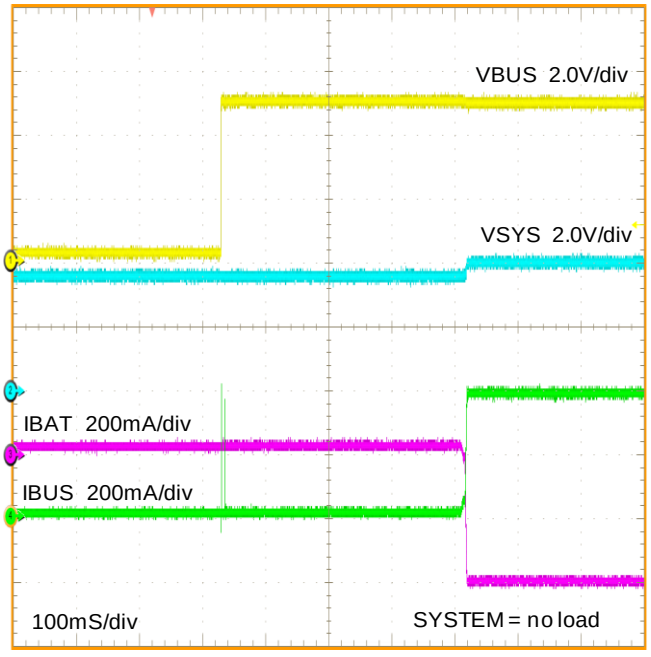
STARTUP CHARACTERISTIC (Input Current Limit 90mA)



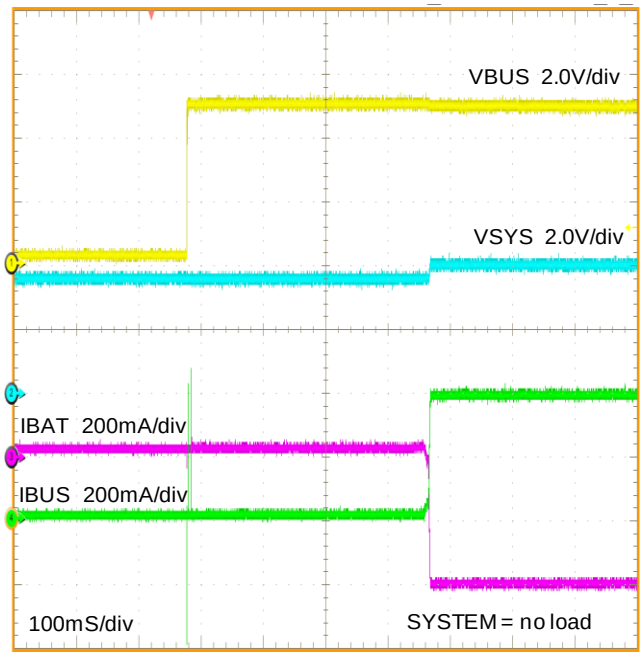
STARTUP CHARACTERISTIC (Input Current Limit 480mA)



STARTUP CHARACTERISTIC (Input Current Limit 860mA)

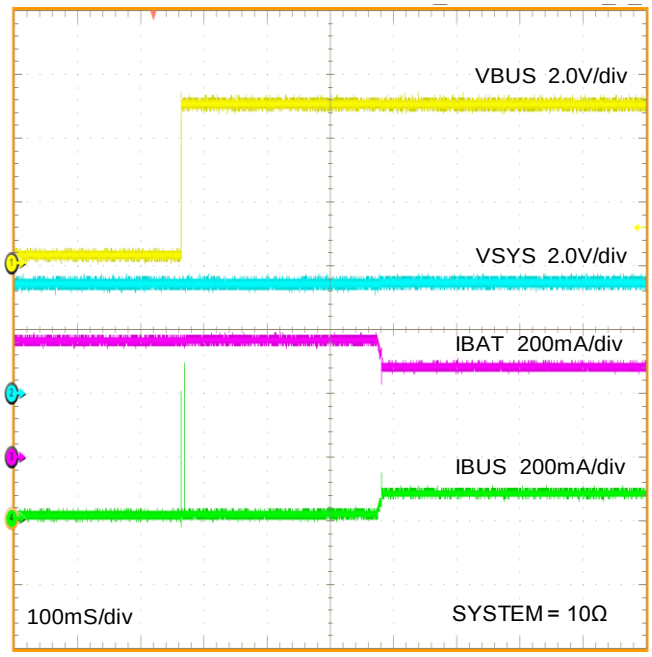


STARTUP CHARACTERISTIC (Input Current Limit 1420mA)

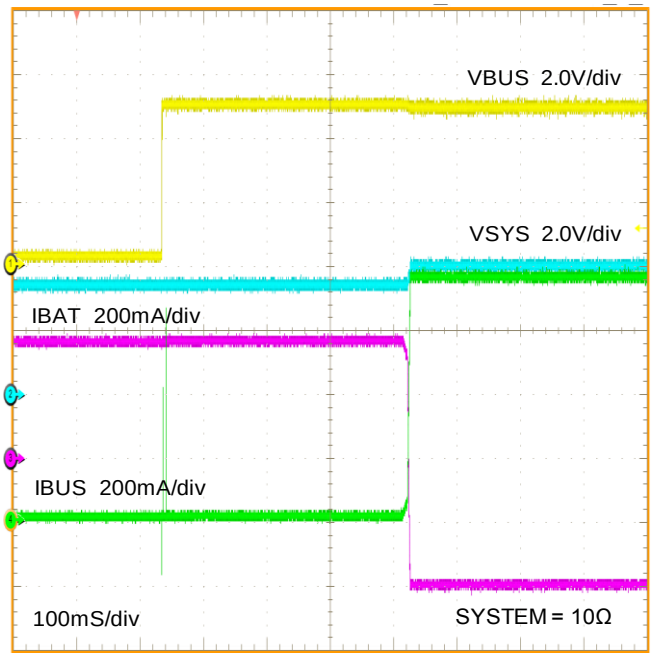


● Reference data

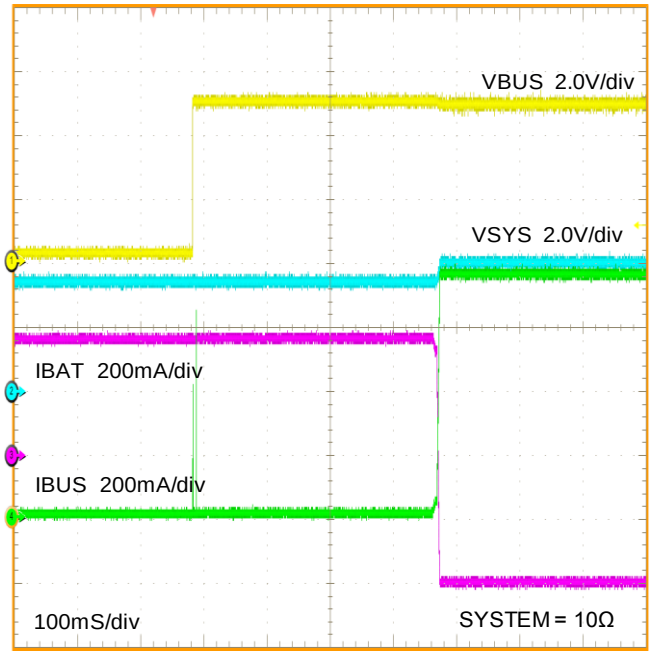
STARTUP CHARACTERISTIC (Input Current Limit 90mA)



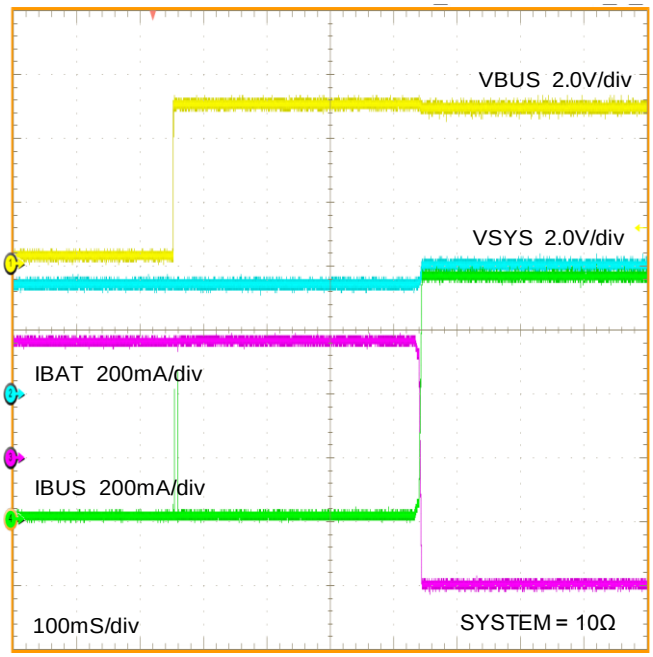
STARTUP CHARACTERISTIC (Input Current Limit 480mA)



STARTUP CHARACTERISTIC (Input Current Limit 860mA)

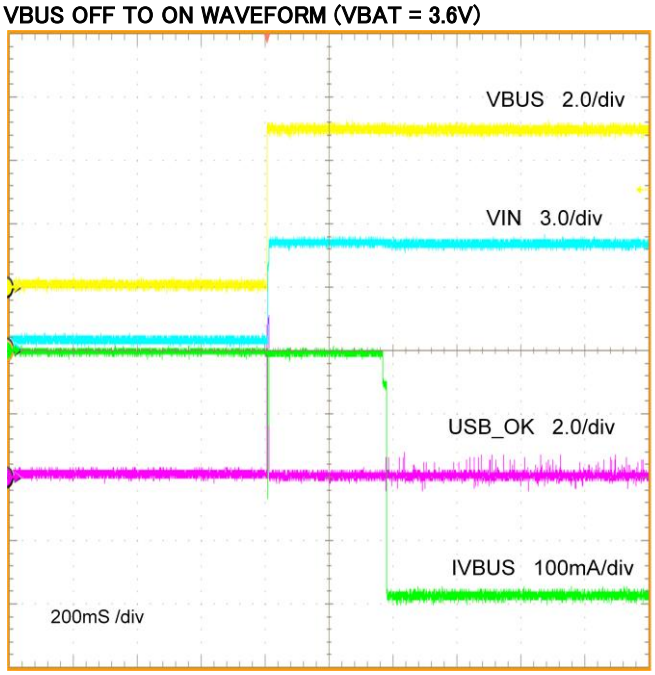


STARTUP CHARACTERISTIC (Input Current Limit 1580mA)

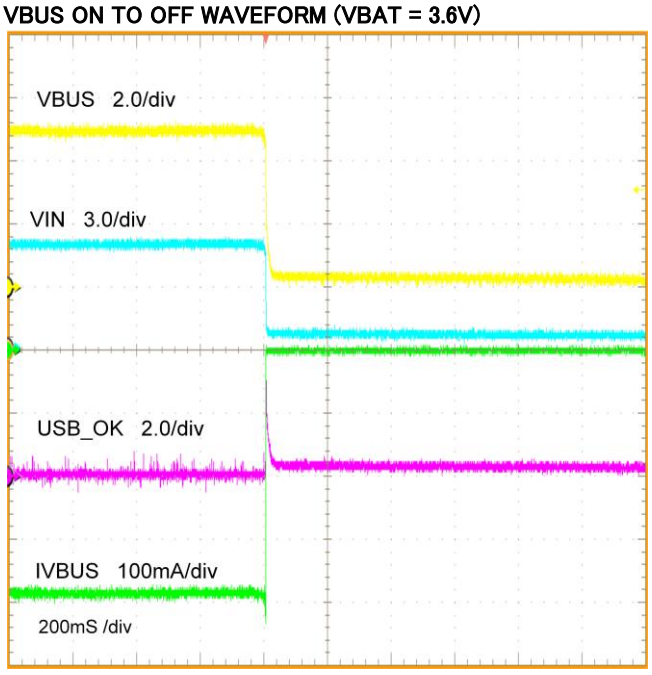


● Reference data

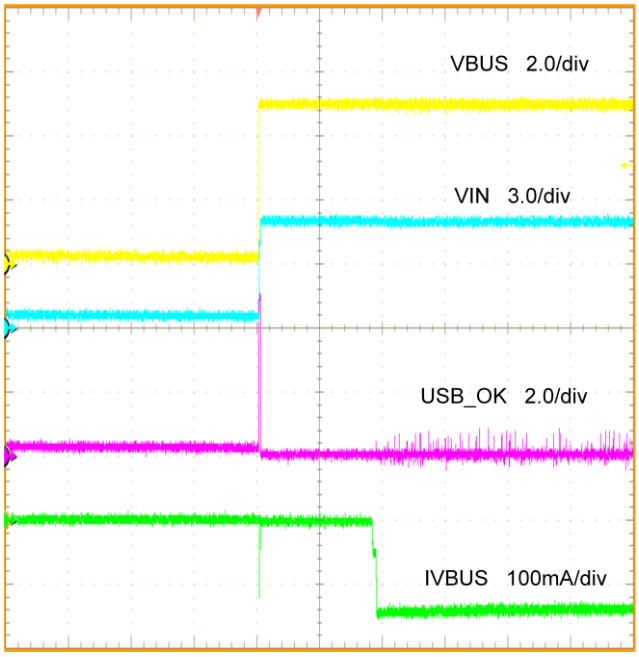
VBUS OFF TO ON WAVEFORM (VBAT = 3.6V)



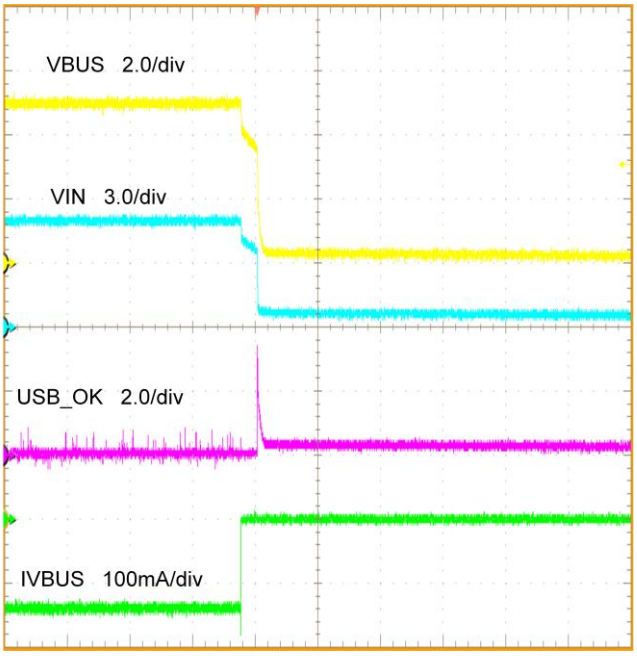
VBUS ON TO OFF WAVEFORM (VBAT = 3.6V)



VBUS OFF TO ON WAVEFORM (VBAT = 4.2V)

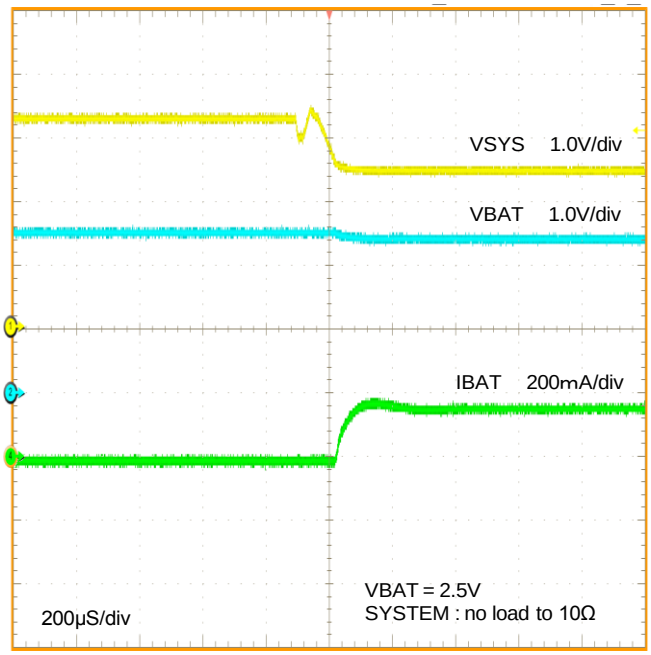


VBUS ON TO OFF WAVEFORM (VBAT = 4.2V)

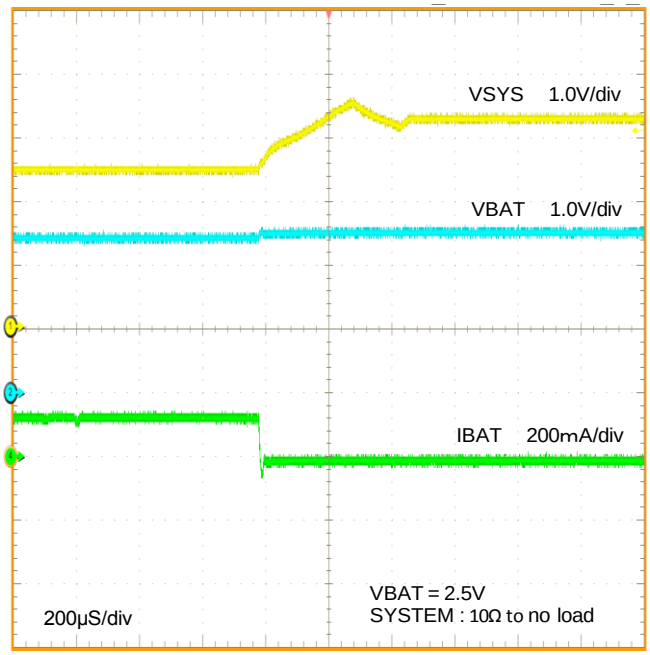


● Reference data

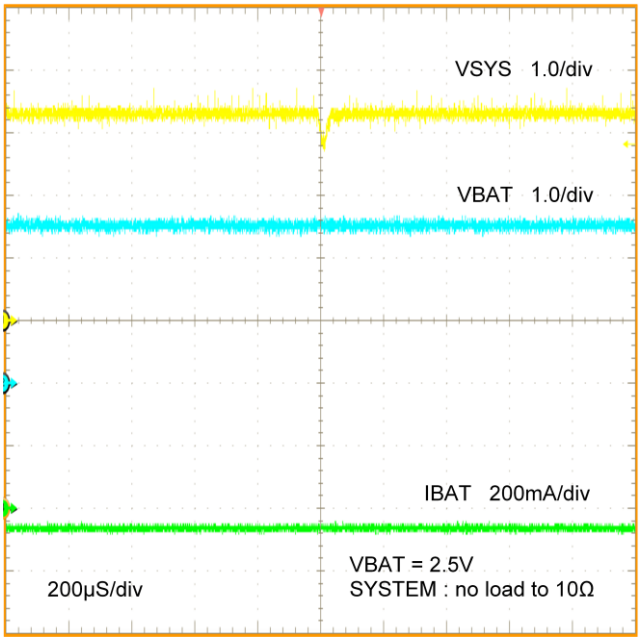
LOAD CHARACTERISTICS (Input Current Limit 90mA)



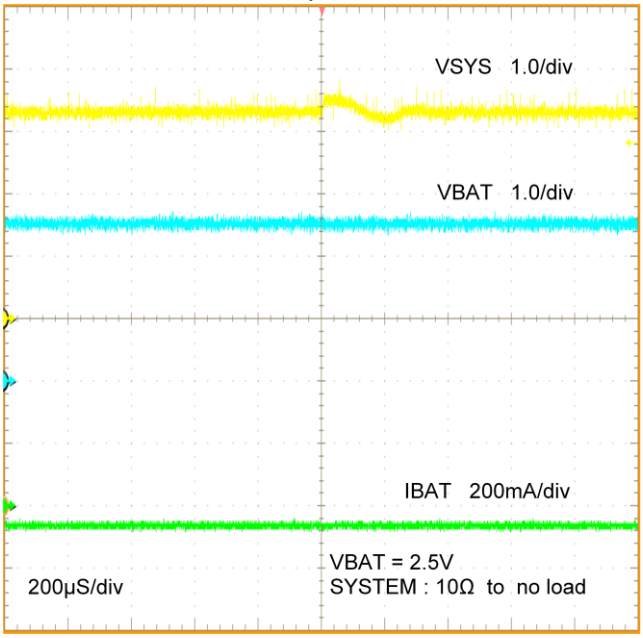
LOAD CHARACTERISTICS (Input Current Limit 90mA)



LOAD CHARACTERISTICS (Input Current Limit 860mA)

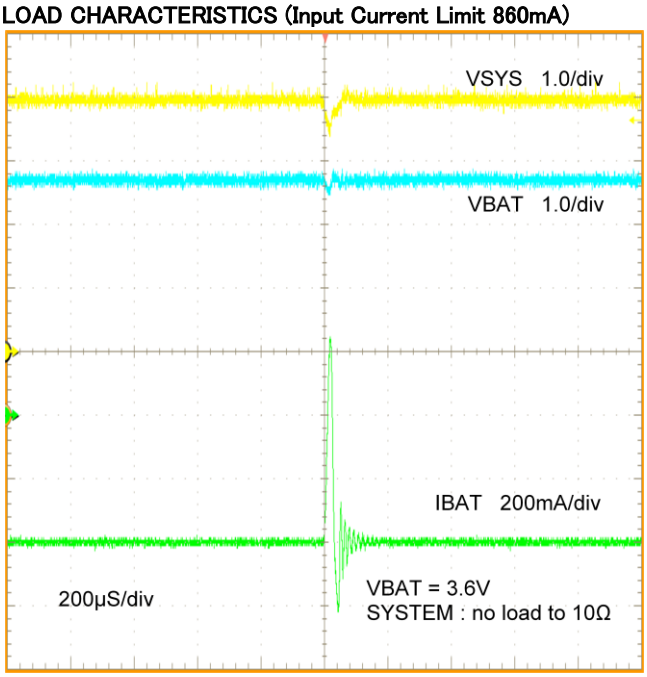


LOAD CHARACTERISTICS (Input Current Limit 860mA)

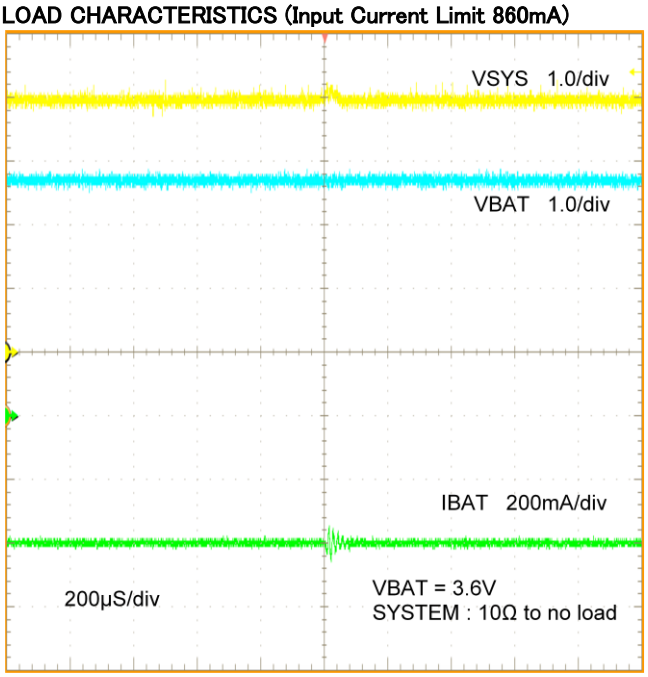


● Reference data

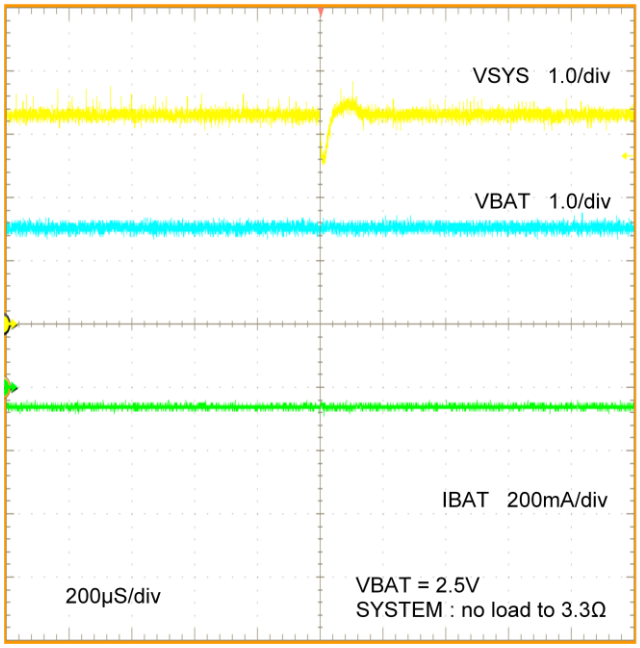
LOAD CHARACTERISTICS (Input Current Limit 860mA)



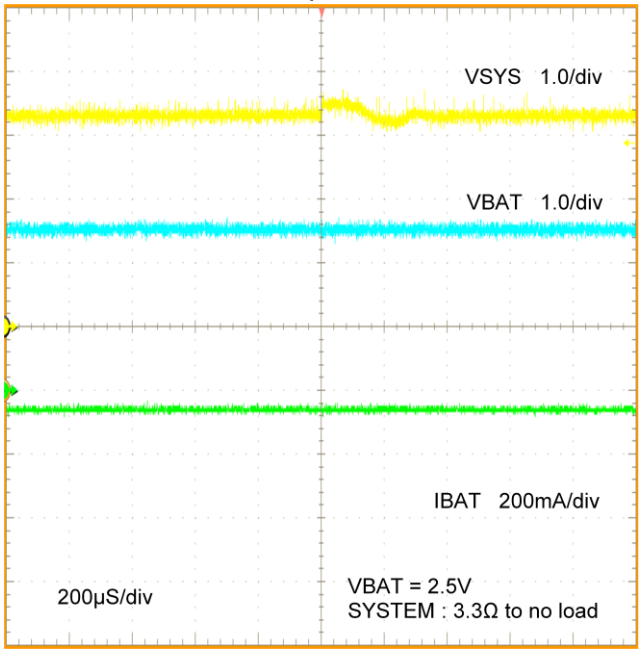
LOAD CHARACTERISTICS (Input Current Limit 860mA)



LOAD CHARACTERISTICS (Input Current Limit 860mA)

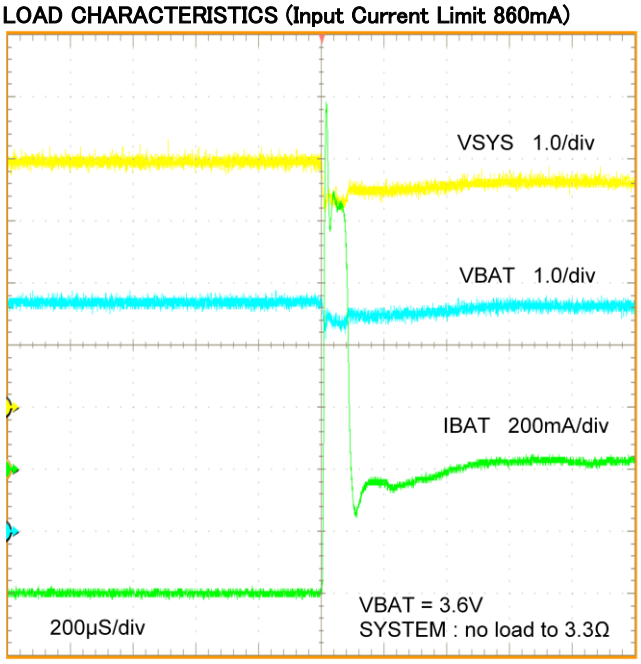


LOAD CHARACTERISTICS (Input Current Limit 860mA)

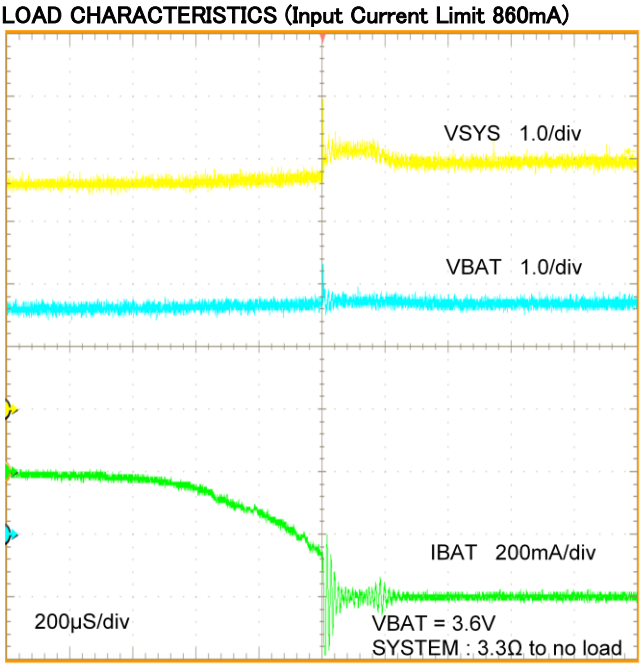


● Reference data

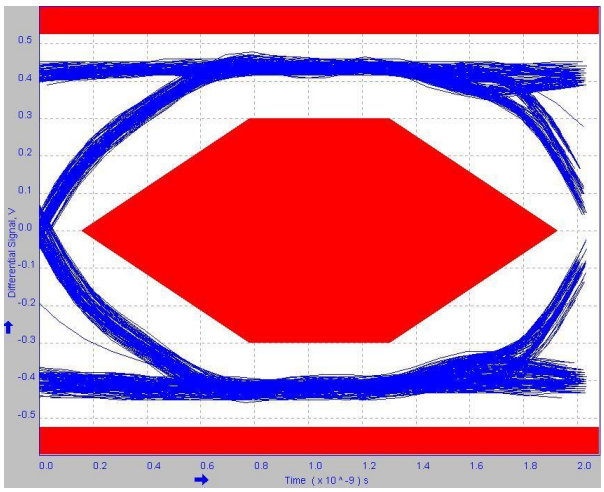
LOAD CHARACTERISTICS (Input Current Limit 860mA)



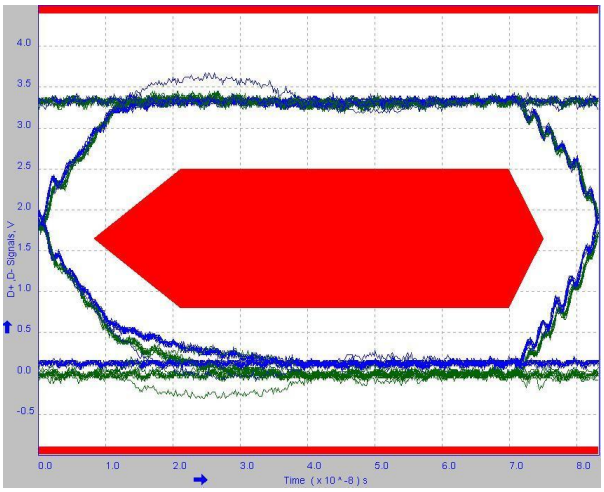
LOAD CHARACTERISTICS (Input Current Limit 860mA)



Analog SW EYE pattern (High speed mode)



Analog SW EYE pattern (Full speed mode)



○ Applied circuit diagram

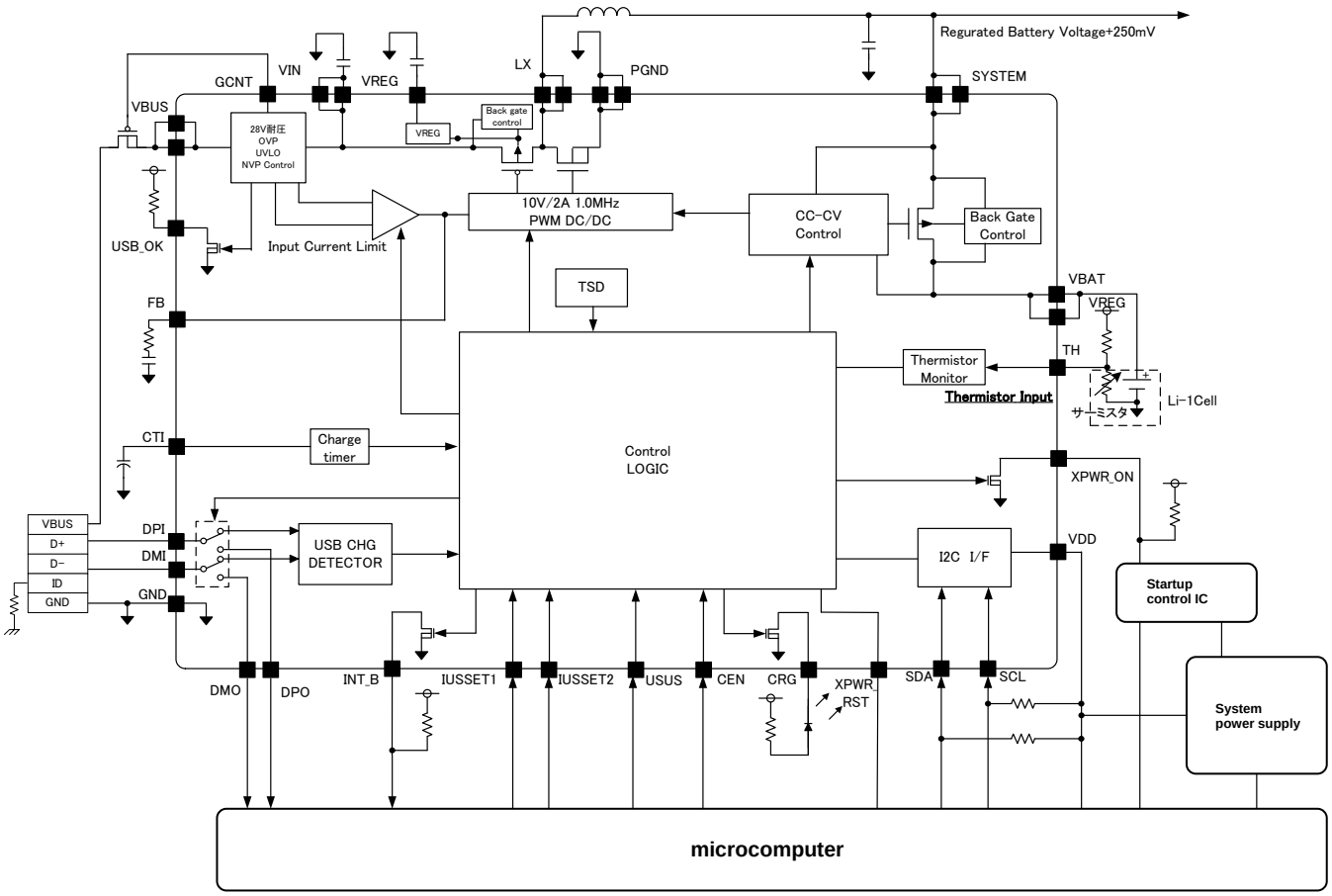


Figure 2. Applied circuit diagram

※Precautions for use

・We believe that the applied circuit diagram shown as an example is recommendable one, but please check the characteristics of the circuit with extreme care before using it. In addition, to use the circuit with any external circuit constant changed, determine it with sufficient margins allowed for variations in external parts and our IC, including static characteristic and transient characteristics.

● Charger unit state transition diagram

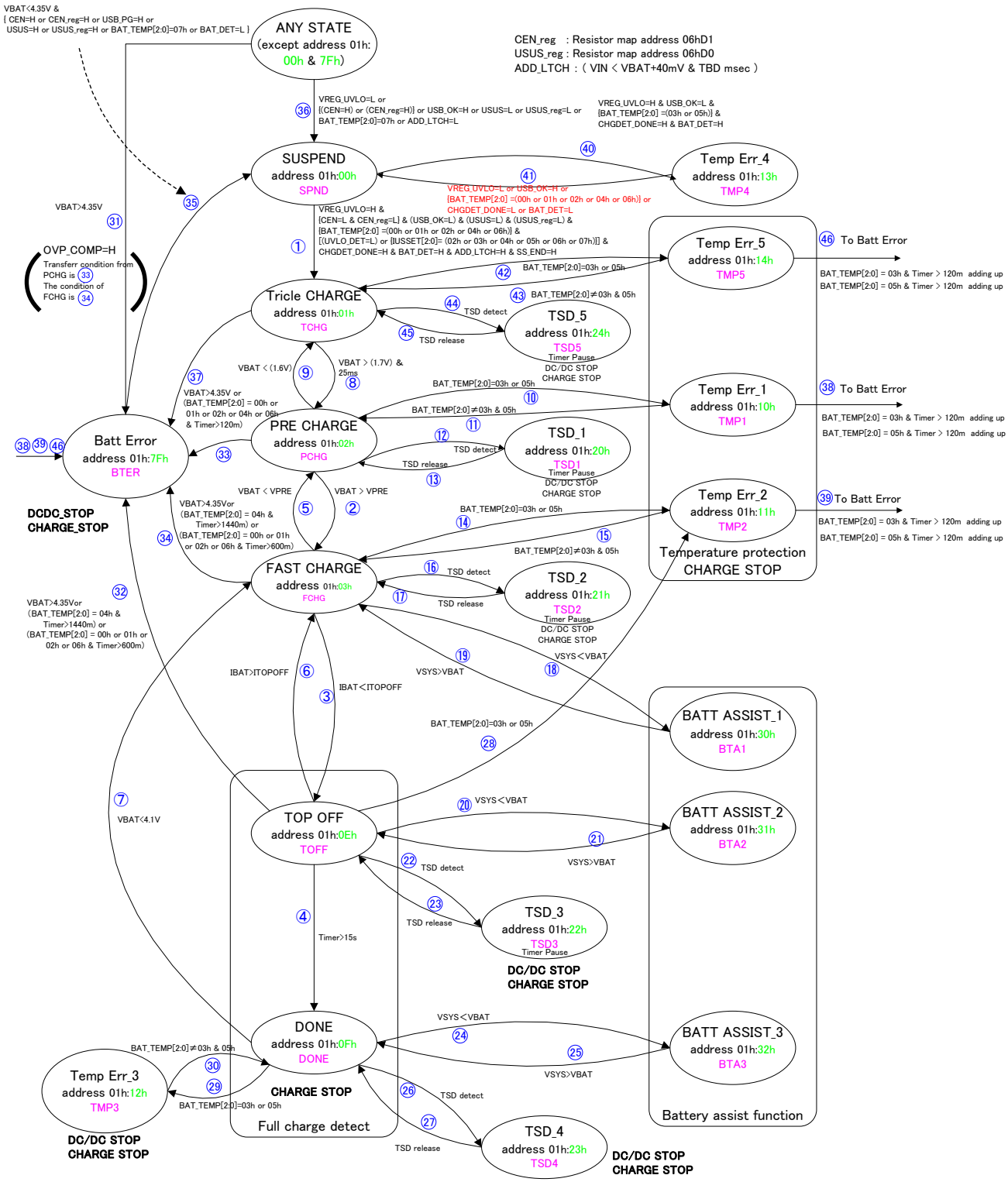


Figure 3. State transition diagram of charger

DC/DC stop condition	DC/DC operating conditions	
	BATDC_EN=L	BATDC_EN=H
Conditions except for the right conditions	USB_OK = L & VREG≧2.5V&USUS_reg = L & USUS= L & Tj≦150℃ VIN>VBAT&CHGDETDONE=H & BAT_DET =H & BATTEMP ≠07h	USB_OK = L & VREG≧2.5V&USUS_reg = L & USUS= L & Tj≦150℃ VIN>VBAT&CHGDETDONE=H

	Form	Start condition	Reset conditon	Pause condition	Restart condition
Precharge timer	Adding up	TricleCHARGE,PRECHARGE	②,㊸,㊱	⑩,⑫	⑪,⑬
Fastcharge timer	Adding up	FAST CHARGE,TOP OFF	⑤,㊷,㊹,④,㊱	⑭,⑯,	⑮,⑰
High temperature timer 1	Adding up	Temp Err1 BAT_TEMP[2:0]=03h	㉛,㊽,㊱,②	⑪	⑩
Low temperature timer 1	Adding up	Temp Err1 BAT_TEMP[2:0]=05h	㉛,㊽,㊱,②	⑪	⑩
High temperature timer 2	Adding up	Temp Err2 BAT_TEMP[2:0]=03h	㉛,㊾,㊱,⑤	⑮	⑭
Low temperature timer 2	Adding up	Temp Err2 BAT_TEMP[2:0]=05h	㉛,㊾,㊱,⑤	⑮	⑭
High temperature timer 5	Adding up	Temp Err5 BAT_TEMP[2:0]=03h	㉛,㊻,㊱,⑧	㊸	㊷
Low temperature timer 5	Adding up	Temp Err5 BAT_TEMP[2:0]=05h	㉛,㊻,㊱,⑧ ,	㊸	㊷

● **Timing chart during regular charge**

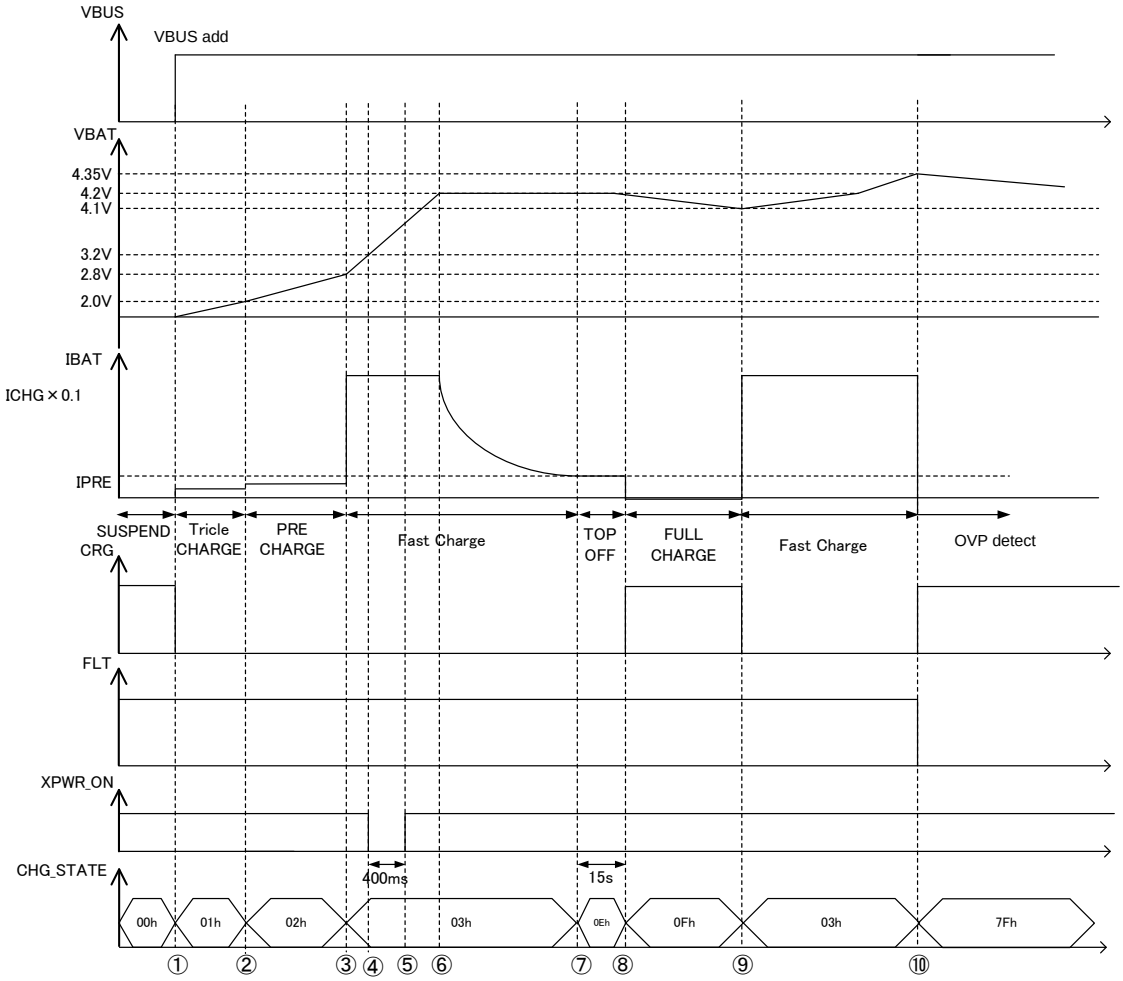


Figure 4. Timing chart during regular charge

① VBUS is applied, tricle-charge begins, and the state of CRG changes from Hi to Low.
② When VBAT>2.0V, pre-charge stars.
③ The charge mode switches to fast charge when VBAT exceeds 2.8 V, and constant-current charge begins.
④ When VBAT>3.2V, XPWR_ON pulse is generated.
⑤ In 400msec XPWR_ON=”Hi-Z”
⑥ When VBAT exceeds 4.2 V, constant-voltage charge begins.
⑦ Constant-voltage charge (fast charge) ends when the IBAT current reaches 80 mA, and a 15-second TOP OFF period begins.
⑧ The TOP OFF period ends. The system is in a full charge state, and charge no longer takes place. The state of CRG changes from Low to Hi.
⑨ Recharge begins when VBAT drops below 4.1 V. The state of CRG changes from Hi to Low.
⑩ In case of overcharge, charge is discontinued by OVP detection when VBAT exceeds 4.35 V. The state of CRG is Low, and FLT terminal change form High to Low.

● USB connection startup timing chart (when current limit automatic detection is changed from 1420mA to 1140mA) (VBAT>3.2V)

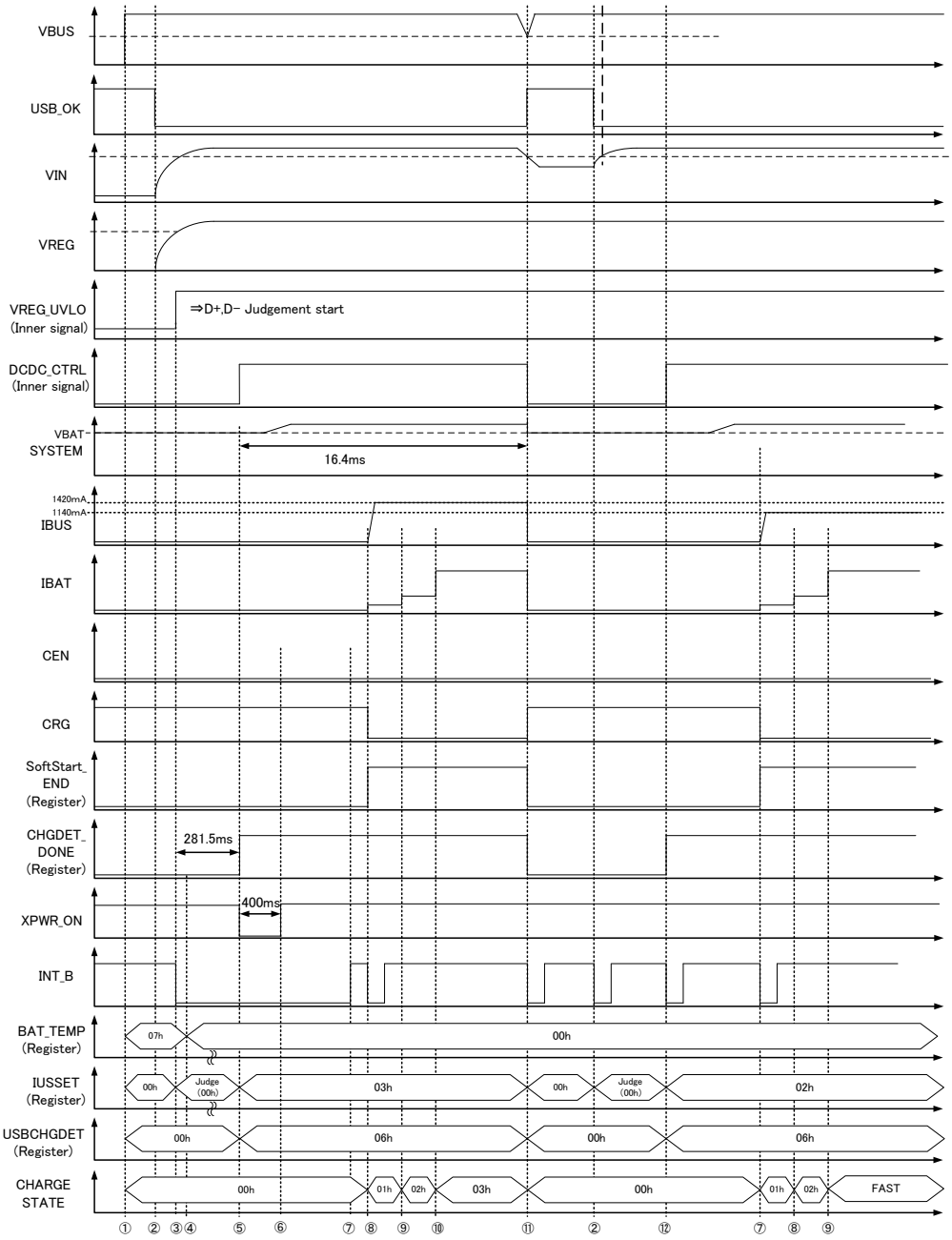


Figure 5. USB connection startup timing chart (when current limit automatic detection is changed from 1420mA to 1140mA)

① VBUS is connected.
② USB_OK output, OVP FET is ON and voltage is supplied to VIN.
③ VREG outputs and UVLO release. After that, charger detection is starts.
④ Charger detection is finished, and DC/DC operates after input current limit and charging port and determined.
⑤ Due to VBAT>3.2V, XPWR_ON outputs after charger detection.
⑥ In 400msec, XPWR_ON resets.
⑦ Confirming the condition with I2C , INT_B and XPWR_ON are released
⑧ DC/DC starts and SS end flag outputs. After that charge starts.
⑨ Charge state is changed from tricle-charge to pre-charge.
⑩ Charge state is changed from pre-charge to fast-charge.
⑪ VBUS voltage is down by increasing load current. Detecting UVLO, the condition move to SUSPEND and input current is changed automatically.
⑫ After charger detection, input current limit and charging port are updated and DC/DC is ON. The value of input current limit is -01h determined at ④.

● USB connection startup timing chart (In a case that the state doesn't return when current limit 900mA→500mA)

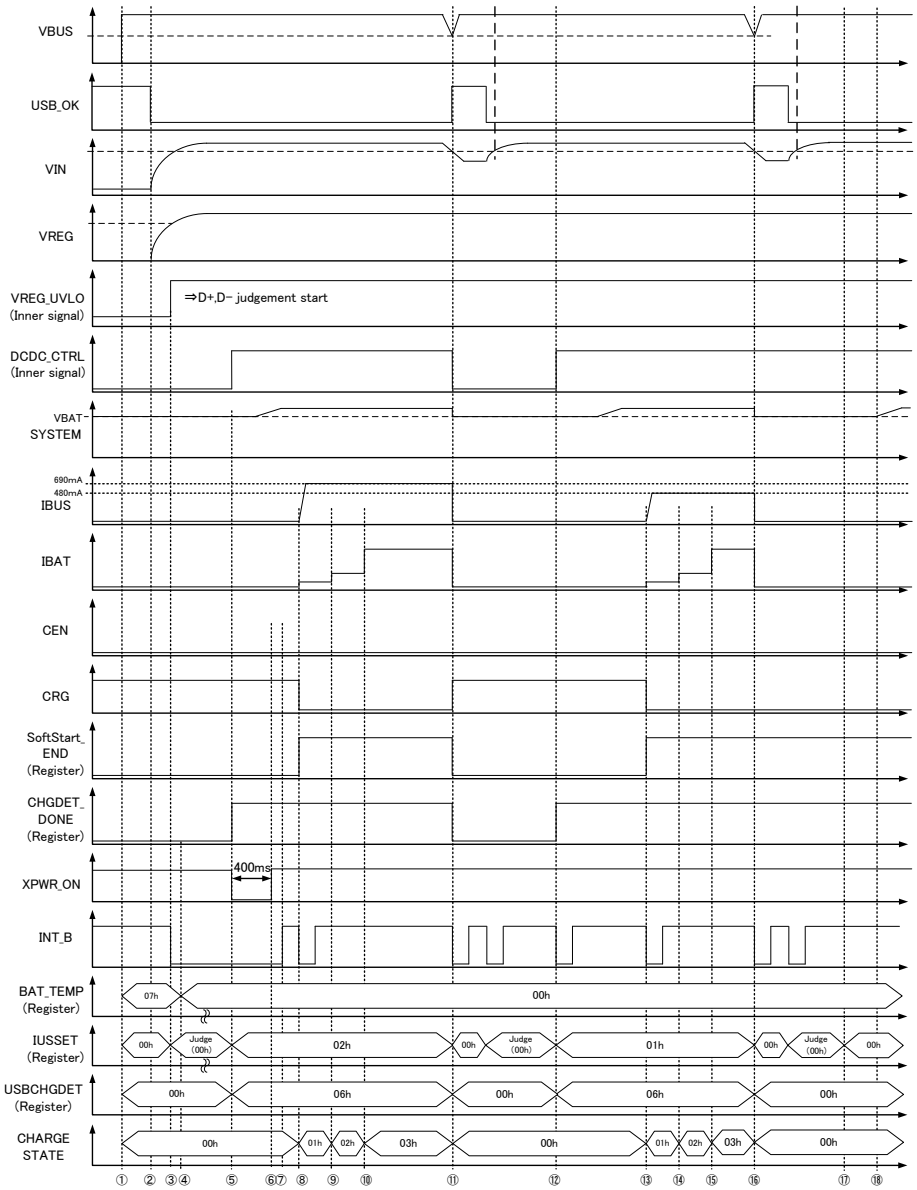


Figure 6. USB connection startup timing chart (In a case that the state doesn't return when current limit 900mA→500mA)

① VBUS is connected.
② USB_OK output, OVP FET is ON and voltage is supplied to VIN.
③ VREG outputs and UVLO release. After that , charger detection is starts.
④ Charger detection is finished, and DC/DC operates after input current limit and charging port and determined.
⑤ Due to VBAT>3.2V, XPWR_ON outputs after charger detection.
⑥ In 400msec, XPWR_ON resets.
⑦ Confirming the condition with I2C , INT_B and XPWR_ON are released
⑧ DC/DC starts and SS end flag outputs. After that charge starts.
⑨ Charge state is changed from tricle-charge to pre-charge.
⑩ Charge state is changed from pre-charge to fast-charge.
⑪ VBUS voltage is down by increasing load current. Detecting UVLO, the condition move to SUSPEND and input current is changed automatically.
⑫ After charger detection, input current limit and charging port are updated and DC/DC is ON.Input current limit is 480mA(01h)
⑬ DC/DC starts , SS end flag output and charge starts.
⑭ The condition change from tricle charge to pre charge.
⑮ The condition change from pre charge to fast charge.
⑯ VBUS voltage is down by increasing load current. Detecting UVLO, the condition move to SUSPEND and input current is changed automatically.
⑰ After charger detection, input current limit and charging port are updated and DC/DC is ON.Input current limit is 90mA(00h)
⑱ DC/DC starts , SS end flag output , but the condition dosen't transferr to charge state but to SUSPEND.

● **Timing chart when USB is pulled out**

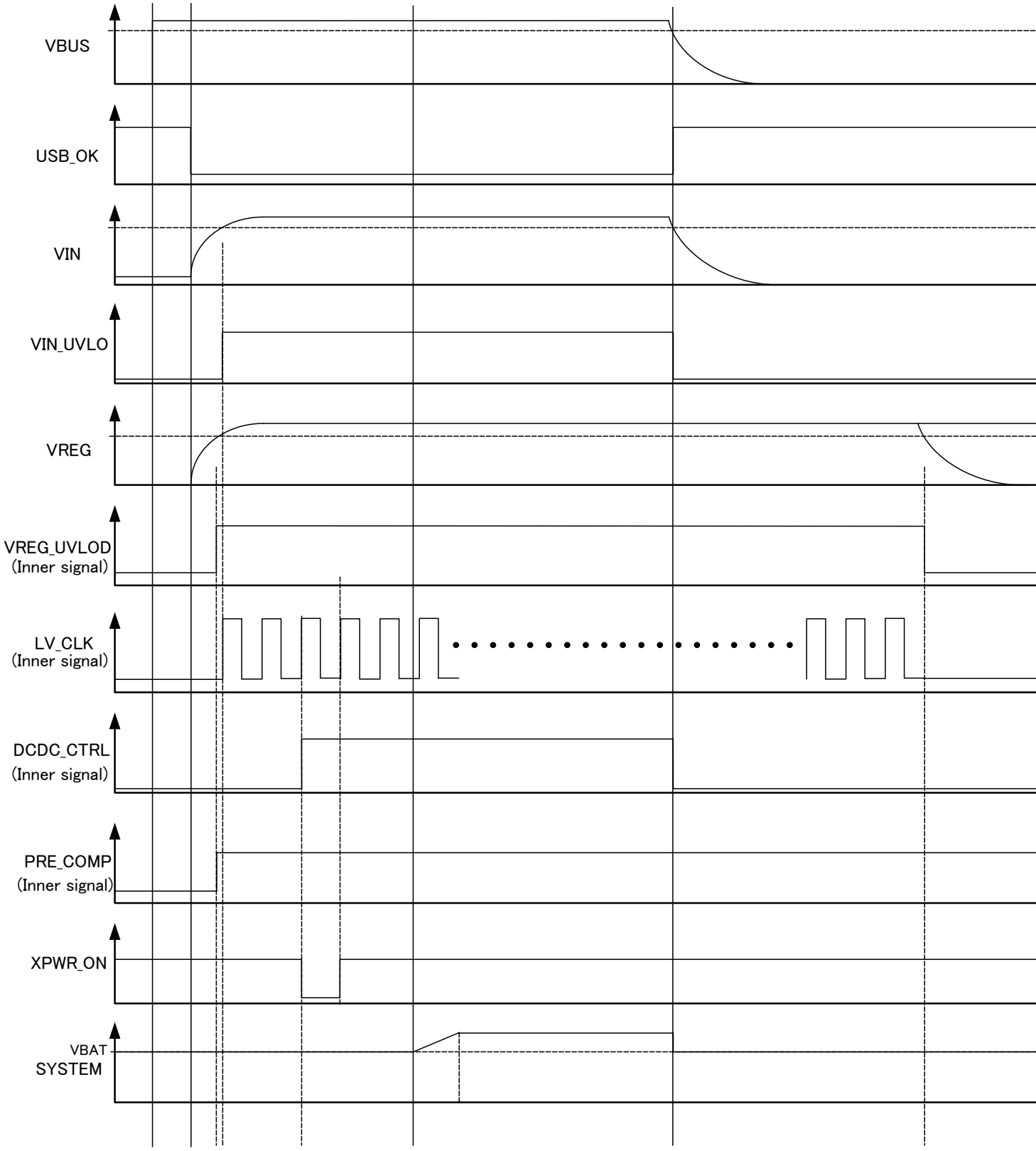
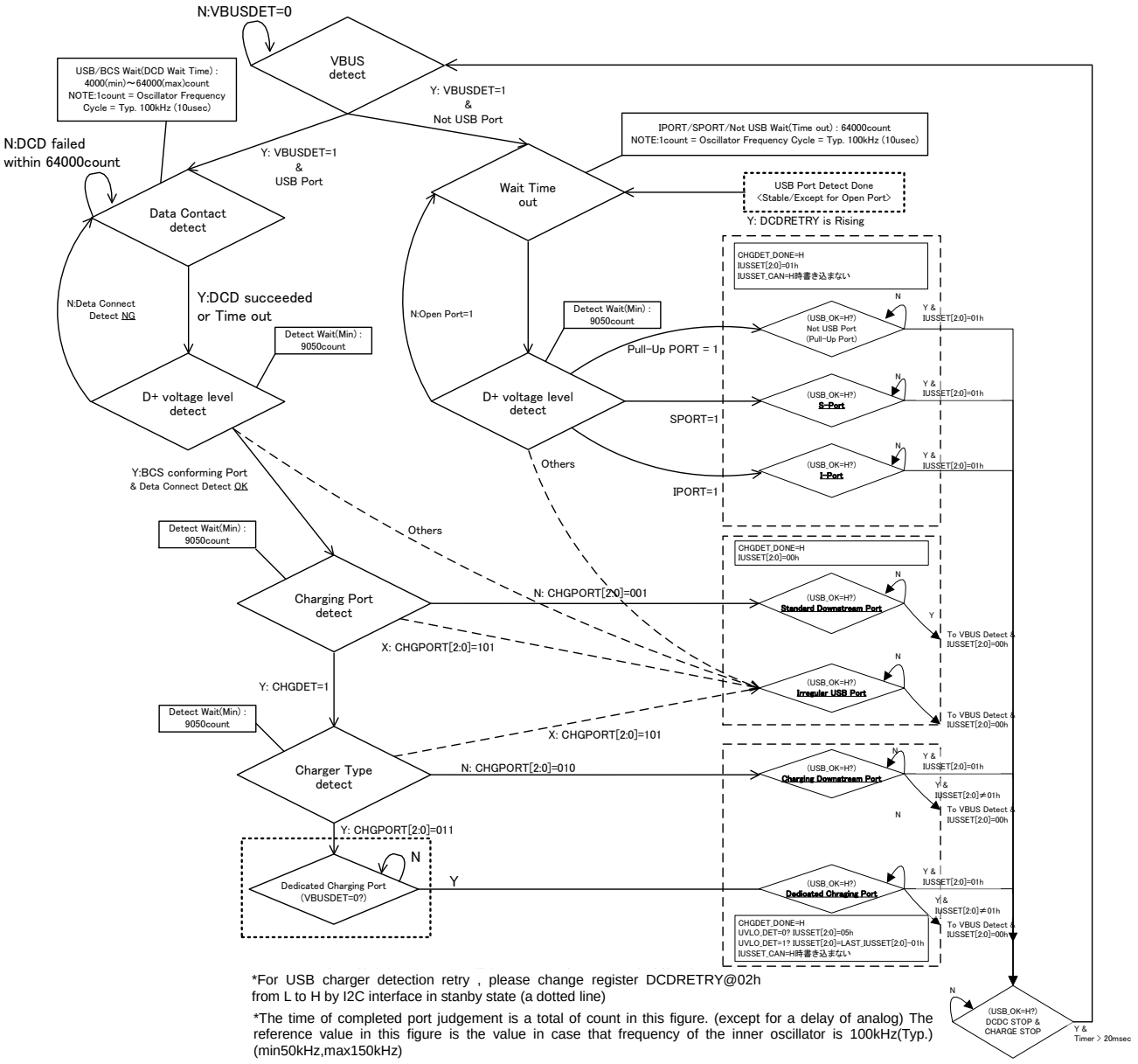


Figure 7. **Timing chart when USB is pulled out**

○ USB charger detection state transition diagram



*For USB charger detection retry , please change register DCDRETRY@02h from L to H by I2C interface in stanby state (a dotted line)

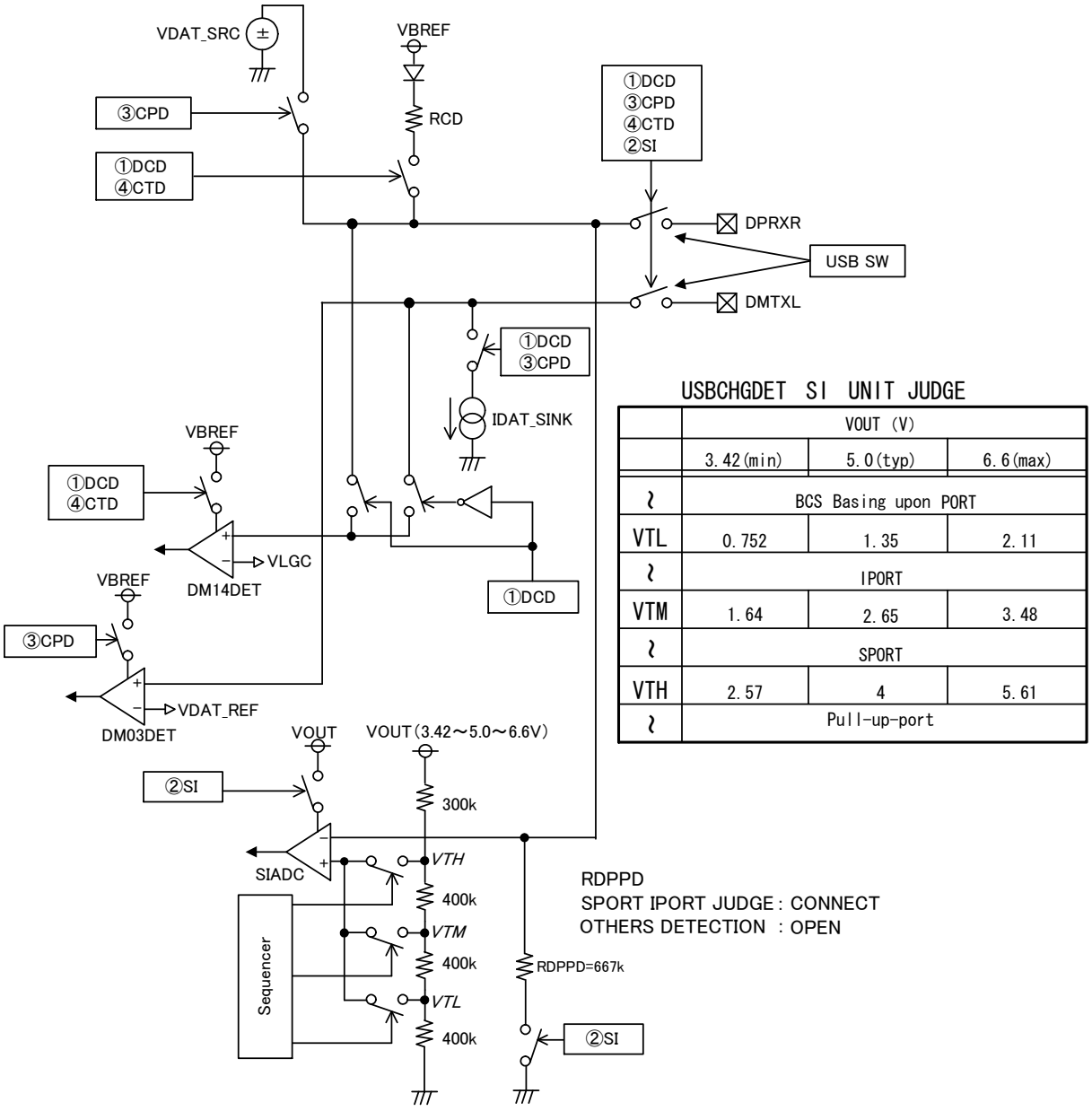
*The time of completed port judgement is a total of count in this figure. (except for a delay of analog) The reference value in this figure is the value in case that frequency of the inner oscillator is 100kHz(Typ.) (min50kHz,max150kHz)

Figure 8. USB charger detection state transition diagram

○ IUSSET Standard value when USB charger is detected

USB detection results	USBCHGDET[2:0] (I2C register)	IUSSET[2:0] (I2C resisitor)
IPORT	7h	1h
SPORT	6h	
SDP (Standard Downstream Port)	1h	0h
CDP (Charging Downstream Port)	3h	5h
DCP (Dedicated Charging Port)	2h	5h
Irregular USB Port	4h	0h
Pull-Up Port	5h	1h

○ USB charger detection block diagram



USBCHGDET SI UNIT JUDGE

	VOUT (V)		
	3.42(min)	5.0(typ)	6.6(max)
≀	BCS Basing upon PORT		
VTL	0.752	1.35	2.11
≀	IPORT		
VTM	1.64	2.65	3.48
≀	SPORT		
VTH	2.57	4	5.61
≀	Pull-up-port		

Figure 9. USB charger detection block diagram

○ **Timing chart of USB charger detector ①**

STANDARD DOWNSTREAM PORT (USB 1.0 / USB2.0)

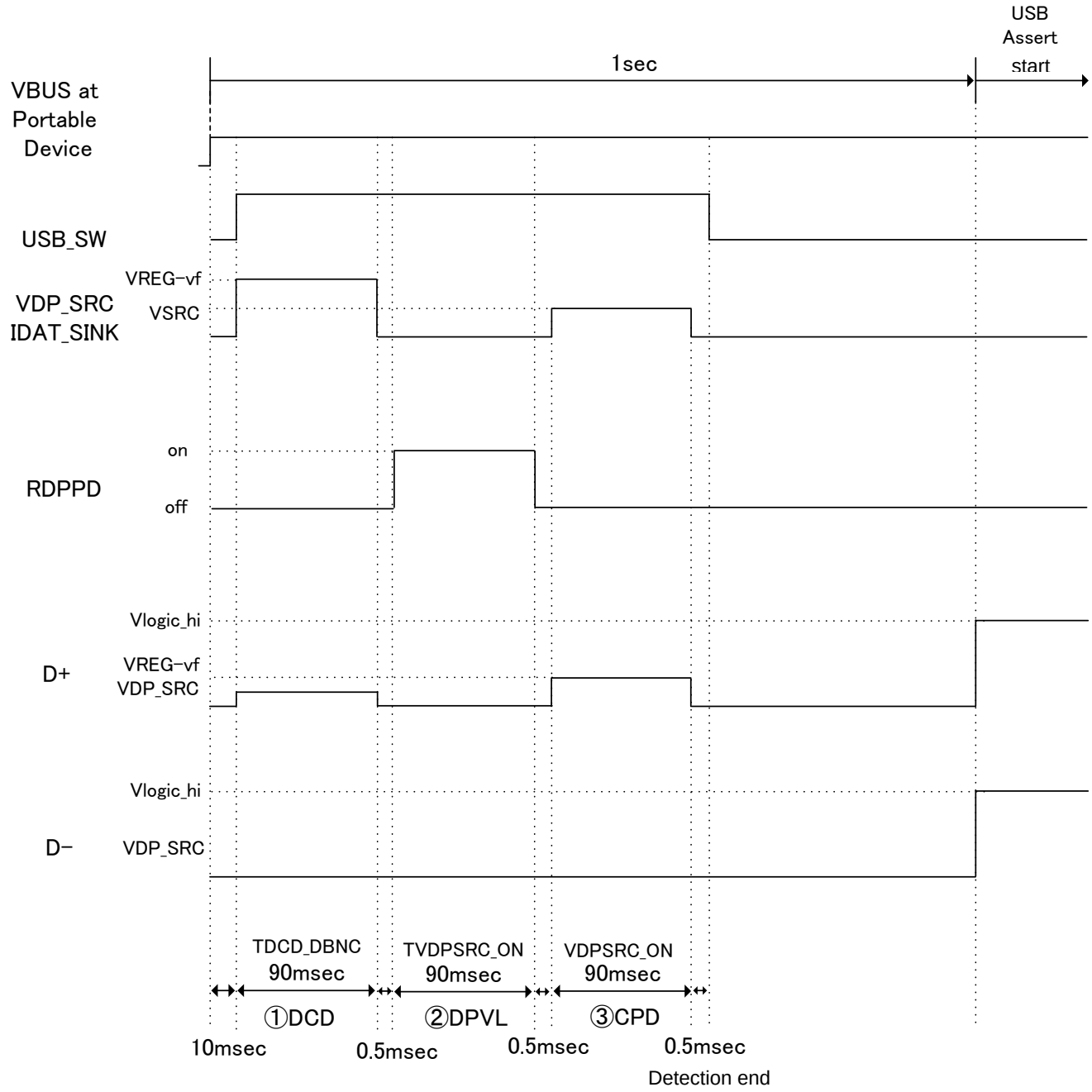
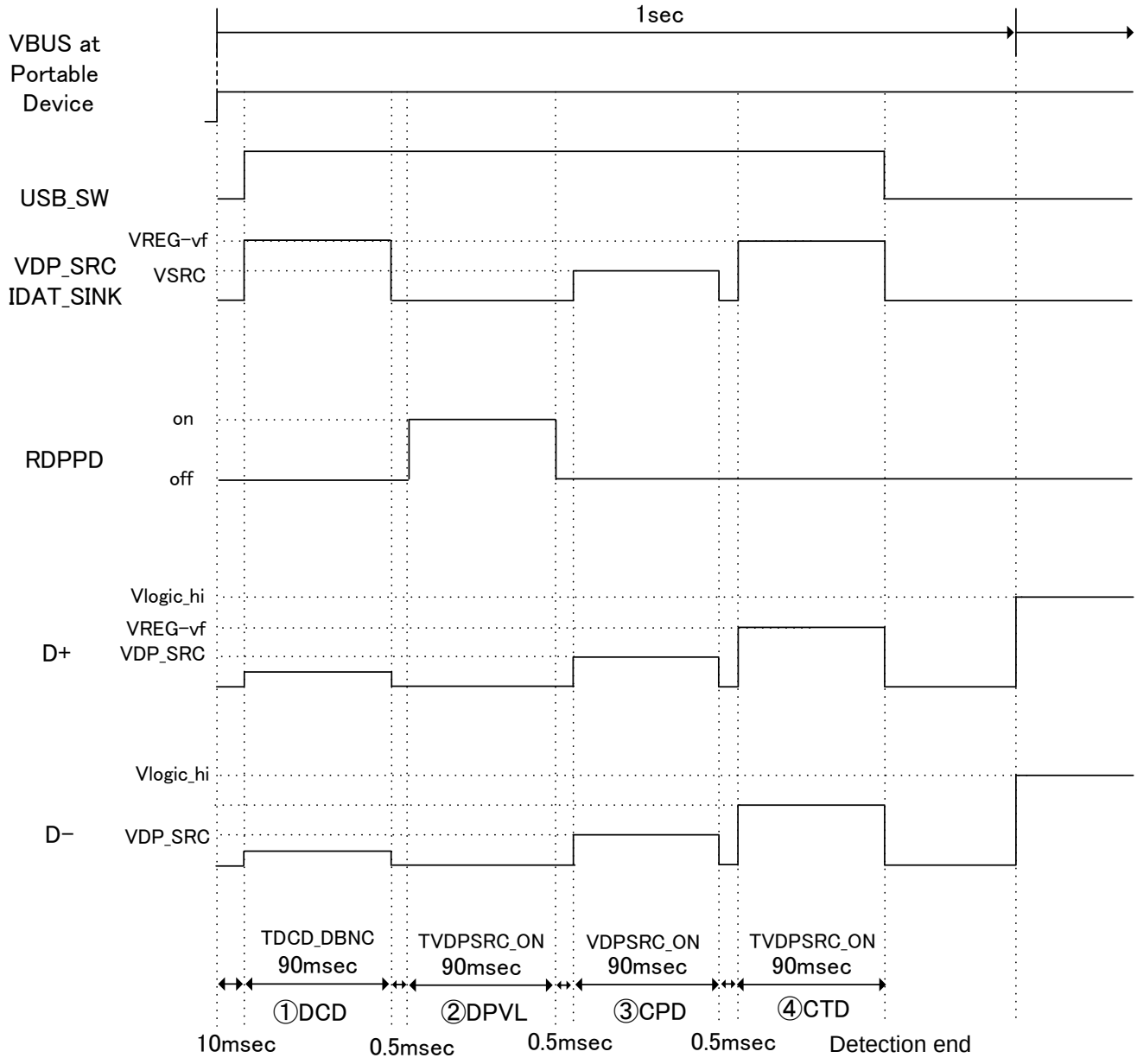


Figure 10. Standard downstream port detection timing chart

①DCD :Data Contact Detect
②DPVL :D+ Voltage Level detect
③CPD :Charging Port Detect
④CTD :Charging Type Detect

● **Timing chart of USB charger detector ②**

Dedicated charger Detection



①DCD :Data Contact Detect
②DPVL :D+ Voltage Level detect
③CPD :Charging Port Detect
④CTD :Charging Type Detect

● **Charge voltage, charge current, and temperature**

(1) The charge current will be switched after the temperature of the thermistor of the Li battery is detected by the TH terminal.

(In the case of the default settings)

Mode	Charge current
Fast charge current	400 mA
Low-temperature charging current	200 mA

The charge current is adjustable between 100 and 2000 mA at address 06h.
The low-temperature charting current will become half of the set value after the charge current is changed.

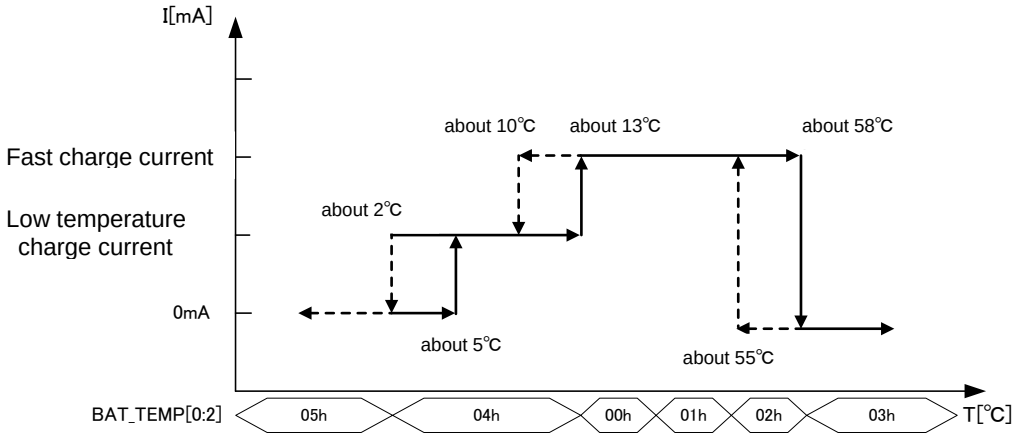


Figure 11. Relationship between battery temperature and charge current

(2) The charge control voltage will be switched after the temperature of the thermistor of the Li battery is detected by the TH battery upon completion of charge.

Thermistor detection voltage		Charge control voltage
①	2 ～ 45℃	4.200V
②	45 ～ 50℃	4.100V
③	50 ～ 58℃	4.050V

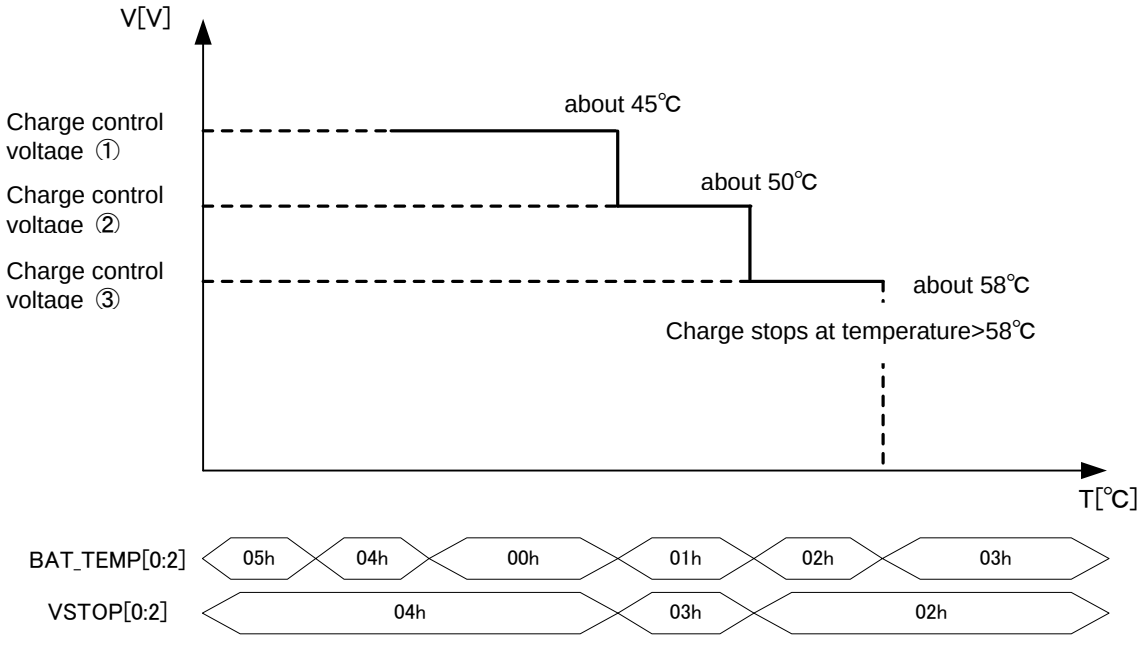


Figure12. Relationship between battery temperature and charge voltage

● CRG,FLT conditions at any states

	Adress		BAT_TEMP [2:0]	CRG	
	01h	02h		LED_FLIC[2:0] =0h	LED_FLIC[2:0] ≠0h
SUSPEND	00h	*	*	Turn off	Blink
Tricle CHARGE	01h	*	*	Turn off	Blink
PRE CHARGE	02h	*	*	Turn off	Blink
FAST CHARGE	03h	*	*	Turn off	Blink
TOP OFF	0Eh	*	*	Turn off	Blink
DONE	0Fh	*	*	Turn off	Blink
TempErr1,2,4,5[TERR]	10h,11h,14h	*	*	Blink with TERR	Turn off
TempErr3	12h	*	*	Turn off	Blink
TempErr4 [TERR]	13h	*	03h,05h	Blink with TERR	Turn off
TSD1,2,3,4,5	20h,21h,22h, 23h,24h	*	*	Turn off	Blink
Batt Assist1,2,3	30h,31h	*	*	Turn on	Blink
Batt Assist3	32h	*	*	Turn off	Blink
Batt Error(Over voltage)	7Fh	Conditions except for the following conditions	Conditions except for the following conditions	Blink with TERR_TOUT	Blink with TERR_TOUT
Batt Error(Over voltage) (No battery)	7Fh	Conditions except for the following conditions	07h	Turn off	Blink
Batt Error (Charge time out)	7Fh	01h, 02h, 03h, 0Eh	00h, 01h, 02h, 04h, 06h	Blink with BERR_TOUT	Blink with BERR_TOUT
Batt Error (Unusual temperature time out)	7Fh	10h, 11h	03h	Blink with BERR_TOUT	Blink with BERR_TOUT

● INT_B OUTPUT CONDITION

When interrupting is occurred, INT_OL=H, and INT_B =output of open drain.

	Occurring factor		Release factor
	External conditions	Inner process and register	
1	Charge state transition (00h,0Fh,10h,11h,12h,20h,21h,22h,23h,7Fh transition)	CHG_STAT transition	Address 01h read
2	Detection end of USB port	CHGPORT detection end	Address 03h read
3	VBUS UVLO detection	VBUS_UV=H→L	Address 04h read
4	VBUS UVLO release	VBUS_UV=L→H	Address 04h read
5	VBUS OVP detection	VBUS_OV=H→L	Address 04h read
6	VBUS OVP release	VBUS_OV=L→H	Address 04h read
7	When input current limit changes automatically	UVLO_DET=L→H VBUS_UV=H→L	Address 05h read
8	Battery detection	BAT_DET=L→H	Address 04h read
9	Battery dead (no battery) detection	BAT_DET=H→L	Address 04h read
10	Countercurrent detection(When VIN<VBAT)	ADD_LATCH=L→H	Address 04h read
11	SS_END	SS_END=L→H	Address 04h read
12	SCP Latch operation	SCP_LATCH=L→H	Address 04h read
13	VIN_UVLO detection	VIN_UV=H→L	Address 04h read
14	VIN_UVLO release	VIN_UV=L→H	Address 04h read
15	Thermistor detection	BAT_TEMP[2:0]= 07h→00h~06h	Address 03h read
16	No thermistor	BAT_TEMP[2:0]= 00h~06h→0h7	Address 03h read
17	XPWR_ON output	XPWR_COMPo=L→H	Address 01h read

● XPWR_ON OUTPUT CONDITION

When interrupting is occurred, XPWR_ON outputs. And XPWR_ON is output of open drain.

	Occurring factor		Release factor
	External conditions	Inner process and register	
1	CHGDET_DONE=H & XPWR_COMP=L→H & XPWR_ON_EN = L BAT_TEMP[2:0]=00h ～ 06h & BAT_DET=H & XPWR_RST=L	None	400msec wait or XPWR_RST=H

When XPWR_RST=L→H, output mask is latched.
Latch release condition

① VREG_UVLOD = L
② BATTEMP[2:0] = 07h or BATDET="0"

If VXPWR is changed by I2C when XPWR is masked, XPWR_ON outputs only one time when XPWR_COMPo= H after that.

XPWR_ON logic is not changed when USUS=H or USUS_reg=H.

● **IC peripheral parts setting method**

- **CTI oscillation frequency setting**

$$f_{CTI} = \frac{I_{CTI}}{C_{CTI} \times V_{CTI\_TH}} = \frac{8[\mu A]}{C_{CTI} \times 0.8[V]} = C_{CTI} \times 10^{-5}$$

■ Specifications of serial control unit

Recommended operation range

Item	Symbol	Standard value			Unit
		MIN	TYP	MAX	
VDD power voltage	VDD	2.7	-	3.6	V

● Electric characteristics (Ta=25℃ and VDD = 3.3 V unless otherwise specified)

Item	Symbol	Standard value			Unit	Condition
		MIN	TYP	MAX		
SCL、SDA						
H level input voltage	V_{INH}	VDD*0.7	-	VDD+0.3	V	
L level input voltage	V_{INL}	-0.3	-	VDD*0.3	V	
H level input current	I_{INH}	-10	-	10	μA	Input voltage ＝ 0.9 × VCC
L level input current	I_{INL}	-10	-	10	μA	Input voltage ＝ 0.1 × VCC
L level output voltage (SDA)	V_{OL}	-	-	0.4	V	I_{IN}=3.0mA
Bus line capacitive load	Cb	-	-	400	pF	

● AC timing characteristics (Ta=25℃ and VDD = 3.3 V unless otherwise specified)

Item	Symbol	FAST-MODE*			STANDARD-MODE*			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL frequency	fSCL	-	-	400	-	-	100	kHz
SCL CLK ”H” zone	fHIGH	0.6	-	-	4	-	-	μsec
SCL CLK ”L” zone	fLOW	1.3	-	-	4.7	-	-	μsec
SDA/SCL rise time	tR	-	-	0.3	-	-	1	μsec
SDA/SCL fall time	tF	-	-	0.3	-	-	1	μsec
Start condition hold time	tHD:STA	0.6	-	-	4	-	-	μsec
Start condition setup time	tSU:STA	0.6	-	-	4.7	-	-	μsec
Data hold time	tHD:DAT	0	-	0.9	0	-	3.45	μsec
Data setup time	tSU:DAT	100	-	-	250	-	-	nsec
Stop condition setup time	tSU:STO	0.6	-	-	4	-	-	μsec
Bus release time	tBUF	1.3	-	-	4.7	-	-	μsec
Noise filtering enable period	t1	0	-	50	0	-	50	nsec

Fast Mode and Standard Mode are modes defined by operation speed.
Operation at 100 kHz is called Standard Mode, whereas operation at 400 kHz is called Fast Mode.
Since these operation frequencies are specified maximum frequencies, the IC can operate with a 100-kHz clock, for example, in Fast Mode.

● Serial data timing

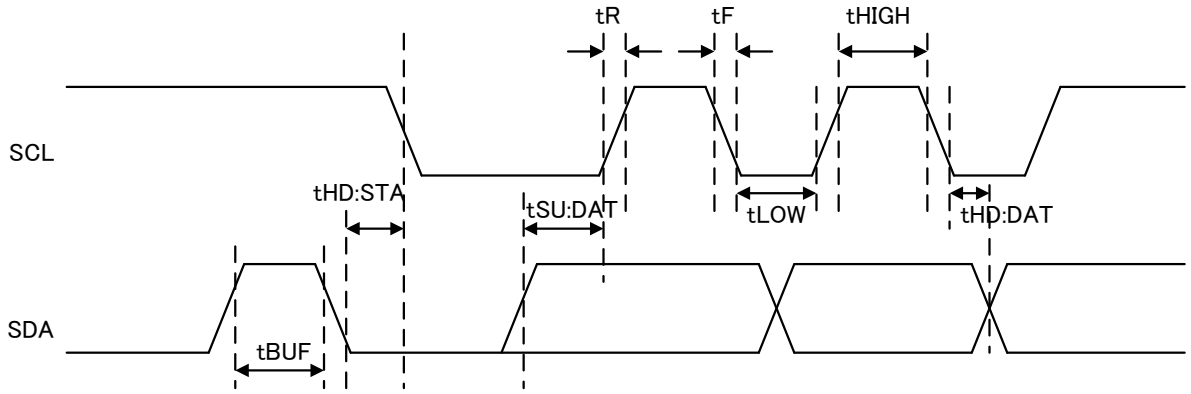


Figure 13. Serial data timing

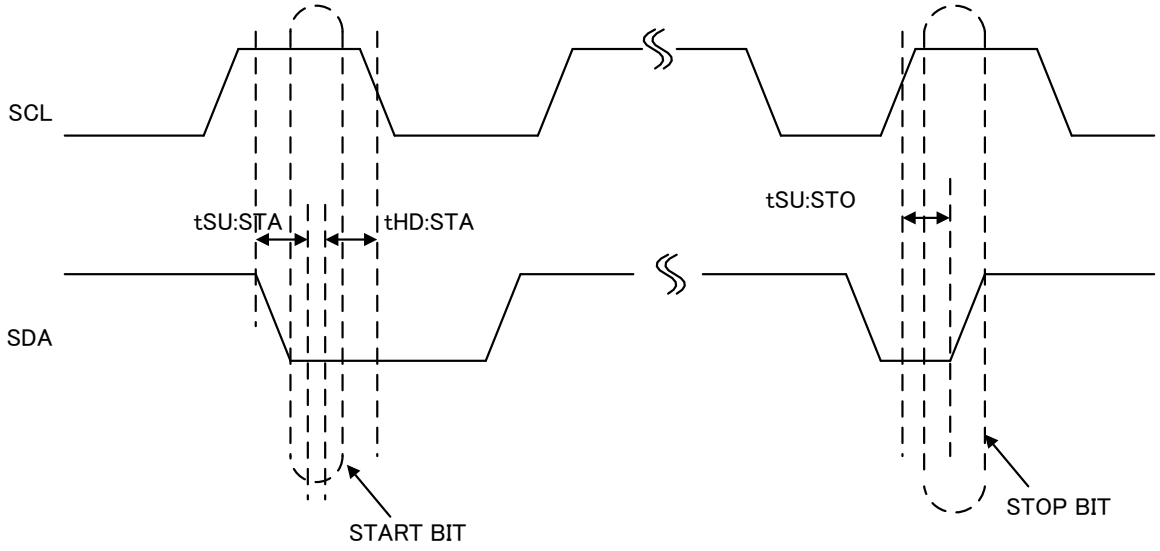


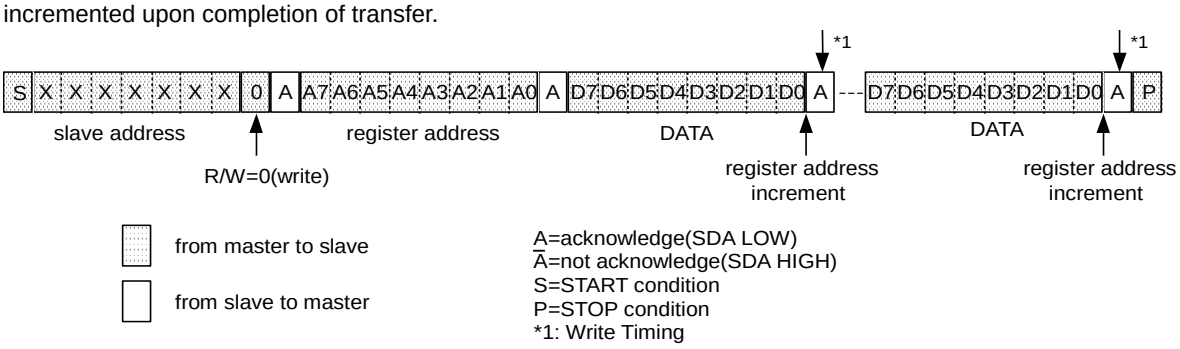
Figure 14. Start bit and stop bit timing

● **Serial I/F read/write**

1. Write protocol

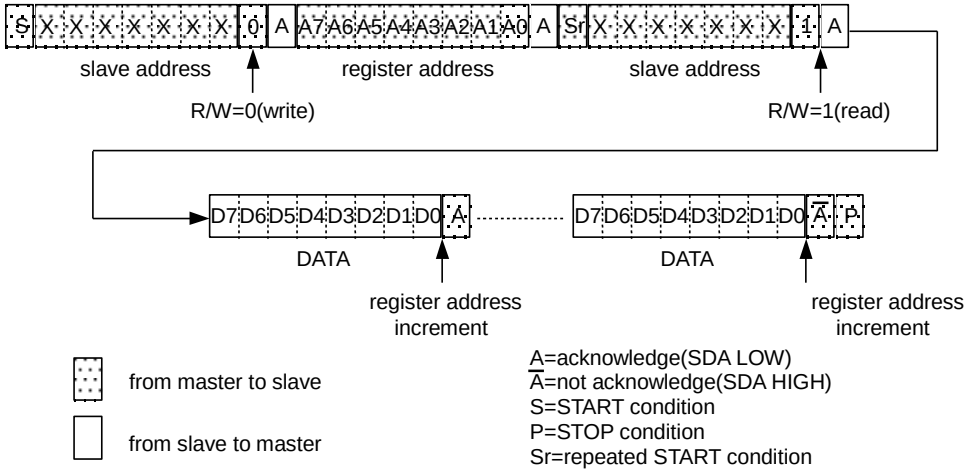
Shown below is the write protocol. Data is transferred, consisting of a slave address and the subsequent byte representing a transferred write instruction.

The third byte writes the data in the internal register written in the second byte, and the register addresses are automatically incremented in the fourth and following bytes. Note, however, that the data at 00h will be transferred in the transfer of the data in the next byte after the last register address is reached. The addresses will have been incremented upon completion of transfer.



2. Composite read protocol

After an internal address is designated, the direction of data transfer is changed by generating a repetitive start condition, and data is read. Data of incremented addresses is read thereafter. After the data at the last address is read, the data at 00h will be read as data read from the next byte. The addresses will have been incremented upon completion of transfer.



*In the composite read protocol, do not fail to set A (not acknowledge) after the last data is read.
If data read is completed with A (acknowledge), the operation will stop in the data read state (if the read data at that time is 0, the operation will stop with SDA in the L level output state). However, if SCL is activated in this state to read data and A (not acknowledge) is set, regular operation will be recovered.

● **Slave address**

Slave address
0110001

● Register map

Description of symbols

- W: Writable register
- R: Readable register
- R/W: Readable and writable register
- ー: Write-protected register (bit that writes “0”)

Address	Address name	Address	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
00h	SFTRST	R/W	-	-	-	-	-	-	-	SFTRST	00h	Software reset control
01h	CHG_STAT	R	CHG_STATE[7:0]								00h	Current state
02h	LAST_ST	R	LAST_STATE[7:0]								00h	Preceding state
03h	STAT1	R	BATDET_DONE	BAT_TEMP[2:0]			CHGDET_DONE	USBCHGDET[2:0]			70h	Expression of the states 1
04h	STAT2	R	UVLO_DET	ADD_LTCH	SCP_LTCH	SS_END	VIN_UV	VBUS_UV	VBUS_OV	BAT_DET	00h	Expression of the states 2
05h	CHGSET1	(*1)	-	IUSSET[2:0]			-	LAST_IUSSET[2:0]			00h	Setting of input current limits
06h	CHGSET2	R/W	INTBEN	XPWR_ON_EN			IUSSET_CAN	REDCD	CEN	USUS	20h	Settings 1
07h	CHGSET3	R/W	-	-	-	BATDC_EN	COLD_EN	COLD_ERR_EN	USB_SW_EN	USB_SW	1Ch	Settings 2
08h	CHGSET4	R/W	VSTOP[2:0]			-	IFST[3:0]				84h	Full charge voltage or fast charge current setting
09h	CHGSET5	R/W	VXPWR[2:0]			IPRE[4:0]					05h	Pre charge current setting
0Ah	CHGSET6	R/W	-	VOVP[1:0]		-	ITOPOFF[3:0]				06h	Over voltage or full charge current setting
0Bh	CHGSET7	R/W	LED_FLIC[2:0]			-	VPRE[3:0]				05h	Pre charge voltage setting
0Ch	LEDSET1	R/W	VSYS[1:0]		BERR_TOUT[2:0]		TERR_TOUT[2:0]				5Bh	LED blink setting
0Dh	LEDSET2	R/W	-	-	BERR_OVP[2:0]		TERR[2:0]				1Bh	LED blink setting

Register reset conditions:

① When VREG_UVLO = L
② When “1” is written in D0 of address 00h

If even either of conditions ① and ② is fulfilled, all registers will be reset.

③ VREG_UVLO = L(Reset address 04hD4-D6)
④ USB_PG=L(Address 03h D3、03h D2-D0、04h D2、05h D5-D4、07h D0)
⑤ BAT_TEMP=07h or BATDET=”0”(Address 09hD7-D5)

Input “0” in “-.” Each empty register is used as a register for IC tests. The IC test enter test mode if “1” is written in “-.” Send “0” to each register marked with “-“ at the time of data transmission.

During data read from an external unit, two-line serial communication timing and IC internal operation timing become asynchronous.
Take a proper measure against it, such as the introduction of a three-time matching sequence, to prevent problems with the application.

(*1) Address 05h is LAST_IUSSET[1:0]、UVLO_DET is Read Only.IUSSET[1:0] is R/W.

● **Register map(TEST MODE)**

Attention about marks

- W is a register which can be written.
- R is a register which can be read.
- R/W is a register which can be written or read.
- ― is a register which can't be written.(bit for '0')

address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0Eh	TEST1	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE1
0Fh	TEST2	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE2
10h	TEST3	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE3
11h	TEST4	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE4
12h	TEST5	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE5
13h	TEST6	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE6
14h	TEST7	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE7
15h	TEST8	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE8
16h	TEST9	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE9
17h	TEST10	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE10
18h	TEST11	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE11
19h	TEST12	R/W	-	-	-	-	-	-	-	-	00h	TEST MODE12

Register reset conditions:

① VREG_UVLOD = L
② When D0 of address 00h is '1'

If ① or ② is detected, all register are reset.

Please input "0" to "-".Blank registers are used as registers for test.
If you write "1" to "-" register , a state move to test mode, so please send "0" to "-" register while data sending.

● **Detailed description of registers 1**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Description of data
00h	SFTRST	W	-	-	-	-	-	-	-	SFTRST	00h	Software reset control input

D0: SFTRST Software reset
'0': Reset canceled (default)
'1': Reset → Reset will be automatically canceled with a single shot pulse.

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Description of data
01h	CHG_STAT	R	CHG_STATE[7:0]								00h	Current state

D7-D0: CHG_STAT[7:0] Signal that indicates the current state

Data (hexadecimal)	Data (binary)								State	Description
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0	0	0	0	0	0	0	0	SUSPEND	Standby state
01h	0	0	0	0	0	0	0	1	Tricle CHARGE	Tricle-charge state
02h	0	0	0	0	0	0	1	0	PRE CHARGE	Pre-charge state
03h	0	0	0	0	0	0	1	1	FAST CHARGE	Fast charge state
0Eh	0	0	0	0	1	1	1	0	TOP OFF	Full charge detection state
0Fh	0	0	0	0	1	1	1	1	DONE	Charge complete state
10h	0	0	0	1	0	0	0	0	Temp Err 1	Battery temperature during pre-charge: 2℃ or below and 58℃ or over
11h	0	0	0	1	0	0	0	1	Temp Err 2	Battery temperature during fast charge: 2℃ or below and 58℃ or over
12h	0	0	0	1	0	0	1	0	Temp Err 3	Battery temperature when charge is completed: 2℃ or below and 58℃ or over
13h	0	0	0	1	0	0	1	1	Temp Err 4	Battery temperature during charge is suspend: 2℃ or below and 58℃ or over
14h	0	0	0	1	0	1	0	0	Temp Err 5	Battery temperature during tricle charge: 2℃ or below and 58℃ or over
20h	0	0	1	0	0	0	0	0	TSD 1	Unusual chip temperature during pre-charge (175℃ or over Typ)
21h	0	0	1	0	0	0	0	1	TSD 2	Unusual chip temperature during fast-charge (175℃ or over Typ)
22h	0	0	1	0	0	0	1	0	TSD 3	Unusual chip temperature during full-charge (175℃ or over Typ)
23h	0	0	1	0	0	0	1	1	TSD 4	Unusual chip temperature during pre-charge (175℃ or over Typ)
24h	0	0	1	0	0	1	0	0	TSD 5	Unusual chip temperature during tricle-charge (175℃ or over Typ)
30h	0	0	1	1	0	0	0	0	BATT ASSIST 1	System < VBAT state during fast charge
31h	0	0	1	1	0	0	0	1	BATT ASSIST 2	System < VBAT state during fast charge
32h	0	0	1	1	0	0	1	0	BATT ASSIST 3	System < VBAT state during full charge
7Fh	0	1	1	1	1	1	1	1	BattError	Battery error state

is default.

● **Detailed description of registers 2**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Description of data
02h	LAST_ST	R	LAST_STATE[7:0]								00h	Preceding state

D7-D0: LAST_STATE[7:0] Signal that indicates the state just before CHG_STATE [7:0]

Data (hexadecimal)	Data (binary)								State	Description
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	0	0	0	0	0	0	0	0	SUSPEND	Standby state
01h	0	0	0	0	0	0	0	1	Tricle CHARGE	Tricle-charge state
02h	0	0	0	0	0	0	1	0	PRE CHARGE	Pre-charge state
03h	0	0	0	0	0	0	1	1	FAST CHARGE	Fast charge state
0Eh	0	0	0	0	1	1	1	0	TOP OFF	Full charge detection state
0Fh	0	0	0	0	1	1	1	1	DONE	Charge complete state
10h	0	0	0	1	0	0	0	0	Temp Err 1	Battery temperature during pre-charge: 2℃ or below and 58℃ or over
11h	0	0	0	1	0	0	0	1	Temp Err 2	Battery temperature during fast charge: 2℃ or below and 58℃ or over
12h	0	0	0	1	0	0	1	0	Temp Err 3	Battery temperature when charge is completed: 2℃ or below and 58℃ or over
13h	0	0	0	1	0	0	1	1	Temp Err 4	Battery temperature when state is suspend: 2℃ or below and 58℃ or over
14h	0	0	0	1	0	1	0	0	Temp Err 5	Battery temperature during tricle-charge: 2℃ or below and 58℃ or over
20h	0	0	1	0	0	0	0	0	TSD 1	Unusual chip temperature during pre-charge (175℃ or over Typ)
21h	0	0	1	0	0	0	0	1	TSD 2	Unusual chip temperature during fast-charge (175℃ or over Typ)
22h	0	0	1	0	0	0	1	0	TSD 3	Unusual chip temperature during full-charge (175℃ or over Typ)
23h	0	0	1	0	0	0	1	1	TSD 4	Unusual chip temperature during pre-charge (175℃ or over Typ)
24h	0	0	1	0	0	1	0	0	TSD 5	Unusual chip temperature during tricle-charge (175℃ or over Typ)
30h	0	0	1	1	0	0	0	0	BATT ASSIST 1	System < VBAT state during fast charge
31h	0	0	1	1	0	0	0	1	BATT ASSIST 2	System < VBAT state when full charge is detected
32h	0	0	1	1	0	0	1	0	BATT ASSIST 3	System < VBAT state during full charge
7Fh	0	1	1	1	1	1	1	1	BattError	Battery error state

: Default

When a state change to fast-charge state (03h) from pre-charge state (02h), a last state is sometimes full-charge state (0E).

● **Detailed description of registers 3**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Description of data
03h	STAT1	R	BATDET_DONE	BAT_TEMP[2:0]			CHGDET_DONE	USBCHGDET[2:0]			70h	Display of states

D2-D0: USBCHGDET[2:0] Signal that indicates the result of USB charger detection

Data (hexadecimal)	Data (binary)			State	Description
	D2	D1	D0		
00h	0	0	0	Not USB Port	default
01h	0	0	1	SDP Port	Standard Downstream Port
02h	0	1	0	DCP Port	Dedicated Charge Port
03h	0	1	1	CDP Port	Charging Downstream Port
04h	1	0	0	OPEN Port	Open Port
05h	1	0	1	Pull-Up Port	Pull-Up Port
06h	1	1	0	S - Port	Sony Charger USB Port
07h	1	1	1	I - Port	Apple Charger USB Port

: Default

D3: CHGDET_DONE USB charge detection end flag
'0': USB charger is not detected (default)
'1': USB charger detection is finished

D5-D3: BAT_TEMP[2:0] Signal that indicates the temperature of the battery

Data (hexadecimal)	Data (binary)			State	Description
	D6	D5	D4		
00h	0	0	0	Room Temp	45℃>Ta>10℃
01h	0	0	1	HOT1	50℃>Ta>45℃
02h	0	1	0	HOT2	58℃>Ta>50℃
03h	0	1	1	HOT3	Ta>58℃
04h	1	0	0	COLD1	2℃<Ta<10℃
05h	1	0	1	COLD2	Ta<2℃
06h	1	1	0	Disable	Temperature control disenable (TH terminal pull-down)
07h	1	1	1	Battery open	When the battery is open（TH terminal Pull-Up）

: Default

D7: BATDET_DONE Battery detection end flag
'0': Battery is not detected or searched(default)
'1': Battery detection is finished

● **Detailed description of registers 4**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
04h	STAT2	R	UVLO_DET	ADD_LTCH	SCP_LTCH	SS_END	VIN_UV	VBUS_UV	VBUS_OV	BAT_DET	00h	Display of states

D0: BAT_DET
Battery detection flag
'0': Battery is not detected(default)
'1': Battery is detected

D1: VBUS_OV
VBUS OVP detection
'0': VBUS OVP is not detected(default)
'1': VBUS OVP is detected

D2: VBUS_UV
VBUS UVLO detection
'0': VBUS UVLO is detected(default)
'1': VBUS UVLO is not detected

D3: VIN_UV
VIN_UVLO detection
'0': VIN UVLO is detected(default)
'1': VIN UVLO is not detected

D4: SS_END
SS_END detection
'0': SS_END is not detected(default)
'1': SS_END is detected

D5: SCP_LATCH
SCP detection
'0': SCP is not detected(default)
'1': SCP is detected

D6: ADD_LATCH
Countercurrent detection（VIN<VBAT detection）
'0': Countercurrent is not detected(default)
'1': Countercurrent is detected

D7: UVLO_DET
Input current automatically change flag
'0': Input current automatically change is not detected(default)
'1': Input current automatically change is detected

● **Detailed description of registers 5**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
05h	CHGSET1	R/W	-	IUSSET[2:0]			-	LAST_IUSSET[2:0]			00h	Display of states

D1-D0: LAST_IUSSET[2:0] Signals that display a preceding state of VBUS input current limit

Data (hexadecimal)	Data (binary)			State	Description	External terminal setting	
	D2	D1	D0			IUSSET2	IUSSET1
00h	0	0	0	90mA	Input current limited to 90 mA	0	0
01h	0	0	1	480mA	Input current limited to 480 mA	0	1
02h	0	1	0	690mA	Input current limited to 690 mA	-	-
03h	0	1	1	860mA	Input current limited to 860 mA	1	0
04h	1	0	0	1140mA	Input current limited to 1140 mA	-	-
05h	1	0	1	1420mA	Input current limited to 1420 mA	1	1
06h	1	1	0	1890mA	Input current limited to 1890 mA	-	-
07h	1	1	1	infinity	Input current is not limited	-	-

は初期値

D5-D4: IUSSET[2:0] Signals that display or change a state of VBUS input current limit

Data (hexadecimal)	Data (binary)			State	Description	External terminal setting	
	D2	D1	D0			IUSSET2	IUSSET1
00h	0	0	0	90mA	Input current limited to 90 mA	0	0
01h	0	0	1	480mA	Input current limited to 480 mA	0	1
02h	0	1	0	690mA	Input current limited to 690 mA	-	-
03h	0	1	1	860mA	Input current limited to 860 mA	1	0
04h	1	0	0	1140mA	Input current limited to 1140 mA	-	-
05h	1	0	1	1420mA	Input current limited to 1420 mA	1	1
06h	1	1	0	1890mA	Input current limited to 1890 mA	-	-
07h	1	1	1	infinity	Input current is not limited	-	-

: Default

● **Detailed description of registers 6**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
06h	CHGSET2	R/W	INTBEN	XPWR_ON_EN	-	-	IUSSET_CAN	REDCD	CEN	USUS	20h	Setting states

D0: USUS Charger state transition diagram : SUSPEND and DC/DC OFF
'0': Regular operation(default)
'1': SUSPEND＆DCDC_CTRL=L

D1: CEN Charger state transition diagram : SUSPEND and DC/DC ON
'0': Regular operation(default)
'1': SUSPEND＆DCDC_CTRL=H

D2: REDCD USB charger redetection (restart at PosEdge: R/W)
'0': Not restart (default)
'1': Restart (PosEdge)

To make a restart when the register value is "1," write "0" in the register, and then write "1" again.
Disregard this setting in all cases, except when CHGDET_DONE is H.

D3: IUSSET_CAN IUSSET write protect flag (R/W)
'0': With IUSSET write sequence (default)
'1': Without IUSSET write sequence

D6: XPWR_ON_EN XPWR_ON terminal output enable control
'0': With XPWR_ON signal output(default)
'1': Without XPWR_ON signal output

D7: INTBEN INT_B terminal output enable control
'0': With interruption signal (default)
'1': Without interruption signal

● **Detailed description of registers 7**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
07h	CHGSET3	R/W	-	-	-	BATDC_EN	COLD_EN	COLD_ERR_EN	USB_SW_EN	USB_SW	1Ch	Setting states

D0: USB_SW USB_SW exchange control
‘0’: USB_SW OPEN(default)
‘1’: USB_SW CLOSE

D1: USB_SW_EN USB_SW automatically change enabling control
‘0’: USB_SW automatically change : invalid(default)
‘1’: USB_SW automatically change :valid

D2: COLD_ERR_EN Timeout function at low temperature enabling control
‘0’: Invalid
‘1’: Valid(default)
Set the timer counter at a unusual low temperature to valid
Set the charge timer counter value at low temperature to double

D3: COLD_EN 1/2 charge current at low temperature enabling control
‘0’: Invalid
‘1’: Valid(default)

D4: BATDC_EN DC/DC enabling control when a battery doesn’t exsist.
‘0’: Invalid
‘1’: Valid(default)

● **Detailed description of registers 8**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Description of data
08h	CHGSET4	R/W	VSTOP[2:0]			-	IFST[3:0]				84h	Setting of full charge voltage Setting of fast charge current
09h	CHGSET5	R/W	VXPWR[2:0]			IPRE[4:0]					05h	Setting of pre-charge current
0Ah	CHGSET6	R/W	-	VOVP[1:0]		-	Setting of over-charge voltage Setting of full charge current				06h	Setting of over-charge voltage Setting of full charge current

Data					Set value					
D4	D3	D2 D7	D1 D6	D0 D5	IFAST [D3～D0]	IPRE [D4～D0]	VXPWR [D7～D5]	VSTOP [D7～D5]	VOVP [D6～D5]	ITOPOFF [D3～D0]
0	0	0	0	0	200mA	10mA	3.200V	3.900V	4.350V	20mA
0	0	0	0	1	250mA	20mA	3.500V	4.000V	4.450V	30mA
0	0	0	1	0	300mA	30mA	3.600V	4.050V	4.450V	40mA
0	0	0	1	1	350mA	40mA	3.700V	4.100V	4.450V	50mA
0	0	1	0	0	400mA	50mA	3.800V	4.200V	-	60mA
0	0	1	0	1	450mA	60mA	3.900V	4.350V	-	70mA
0	0	1	1	0	500mA	70mA	4.000V	4.350V	-	80mA
0	0	1	1	1	550mA	80mA	4.100V	4.350V	-	90mA
0	1	0	0	0	600mA	90mA		-	-	100mA
0	1	0	0	1	650mA	100mA		-	-	100mA
0	1	0	1	0	700mA	110mA		-	-	100mA
0	1	0	1	1	750mA	120mA		-	-	100mA
0	1	1	0	0	800mA	130mA		-	-	100mA
0	1	1	0	1	800mA	140mA		-	-	100mA
0	1	1	1	0	800mA	150mA		-	-	100mA
0	1	1	1	1	800mA	160mA		-	-	100mA
1	0	0	0	0	-	170mA		-	-	-
1	0	0	0	1	-	180mA		-	-	-
1	0	0	1	0	-	190mA		-	-	-
1	0	0	1	1	-	200mA		-	-	-
1	0	1	0	0	-	200mA		-	-	-
1	0	1	0	1	-	200mA		-	-	-
1	0	1	1	0	-	200mA		-	-	-
1	0	1	1	1	-	200mA		-	-	-
1	1	0	0	0	-	200mA		-	-	-
1	1	0	0	1	-	200mA		-	-	-
1	1	0	1	0	-	200mA		-	-	-
1	1	0	1	1	-	200mA		-	-	-
1	1	1	0	0	-	200mA		-	-	-
1	1	1	0	1	-	200mA		-	-	-
1	1	1	1	0	-	200mA		-	-	-
1	1	1	1	1	-	200mA		-	-	-

: Default

● **Detailed description of registers 9**

Address	Address name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default	Function
0Bh	CHGSET7	R/W	LED_FLIC[2:0]			-	VPRE[3:0]				05h	Setting of pre-charge voltage
0Ch	LEDSET1	R/W	VSYS[1:0]		BERR_TOUT[1:0]			TERR_TOUT[2:0]			5Bh	LED blink setting
0Dh	LEDSET2	R/W			BERR_OVP[1:0]			TERR[1:0]			1Bh	LED blink setting

data				Set value	
D3	D2	D1 D7	D0 D6	VPRE [D3～D0]	VSYS [D7～D6]
0	0	0	0	2.300V	VREG+275mV
0	0	0	1	2.400V	VREG+25mV
0	0	1	0	2.500V	VREG-15mV
0	0	1	1	2.600V	VREG-225mV
0	1	0	0	2.700V	-
0	1	0	1	2.800V	-
0	1	1	0	2.900V	-
0	1	1	1	3.000V	-
1	0	0	0	3.100V	-
1	0	0	1	3.200V	-
1	0	1	0	3.300V	-
1	0	1	1	3.400V	-
1	1	0	0	3.400V	-
1	1	0	1	3.400V	-
1	1	1	0	3.400V	-
1	1	1	1	3.400V	-

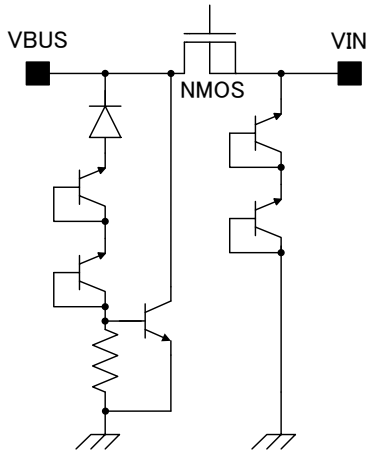
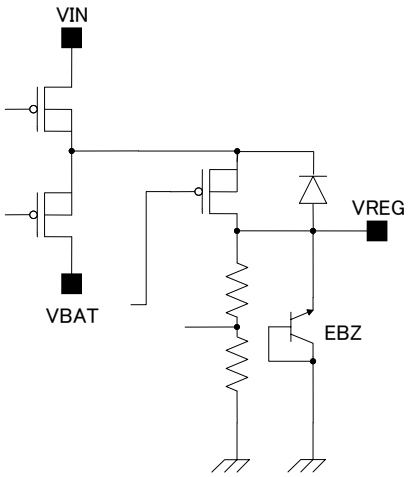
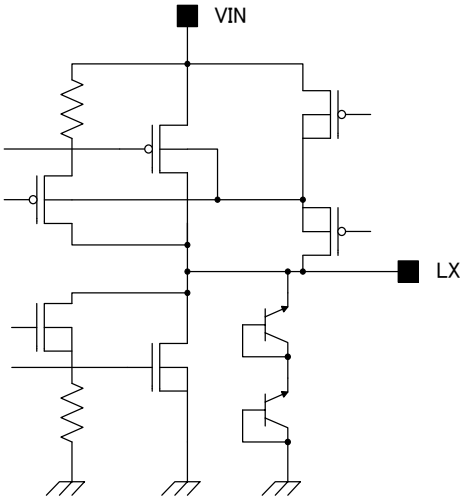
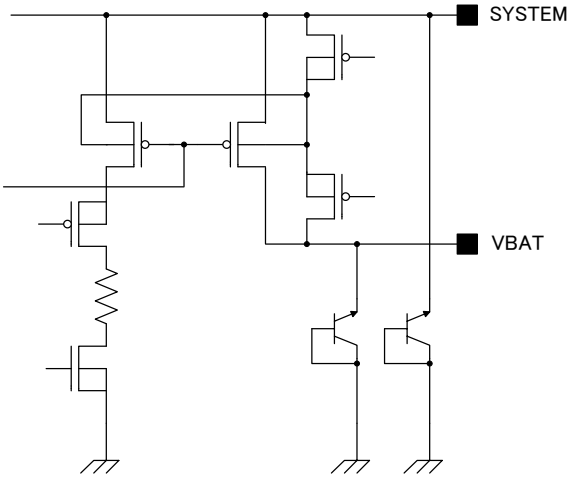
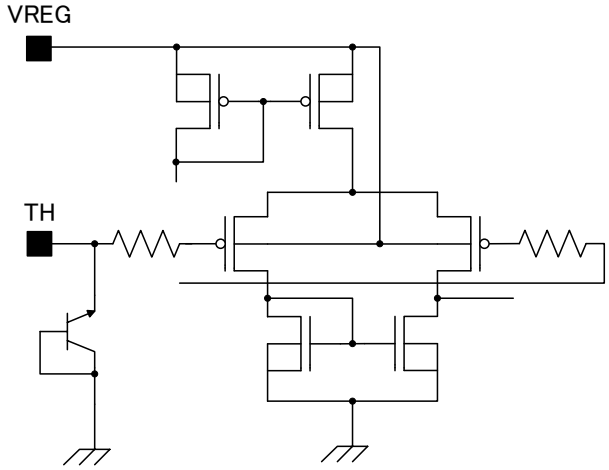
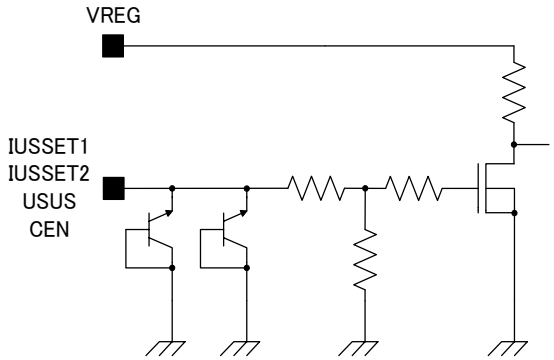
data			Set value				
D2 D5 D7	D1 D4 D6	D0 D3 D5	LED_FLIC [D7～D5]	TERR [D2～D0]	BERR_OVP [D5～D3]	BERR_TOUT [D5～D3]	TERR_TOUT [D2～D0]
0	0	0	Forced ON Invalid	Turn on	Turn on	Turn on	Turn on
0	0	1	Turn on	0.125 Hz	0.125 Hz	0.125 Hz	0.125 Hz
0	1	0	0.25Hz	0.25 Hz	0.25 Hz	0.25 Hz	0.25 Hz
0	1	1	0.5Hz	0.5 Hz	0.5 Hz	0.5 Hz	0.5 Hz
1	0	0	0.6 Hz	0.6 Hz	0.6 Hz	0.6 Hz	0.6 Hz
1	0	1	1 Hz	1 Hz	1 Hz	1 Hz	1 Hz
1	1	0	6 Hz	6 Hz	6 Hz	6 Hz	6 Hz
1	1	1	Turn off	Turn off	Turn off	Turn off	Turn off

: Default

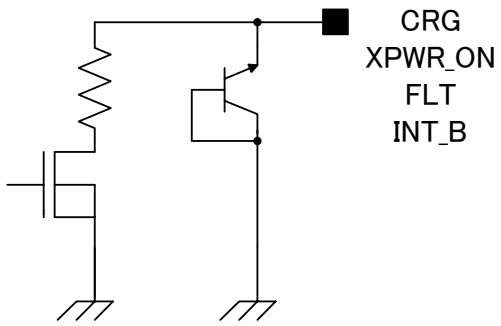
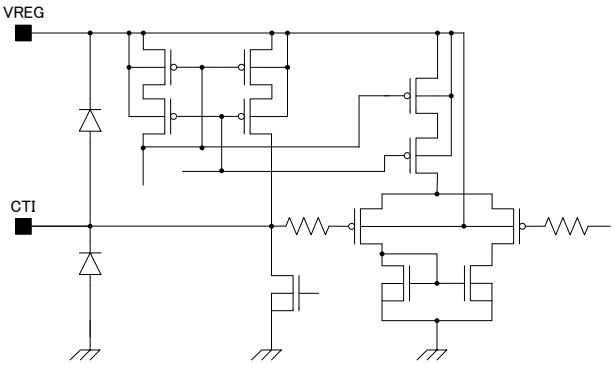
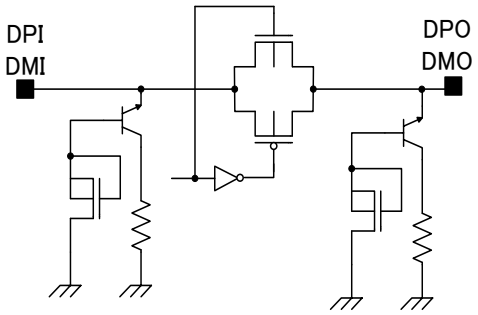
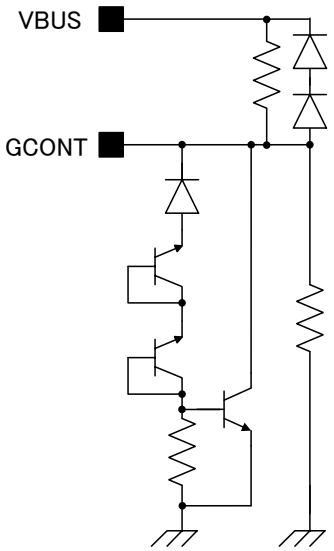
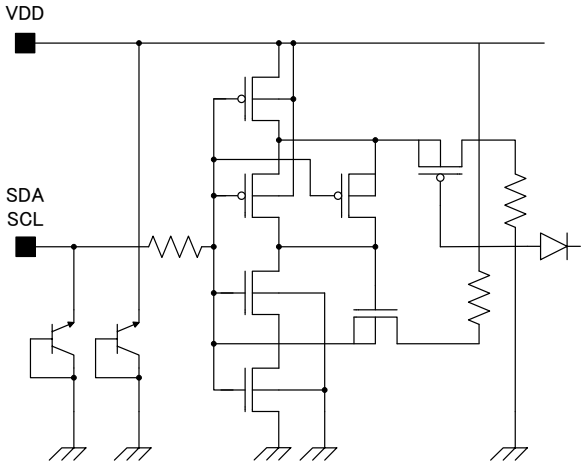
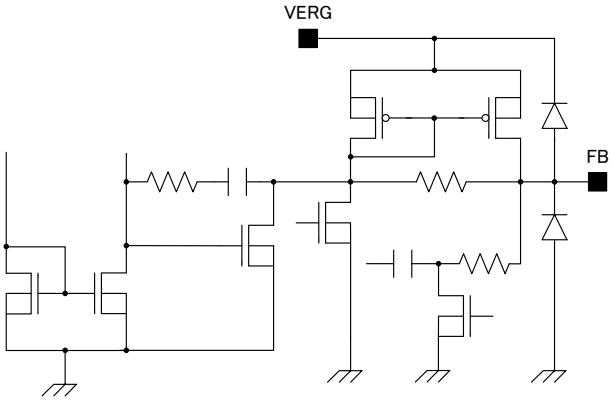
LED_FLIC[1:0] : LED Forced ON/OFF
TERR[2:0] : Timer count at unusual temperature
BERR_OVP [2:0] : Over voltage protection error
BERR_TOUT[2:0] : Timeout error of charge time
TERR_TOUT[2:0] : Timeout error of unusual temperature

Blink signals in a normal condition are prior to LED Forced ON/OFF.

○**I/O terminal equivalent circuit diagram 1**

VBUS,VIN	VREG
	
LX	**SYSTEM , VBAT**
	
TH	**CEN , USUS**
	

○I/O terminal equivalent circuit diagram 2

CRG , XPWR_ON, FLT, INT_B	CTI
	
DPI , DMI, DMO,DPO	**GCNT**
	
VDD , SCL , SDA	**FB**
	

○ Precautions for use

1.) Absolute maximum rating

Although this product was manufactured under strict quality control, it may degrade or break if the applied voltage or operating temperature range exceeds the absolute maximum rating. It was not manufactured in anticipation of breakage states, such as short circuit and open circuit modes, either. If a special mode in which any factor exceeds the absolute maximum rating is expected to occur, consider taking a proper physical measure, such as a fuse.

2.) Charge establishment

The BD7166GU is high-efficiency switch-mode charge management device for single-cell Li-ion battery. The charge parameters can be programmed through an I2C interface. Then this IC is necessary to design in consideration of rating, peripheral circuit and parts of connected accessories.

3.) Potential of the GND terminal

Set the potential of the GND terminal so that it will remain minimum in any operation state.

Take a proper measure not to allow all terminals to drop below the potential of the GND terminal in actual transition and other phenomena.

4.) Thermal design

Perform thermal design allowing sufficient margins for permissible losses (Pd) in actual use.

5.) Short circuit between terminals and improper mounting

Mount the IC in the correct direction and position on a printed circuit board. Improper mounting may result in the breakage of the IC.

There is another possibility that the IC will break in case of a short circuit attributable to a foreign substance between output terminals or between an output terminal and the power GND.

6.) Operation in a strong electromagnetic field

Note that the IC may malfunction if it is used in a strong electromagnetic field.

7.) Influences in a strong light

Note that the IC may malfunction if it is used in a large amount of light like a strobe. Please shade and check the operation sufficiently.

8.) Common impedance

Connect the power and GND wires with extreme care, such as lowering common impedance or minimizing the ripple (using as thick and short a wire as possible, lowering the ripple with an LC, etc.).

9.) Temperature protection circuit (TSD circuit)

This IC integrates a temperature protection circuit (TSD circuit). This circuit is intended exclusively to isolate the IC from thermal runaway, not to protect and guarantee the IC. Do not continuously operate after this circuit was operated, or operate it on the premise that this circuit becomes active.

10.) Rush current when the power is turned on

In the case of a CMOS IC or an IC with plural power supplies, a rush current may instantaneously flow when the power is/powers are turned on. Pay close attention to the power coupling capacity, the power supply/power supplies, and the width and layout of the GND pattern wires.

11.) IC terminal input

This IC is a monolithic IC and has P+ isolation and a P board between elements to separate them.

This P layer and the N layer of each element form a P-N junction, which makes up each parasitic element.

For example, when a register and a transistor are connected to terminals as shown in Figure . 15

- ○The P-N junction serves as a parasitic diode when GND > (terminal A) in the case of the register or when GND > (terminal B) in the case of the transistor (NPN).
- ○In the case of the transistor (NPN), a parasitic NPN transistor becomes activated by the N layer of another element close to the abovementioned parasitic diode when GND > (terminal B).

Because of the structure of the IC, parasitic elements will be inevitably formed by the potential relationship. If such parasitic elements work, it may result in circuit operation interference, malfunction, or, in the worst case, breakage. Use the IC with extreme care not to allow parasitic elements to work, such as applying a lower voltage than GND (P board) to the input terminal.

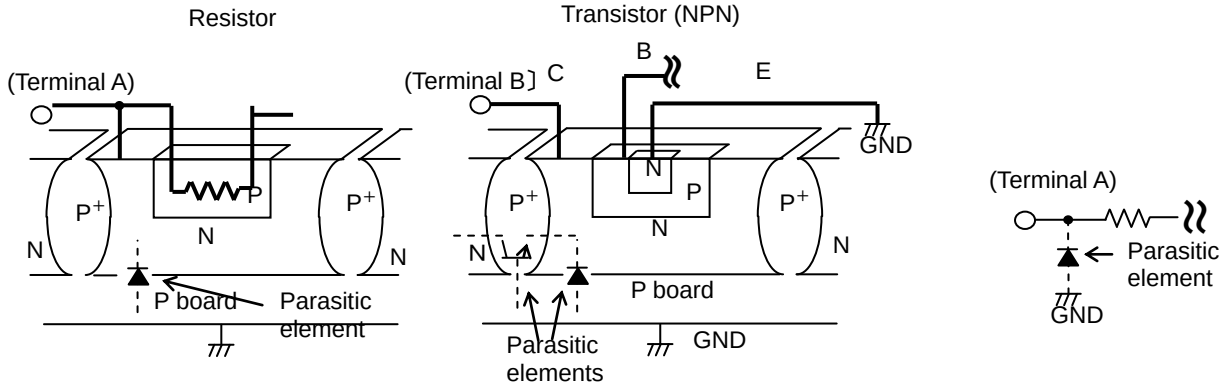


Fig. 15: Example of simple structure of bipolar IC

● Selection of model to order

B	D	7	1	6	8	G	U	-	E	2

Loam type

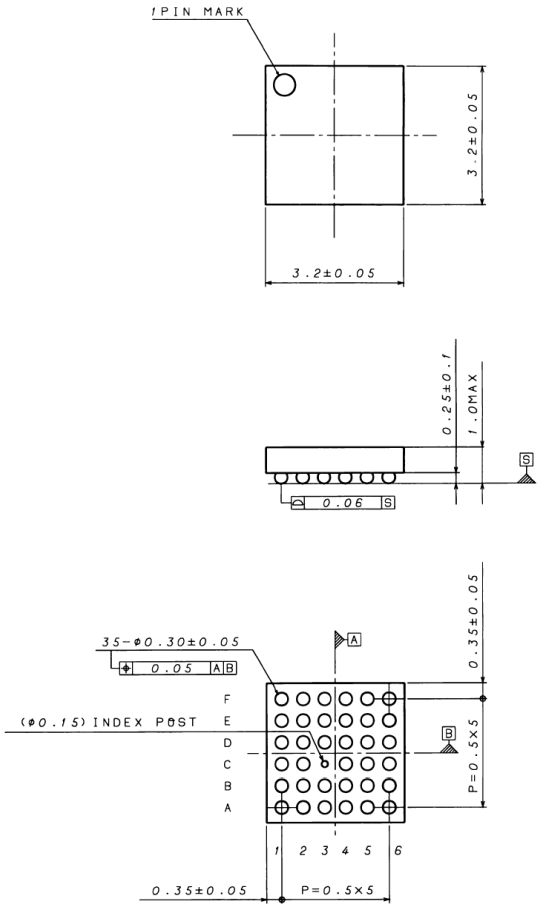
Product No.

Package
GU: VCSP85H3

Packing/Forming specification
E2: Reel-shaped emboss taping

Figure 16. Selection of model to order

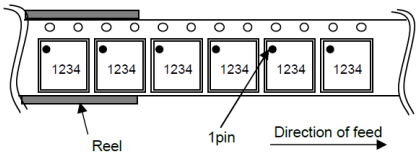
< External dimensions **>**



(UNIT:mm)

＜Tape and Reel information＞

Tape	Embossed carrier tape
Quantity	2,500pcs/Reel
Direction of feed	E2 (See Fig. 2)



<Marking diagram>

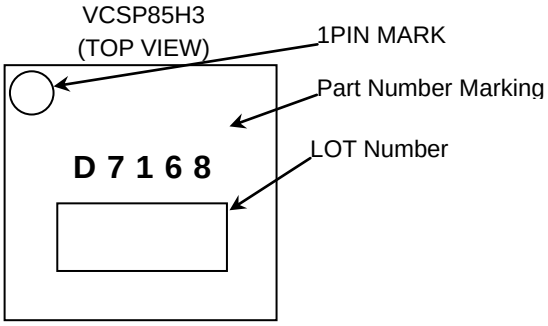


Figure 17. Outline drawing

Notice

●General Precaution

1) Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2) All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

●Precaution on using ROHM Products

1) Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

2) ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3) Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

●Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

●Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

●Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

●Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

●Precaution Regarding Intellectual Property Rights

1) All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

2) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the information contained in this document.

●Other Precaution

1) The information contained in this document is provided on an “as is” basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.

2) This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

3) The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

4) In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

5) The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.