128K × 8 HIGH SPEED CMOS STATIC RAM

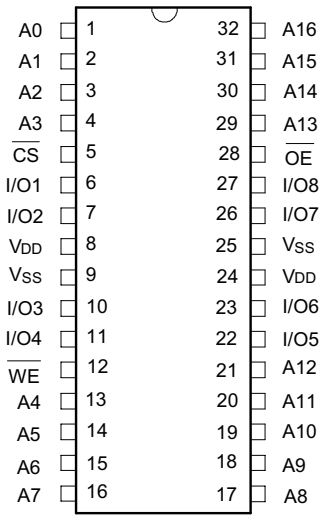
GENERAL DESCRIPTION

The W24L011A is a high speed, low power CMOS static RAM organized as 131072 × 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

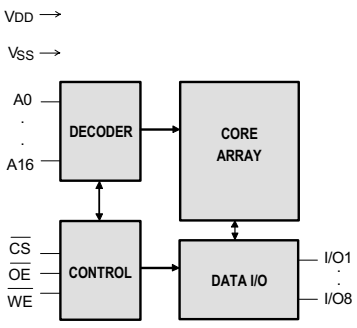
FEATURES

- High speed access time: 10/12/15 nS
- Single +3.3V power supply
- Center power/ground pin configuration
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil and 400 mil SOJ

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V_{DD} CURRENT
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +4.6	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	0.8	V
Input High Voltage	V_{IH}	-		+2.0	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS}$ = V_{IH} (min.) or $\overline{OE}$ = V_{IH} (min.) or $\overline{WE}$ = V_{IL} (max.)		-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL} (max.), I/O = 0 mA Cycle = mim., Duty = 100%	10	-	-	130	mA
			12	-	-	120	
			15	-	-	110	
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} (min.)		-	-	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{DD} -0.2V		-	-	10	mA

Note: Typical characteristics are at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

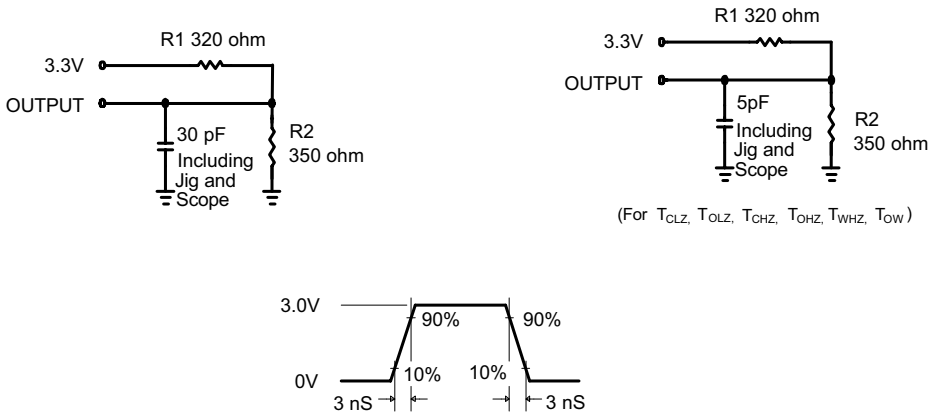
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24L011A-10		W24L011A-12		W24L011A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	10	-	12	-	15	-	nS
Address Access Time	T_{AA}	-	10	-	12	-	15	nS
Chip Select Access Time	T_{ACS}	-	10	-	12	-	15	nS
Output Enable to Output Valid	T_{AOE}	-	5	-	6	-	8	nS
Chip Selection to Output in Low Z	T_{CLZ}	3	-	3	-	-	3	nS
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	-		nS
Chip Deselection to Output in High Z	T_{CHZ}	-	5	-	6	-	8	nS
Output Disable to Output in High Z	T_{OHZ}*	-	5	-	6	-	8	nS
Output Hold from Address Change	T_{OH}	3	-	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

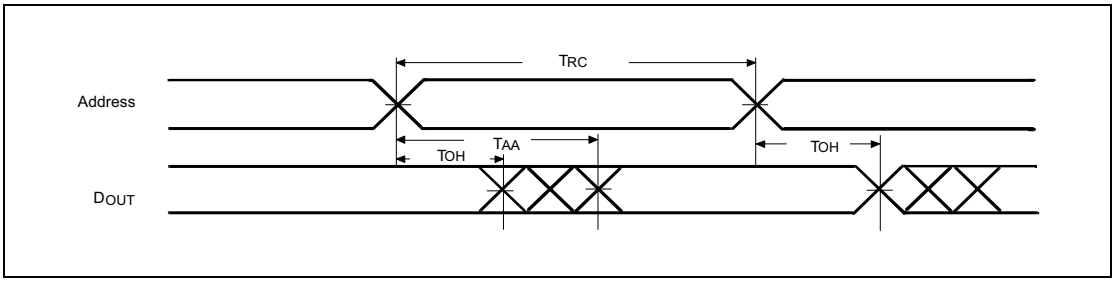
PARAMETER		SYM.	W24L011A-10		W24L011A-12		W24L011A-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	10	-	12	-	15	-	nS
Chip Selection to End of Write		T_{CW}	9	-	10	-	12	-	nS
Address Valid to End of Write		T_{AW}	9	-	10	-	12	-	nS
Address Setup Time		T_{AS}	0	-	0	-	0	-	nS
Write Pulse Width		T_{WP}	9	-	10	-	12	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	5	-	7	-	9	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	5	-	6	-	8	nS
Output Disable to Output in High Z		T_{OHZ}*	-	5	-	6	-	8	nS
Output Active from End of Write		T_{OW}	0	-	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

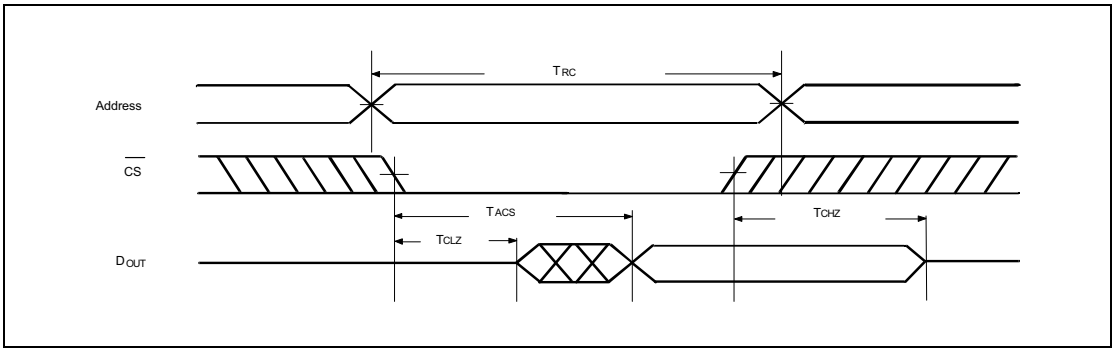
Read Cycle 1

(Address Controlled, $\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



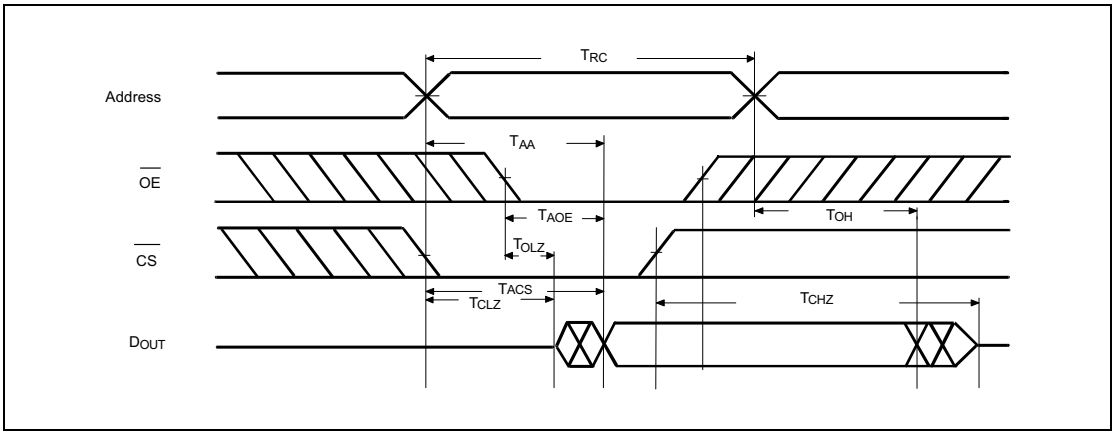
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

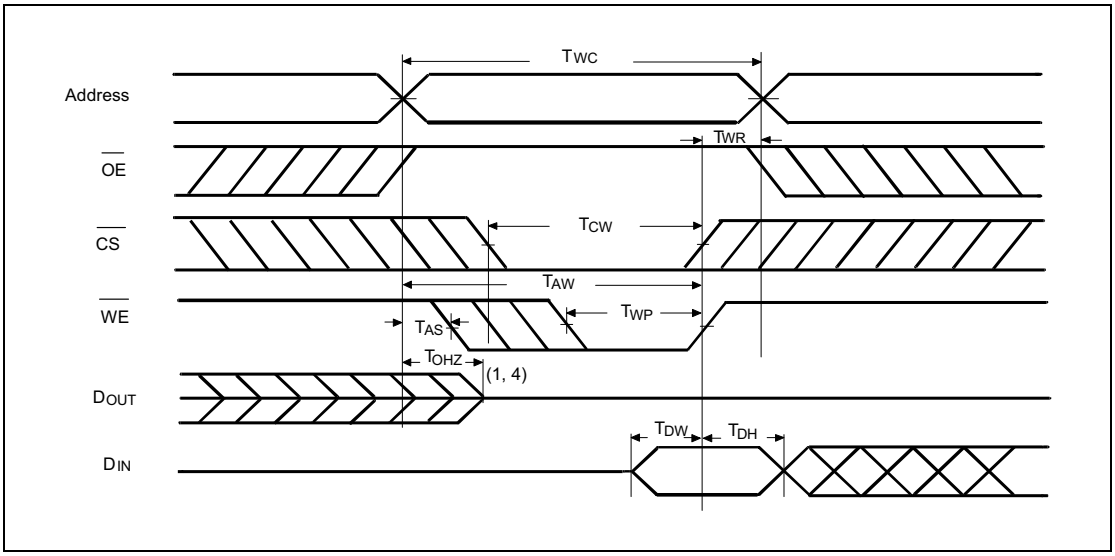
(Output Enable Controlled)



Timing Waveforms, continued

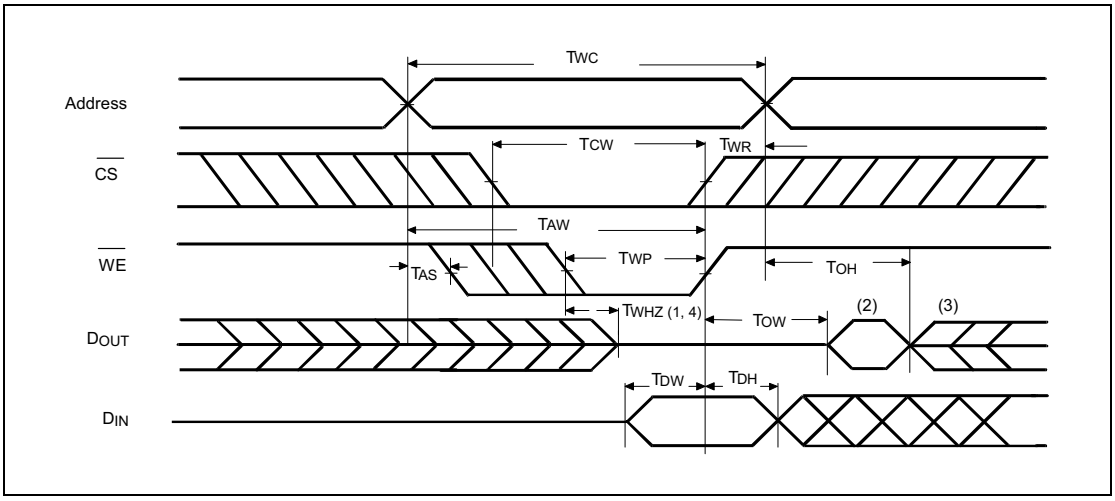
Write Cycle 1

($\overline{OE}$ Clock)



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:
1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. Dout provides the read data for the next address.
4. Transition is measured ±200 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

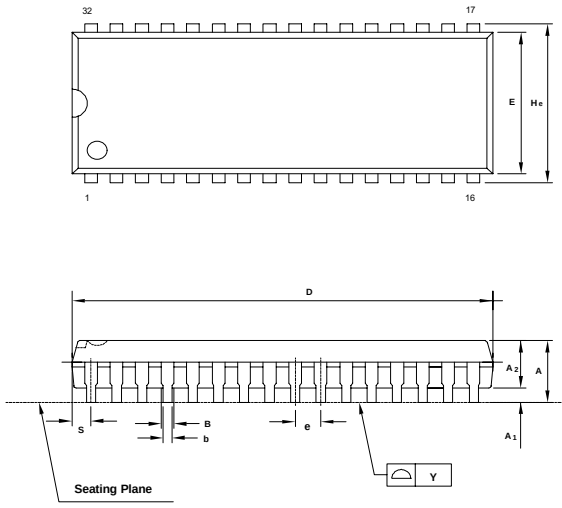
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24L011AJ-10	10	130	10	300 mil SOJ
W24L011AJ-12	12	120	10	300 mil SOJ
W24L011AJ-15	15	110	10	300 mil SOJ
W24L011AI-10	10	130	10	400 mil SOJ
W24L011AI-12	12	120	10	400 mil SOJ
W24L011AI-15	15	110	10	400 mil SOJ

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

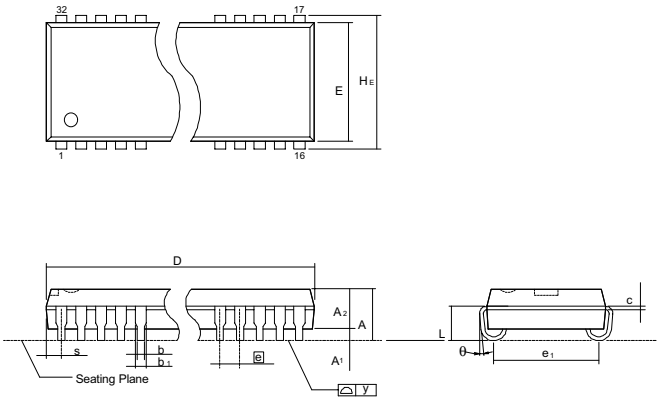
PACKAGE DIMENSIONS

32-pin SOJ (300 mil)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.556
A_1	0.020	—	—	0.508	—	—
A_2	0.095	0.100	0.105	2.413	2.540	2.667
B	0.026	0.028	0.032	0.660	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.815	0.825	0.835	20.701	20.955	21.209
E	0.295	0.300	0.305	7.493	7.620	7.747
e	0.044	0.050	0.056	1.118	1.270	1.422
e_1	0.247	0.267	0.287	6.274	6.782	7.290
H_e	0.325	0.335	0.345	8.255	8.509	8.763
L	0.080	—	—	2.032	—	—
S	—	—	0.045	—	—	1.143
Y	—	—	0.004	—	—	0.102
θ	0	—	10	0	—	10

32-pin SOJ (400 mil)



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.131	0.138	0.145	3.33	3.51	3.68
A_1	0.025	—	—	0.635	—	—
A_2	0.105	0.110	0.115	2.67	2.79	2.91
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.020	0.41	0.46	0.51
c	0.006	0.008	0.011	0.15	0.20	0.28
D	0.820	0.825	0.830	20.83	20.96	21.08
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.360	0.37	0.380	9.15	9.40	9.65
H_E	0.435	0.440	0.445	11.05	11.18	11.31
L	0.082	—	—	2.08	—	—
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
θ	-5°	2°	6°	-5°	2°	6°

Notes:
1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inches
5. General appearance spec. should be based on final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	August 1997		Initial Issued
A2	August 1999	1, 2, 4, 7	Add 15 nS specification

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