

MITSUBISHI LSIs

M5M44260CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is small enough for battery back-up application.

This device has $2\overline{CAS}$ and $1\overline{W}$ terminals with a refresh cycle of 512 cycles every 8.2ms.

FEATURES

| Type name | RAS access time (max.ns) | CAS access time (max.ns) | Address access time (max.ns) | OE access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|-------------------|--------------------------|--------------------------|------------------------------|-------------------------|---------------------|----------------------------|
| M5M44260CXX-5,-5S | 50 | 13 | 25 | 13 | 90 | 625 |
| M5M44260CXX-6,-6S | 60 | 15 | 30 | 15 | 110 | 550 |
| M5M44260CXX-7,-7S | 70 | 20 | 35 | 20 | 130 | 475 |

XX=J,TP

- Standard 40pin SOJ, 44 pin TSOP (II)
- Single $5V \pm 10\%$ supply
- Low stand-by power dissipation
 - CMOS Input level ----- 5.5mW (Max)
 - CMOS Input level ----- $550\mu W$ (Max) *
- Operating power dissipation
 - M5M44260Cxx-5,-5S ----- 688mW (Max)
 - M5M44260Cxx-6,-6S ----- 605mW (Max)
 - M5M44260Cxx-7,-7S ----- 523mW (Max)
- Self refresh capability *
 - Self refresh current ----- $150\mu A$ (Max)
- Extended refresh capability
 - Extended refresh current ----- $150\mu A$ (Max)
- Fast-page mode (512-column random access), Read-modify-write, RAS-only refresh, \overline{CAS} before RAS refresh, Hidden refresh capabilities.
- Early-write mode, \overline{LCAS} / \overline{UCAS} and \overline{OE} to control output buffer impedance
- 512 refresh cycles every 8.2ms (A_0 ~ A_8)
- 512 refresh cycles every 128ms (A_0 ~ A_8) *
- Byte or word control for Read/Write operation ($2\overline{CAS}$, $1\overline{W}$ type)
 - * : Applicable to self refresh version (M5M44260CJ,TP-5S,-6S,-7S : option) only

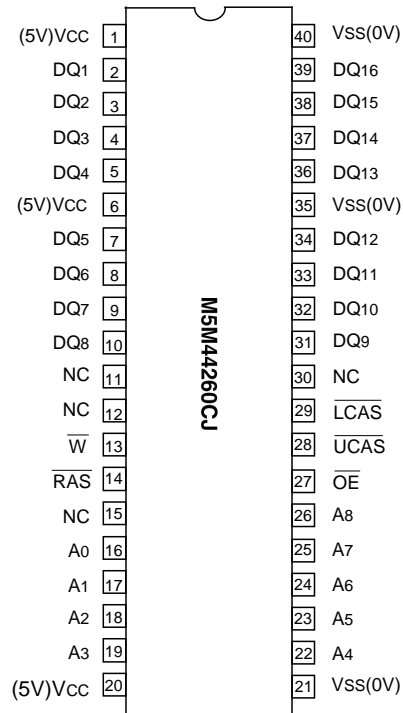
APPLICATION

Microcomputer memory, Refresh memory for CRT

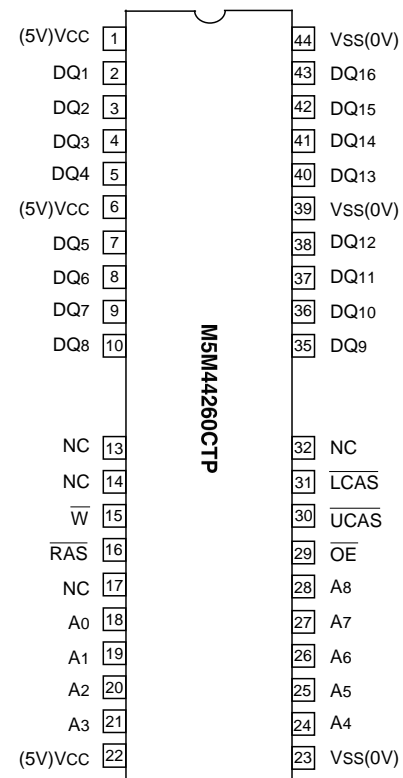
PIN DESCRIPTION

| Pin name | Function |
|-------------------|--|
| A_0 ~ A_8 | Address inputs |
| DQ1~DQ16 | Data inputs / outputs |
| \overline{RAS} | Row address strobe input |
| \overline{LCAS} | Lower byte control column address strobe input |
| \overline{UCAS} | Upper byte control column address strobe input |
| \overline{W} | Write control input |
| \overline{OE} | Output enable input |
| Vcc | Power supply (+5V) |
| Vss | Ground (0V) |

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (400mil SOJ)



Outline 44P3W-R (400mil TSOP Nomal Bend)

NC: NO CONNECTION

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FUNCTION

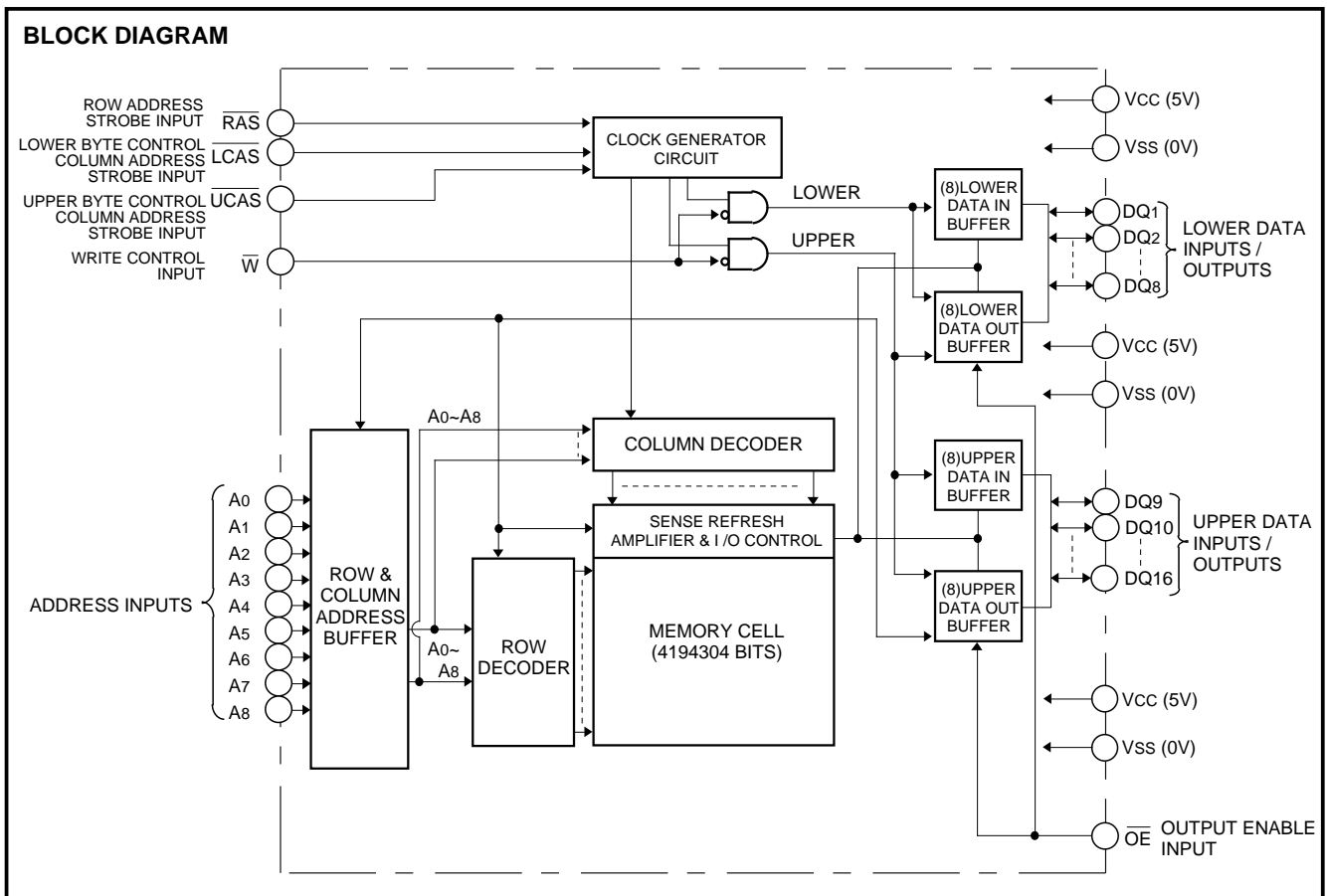
In addition to normal read, write and read-modify-write operations the M5M44260CJ, TP provides a number of other functions, e.g.,

fast page mode, $\overline{\text{RAS}}$ -only refresh and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

| Operation | Inputs | | | | | | | Input/Output | | Refresh | Remark |
|---|-------------------------|--------------------------|--------------------------|-----------------------|------------------------|-------------|----------------|--------------|----------|---------|--------------------------|
| | $\overline{\text{RAS}}$ | $\overline{\text{LCAS}}$ | $\overline{\text{UCAS}}$ | $\overline{\text{W}}$ | $\overline{\text{OE}}$ | Row address | Column address | DQ1~DQ8 | DQ9~DQ16 | | |
| Lower byte read | ACT | ACT | NAC | NAC | ACT | APD | APD | DOUT | OPN | YES | Fast page mode identical |
| Upper byte read | ACT | NAC | ACT | NAC | ACT | APD | APD | OPN | DOUT | YES | |
| Word read | ACT | ACT | ACT | NAC | ACT | APD | APD | DOUT | DOUT | YES | |
| Lower byte write | ACT | ACT | NAC | ACT | NAC | APD | APD | DIN | DNC | YES | |
| Upper byte write | ACT | NAC | ACT | ACT | NAC | APD | APD | DNC | DIN | YES | |
| Word write | ACT | ACT | ACT | ACT | NAC | APD | APD | DIN | DIN | YES | |
| $\overline{\text{RAS}}$ only refresh | ACT | NAC | NAC | DNC | DNC | APD | DNC | OPN | OPN | YES | |
| Hidden refresh | ACT | ACT | ACT | DNC | ACT | DNC | DNC | DOUT | DOUT | YES | |
| $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (Extended *) refresh | ACT | ACT | ACT | DNC | DNC | DNC | DNC | OPN | OPN | YES | |
| Self refresh * | ACT | ACT | ACT | DNC | DNC | DNC | DNC | OPN | OPN | YES | |
| Stand-by | NAC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | OPN | No | |

Note : ACT : active, NAC : nonactive, DNC : don't care, OPN : open



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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-----------------------|---------------------------------|---------|------|
| V _{CC} | Supply voltage | With respect to V _{SS} | -1~7 | V |
| V _I | Input voltage | | -1~7 | V |
| V _O | Output voltage | | -1~7 | V |
| I _O | Output current | | 50 | mA |
| P _d | Power dissipation | T _a =25°C | 1000 | mW |
| T _{opr} | Operating temperature | | 0~70 | °C |
| T _{stg} | Storage temperature | | -65~150 | °C |

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|-----------------|--------------------------------------|---------|-----|-----|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{SS} | Supply voltage | 0 | 0 | 0 | V |
| V _{IH} | High-level input voltage, all inputs | 2.4 | | 6.0 | V |
| V _{IL} | Low-level input voltage, all inputs | -0.5 ** | | 0.8 | V |

Note 1 : All voltage values are with respect to V_{SS}.

** : V_{IL}(min) is -2.0V when pulse width is less than 25ns. (Pulse width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------------|---|---|--------|-----|-----------------|------|
| | | | Min | Typ | Max | |
| V _{OH} | High-level output voltage | I _{OH} =-5mA | 2.4 | | V _{CC} | V |
| V _{OL} | Low-level output voltage | I _{OL} =4.2mA | 0 | | 0.4 | V |
| I _{OZ} | Off-state output current | Q floating 0V V _{OUT} 5.5V | -10 | | 10 | μA |
| I _I | Input current | 0V V _{IN} +6.0V, Other inputs pins=0V | -10 | | 10 | μA |
| I _{CC1(AV)} | Average supply current from V _{CC} , operating (Note 3,4,5) | M5M44260C-5,-5S M5M44260C-6,-6S M5M44260C-7,-7S RAS, CAS cycling trc=tWC=min. output open | | | 125 | mA |
| | | | | | 110 | |
| | | | | | 95 | |
| I _{CC2} | Supply current from V _{CC} , stand-by (Note 6) | RAS= CAS =V _{IH} , output open RAS= CAS V _{CC} -0.5V output open | | | 2 | mA |
| | | | | | 1.0 | |
| | | | | | 0.1 * | |
| I _{CC3(AV)} | Average supply current from V _{CC} , RAS only refresh mode (Note 3,5) | M5M44260C-5,-5S M5M44260C-6,-6S M5M44260C-7,-7S RAS cycling, CAS=V _{IH} trc=min. output open | | | 125 | mA |
| | | | | | 110 | |
| | | | | | 95 | |
| I _{CC4(AV)} | Average supply current from V _{CC} Fast page mode (Note 3,4,5) | M5M44260C-5,-5S M5M44260C-6,-6S M5M44260C-7,-7S RAS=V _{IL} , CAS cycling tpc=min. output open | | | 125 | mA |
| | | | | | 110 | |
| | | | | | 95 | |
| I _{CC6(AV)} | Average supply current from V _{CC} CAS before RAS refresh mode (Note 3,5) | M5M44260C-5,-5S M5M44260C-6,-6S M5M44260C-7,-7S CAS before RAS refresh cycling trc=min. output open | | | 115 | mA |
| | | | | | 100 | |
| | | | | | 85 | |
| I _{CC8(AV) *} | Average supply current from V _{CC} Extended-refresh mode (Note 6) | RAS cycling CAS 0.2V or CAS before RAS refresh cycling RAS 0.2V or V _{CC} -0.2V CAS 0.2V or V _{CC} -0.2V W 0.2V or V _{CC} -0.2V OE 0.2V or V _{CC} -0.2V A ₀ -A ₈ 0.2V or V _{CC} -0.2V, DQ=open trc=250μs, t _{RAS} =t _{TRAS} min~1μs | | | 150 | μA |
| I _{CC9(AV) *} | Average supply current from V _{CC} Self-refresh mode (Note 6) | RAS=CAS 0.2V output open | | | 150 | μA |

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV), and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and CAS=V_{IH}.

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CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------------------|--------------------------------------|---------------------------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| C _{I(A)} | Input capacitance, address inputs | V _I =V _{SS} | | | 5 | pF |
| C _{I(CLK)} | Input capacitance, clock inputs | f=1MHz | | | 7 | pF |
| C _{I/O} | Input/Output capacitance, data ports | V _I =25mVrms | | | 7 | pF |

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|---|-----------------|-----|-----------------|-----|-----------------|-----|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{CAC} | Access time from $\overline{\text{CAS}}$ (Note 7,8) | | 13 | | 15 | | 20 | ns |
| t _{RAC} | Access time from $\overline{\text{RAS}}$ (Note 7,9) | | 50 | | 60 | | 70 | ns |
| t _{AA} | Column address access time (Note 7,10) | | 25 | | 30 | | 35 | ns |
| t _{CPA} | Access time from $\overline{\text{CAS}}$ precharge (Note 7,11) | | 30 | | 35 | | 40 | ns |
| t _{OEa} | Access time from $\overline{\text{OE}}$ (Note 7) | | 13 | | 15 | | 20 | ns |
| t _{CLZ} | Output low impedance time from $\overline{\text{CAS}}$ low (Note 7) | 5 | | 5 | | 5 | | ns |
| t _{OFF} | Output disable time after $\overline{\text{CAS}}$ high (Note 12) | | 13 | | 15 | | 20 | ns |
| t _{OEZ} | Output disable time after $\overline{\text{OE}}$ high (Note 12) | | 13 | | 15 | | 20 | ns |

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than 8.2ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assumes that t_{RCD} = t_{RCD(max)} and t_{ASC} = t_{ASC(max)}.

9: Assumes that t_{RCD} = t_{RCD(max)} and t_{RAD} = t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that t_{RAD} = t_{RAD(max)} and t_{ASC} = t_{ASC(max)}.

11: Assumes that t_{CP} = t_{CP(max)} and t_{ASC} = t_{ASC(max)}.

12: t_{OFF(max)} and t_{OEZ(max)} defines the time at which the output achieves the high impedance state (I_{OUT} = ±10 μA) and is not reference to V_{OH(min)} or V_{OL(max)}.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh and Fast-Page Mode Cycles)

(Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|--|-----------------|-----|-----------------|-----|-----------------|-----|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tREF | Refresh cycle time | | 8.2 | | 8.2 | | 8.2 | ms |
| tREF | Refresh cycle time * | | 128 | | 128 | | 128 | ms |
| tRP | $\overline{\text{RAS}}$ high pulse width | 30 | | 40 | | 50 | | ns |
| tRCD | Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 15) | 18 | 37 | 20 | 45 | 20 | 50 | ns |
| tCRP | Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low | 5 | | 5 | | 5 | | ns |
| tRPC | Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low | 0 | | 0 | | 0 | | ns |
| tCPN | $\overline{\text{CAS}}$ high pulse width | 10 | | 10 | | 10 | | ns |
| tRAD | Column address delay time from $\overline{\text{RAS}}$ low (Note 16) | 13 | 25 | 15 | 30 | 15 | 35 | ns |
| tASR | Row address setup time before $\overline{\text{RAS}}$ low | 0 | | 0 | | 0 | | ns |
| tASC | Column address setup time before $\overline{\text{CAS}}$ low (Note 17) | 0 | 7 | 0 | 10 | 0 | 10 | ns |
| tRAH | Row address hold time after $\overline{\text{RAS}}$ low | 8 | | 10 | | 10 | | ns |
| tCAH | Column address hold time after $\overline{\text{CAS}}$ low | 13 | | 15 | | 15 | | ns |
| tDZC | Delay time, data to $\overline{\text{CAS}}$ low (Note 18) | 0 | | 0 | | 0 | | ns |
| tDZO | Delay time, data to $\overline{\text{OE}}$ low (Note 18) | 0 | | 0 | | 0 | | ns |
| tCDD | Delay time, $\overline{\text{CAS}}$ high to data (Note 19) | 13 | | 15 | | 20 | | ns |
| tODD | Delay time, $\overline{\text{OE}}$ high to data (Note 19) | 13 | | 15 | | 20 | | ns |
| tT | Transition time (Note 20) | 1 | 50 | 1 | 50 | 1 | 50 | ns |

Note 13: The timing requirements are assumed $t_T = 5\text{ns}$.

14: $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ are reference levels for measuring timing of input signals.

15: $t_{RCD(\text{max})}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(\text{max})}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(\text{max})}$, access time is controlled exclusively by t_{CAC} or t_{AA} .

16: $t_{RAD(\text{max})}$ is specified as a reference point only. If t_{RAD} $t_{RAD(\text{max})}$ and t_{ASC} $t_{ASC(\text{max})}$, access time is controlled exclusively by t_{AA} .

17: $t_{ASC(\text{max})}$ is specified as a reference point only. If t_{RCD} $t_{RCD(\text{max})}$ and t_{ASC} $t_{ASC(\text{max})}$, access time is controlled exclusively by t_{CAC} .

18: Either t_{DZC} or t_{DZO} must be satisfied.

19: Either t_{CDD} or t_{ODD} must be satisfied.

20: t_T is measured between $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$.

Read and Refresh Cycles

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|---|-----------------|-------|-----------------|-------|-----------------|-------|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tRC | Read cycle time | 90 | | 110 | | 130 | | ns |
| tRAS | $\overline{\text{RAS}}$ low pulse width | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | $\overline{\text{CAS}}$ low pulse width | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| tCSH | $\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low | 50 | | 60 | | 70 | | ns |
| tRSH | $\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low | 13 | | 15 | | 20 | | ns |
| tRCS | Read setup time before $\overline{\text{CAS}}$ low | 0 | | 0 | | 0 | | ns |
| tRCH | Read hold time after $\overline{\text{CAS}}$ high (Note 21) | 0 | | 0 | | 0 | | ns |
| tRRH | Read hold time after $\overline{\text{RAS}}$ high (Note 21) | 0 | | 0 | | 0 | | ns |
| tRAL | Column address to $\overline{\text{RAS}}$ hold time | 25 | | 30 | | 35 | | ns |
| tOCH | $\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low | 13 | | 15 | | 20 | | ns |
| tORH | $\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low | 13 | | 15 | | 20 | | ns |

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|---|-----------------|-------|-----------------|-------|-----------------|-------|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tWC | Write cycle time | 90 | | 110 | | 130 | | ns |
| tRAS | RAS low pulse width | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | CAS low pulse width | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| tCSH | CAS hold time after RAS low | 50 | | 60 | | 70 | | ns |
| tRSH | RAS hold time after CAS low | 13 | | 15 | | 20 | | ns |
| tWCS | Write setup time before CAS low (Note 23) | 0 | | 0 | | 0 | | ns |
| tWCH | Write hold time after CAS low | 8 | | 10 | | 15 | | ns |
| tCWL | CAS hold time after W low | 13 | | 15 | | 20 | | ns |
| tRWL | RAS hold time after W low | 13 | | 15 | | 20 | | ns |
| tWP | Write pulse width | 8 | | 10 | | 15 | | ns |
| tDS | Data setup time before CAS low or W low | 0 | | 0 | | 0 | | ns |
| tDH | Data hold time after CAS low or W low | 8 | | 10 | | 15 | | ns |
| tOEH | OE hold time after W low | 13 | | 15 | | 20 | | ns |

Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|---|-----------------|-------|-----------------|-------|-----------------|-------|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tRWC | Read write/read modify write cycle time (Note 22) | 126 | | 150 | | 180 | | ns |
| tRAS | RAS low pulse width | 86 | 10000 | 100 | 10000 | 120 | 10000 | ns |
| tCAS | CAS low pulse width | 49 | 10000 | 55 | 10000 | 70 | 10000 | ns |
| tCSH | CAS hold time after RAS low | 86 | | 100 | | 120 | | ns |
| tRSH | RAS hold time after CAS low | 49 | | 55 | | 70 | | ns |
| tRCS | Read setup time before CAS low | 0 | | 0 | | 0 | | ns |
| tCWD | Delay time, CAS low to W low (Note 23) | 31 | | 35 | | 45 | | ns |
| tRWD | Delay time, RAS low to W low (Note 23) | 68 | | 80 | | 95 | | ns |
| tAWD | Delay time, address to W low (Note 23) | 43 | | 50 | | 60 | | ns |
| tCWL | CAS hold time after W low | 13 | | 15 | | 20 | | ns |
| tRWL | RAS hold time after W low | 13 | | 15 | | 20 | | ns |
| tWP | Write pulse width | 8 | | 10 | | 15 | | ns |
| tDS | Data setup time before CAS low or W low | 0 | | 0 | | 0 | | ns |
| tDH | Data hold time after CAS low or W low | 8 | | 10 | | 15 | | ns |
| tOEH | OE hold time after W low | 13 | | 15 | | 20 | | ns |

Note 22: t_{RWC} is specified as $t_{RWC}(\min) = t_{RAC}(\max) + t_{ODD}(\min) + t_{RWL}(\min) + t_{RP}(\min) + 4t_t$.

23: t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} = t_{WCS}(\min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} = t_{CWD}(\min)$, $t_{RWD} = t_{RWD}(\min)$, $t_{AWD} = t_{AWD}(\min)$ and $t_{CPWD} = t_{CPWD}(\min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address.

If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

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Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|--|-----------------|--------|-----------------|--------|-----------------|--------|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tPC | Fast page mode read/write cycle time | 35 | | 40 | | 45 | | ns |
| tPRWC | Fast page mode read write/read modify write cycle time | 71 | | 80 | | 95 | | ns |
| tRAS | $\overline{\text{RAS}}$ low pulse width for read or write cycle (Note 25) | 85 | 100000 | 100 | 100000 | 115 | 100000 | ns |
| tCP | $\overline{\text{CAS}}$ high pulse width (Note 26) | 8 | 12 | 10 | 15 | 10 | 15 | ns |
| tCPRH | $\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ precharge | 30 | | 35 | | 40 | | ns |
| tCPWD | Delay time, $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ low (Note 23) | 48 | | 55 | | 65 | | ns |

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: tRAS(min) is specified as two cycles of $\overline{\text{CAS}}$ input are performed.

26: tCP(max) is specified as a reference point only.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|---|-----------------|-----|-----------------|-----|-----------------|-----|------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tCSR | $\overline{\text{CAS}}$ setup time before $\overline{\text{RAS}}$ low | 5 | | 5 | | 5 | | ns |
| tCHR | $\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low | 10 | | 10 | | 15 | | ns |
| tCAS | $\overline{\text{CAS}}$ low pulse width | 20 | | 20 | | 25 | | ns |

Note 27: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

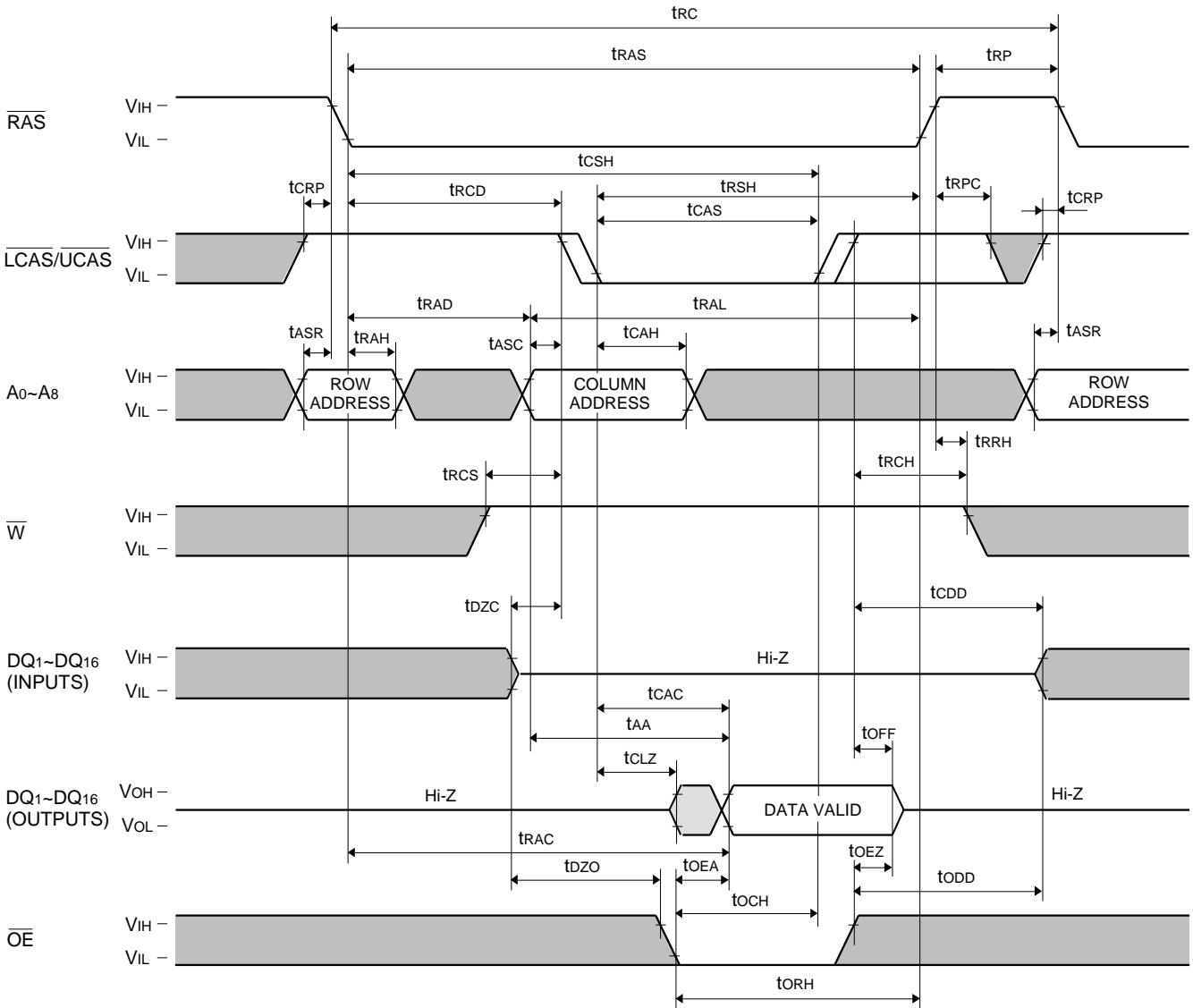
Self Refresh Cycle * (Note 28)

| Symbol | Parameter | Limits | | | | | | Unit |
|--------|--|-----------------|-----|-----------------|-----|-----------------|-----|---------------|
| | | M5M44260C-5,-5S | | M5M44260C-6,-6S | | M5M44260C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| tRASS | CBR self refresh $\overline{\text{RAS}}$ low pulse width | 100 | | 100 | | 100 | | μs |
| tRPS | CBR self refresh $\overline{\text{RAS}}$ high precharge time | 90 | | 110 | | 130 | | ns |
| tCHS | CBR self refresh $\overline{\text{CAS}}$ hold time | -50 | | -50 | | -50 | | ns |

M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 29) Read Cycle



Note 29



Indicates the don't care input.

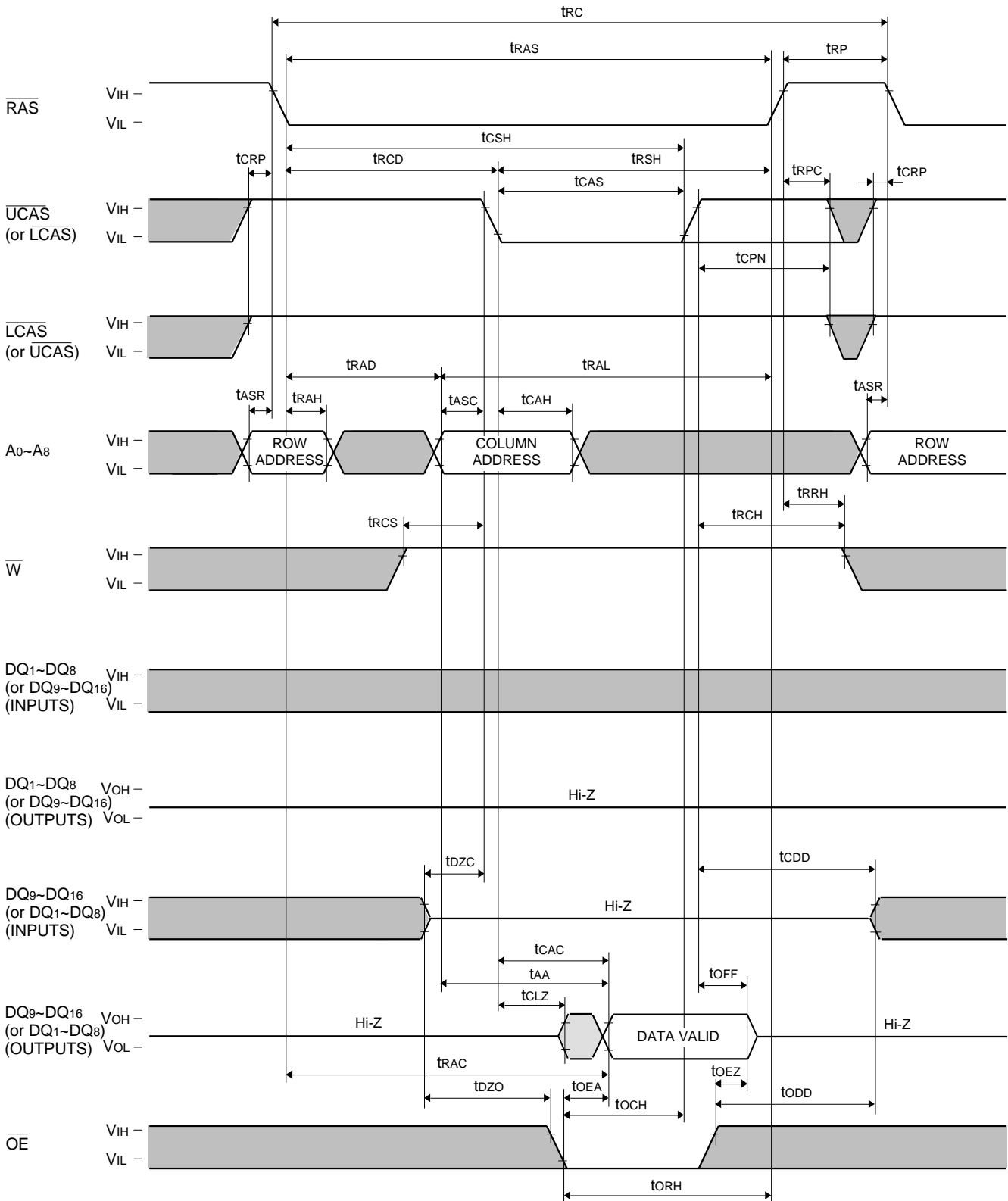
$V_{IH(min)}$ V_{IN} $V_{IH(max)}$ or $V_{IL(min)}$ V_{IN} $V_{IL(max)}$

Indicates the invalid output.

M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

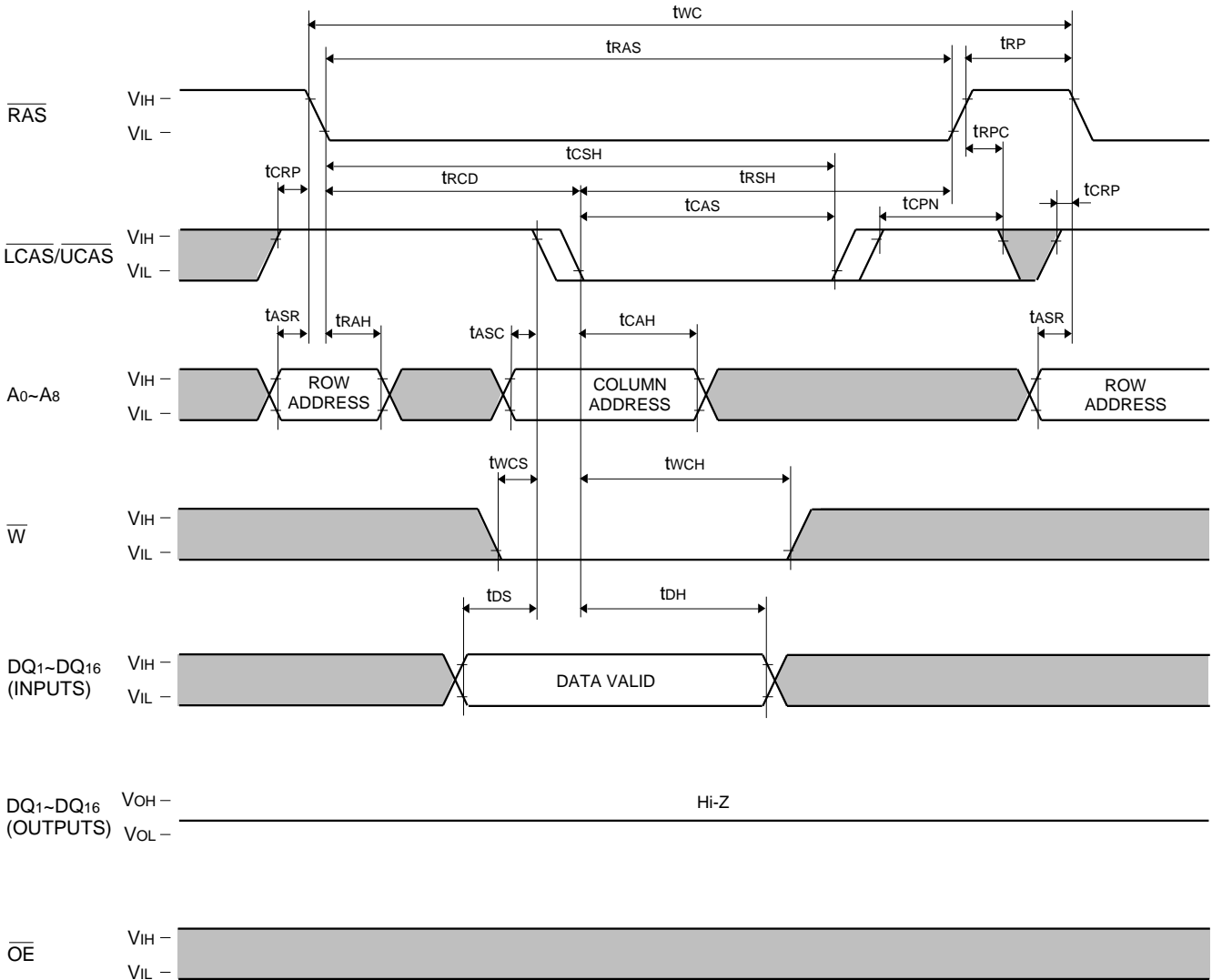
Byte Read Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

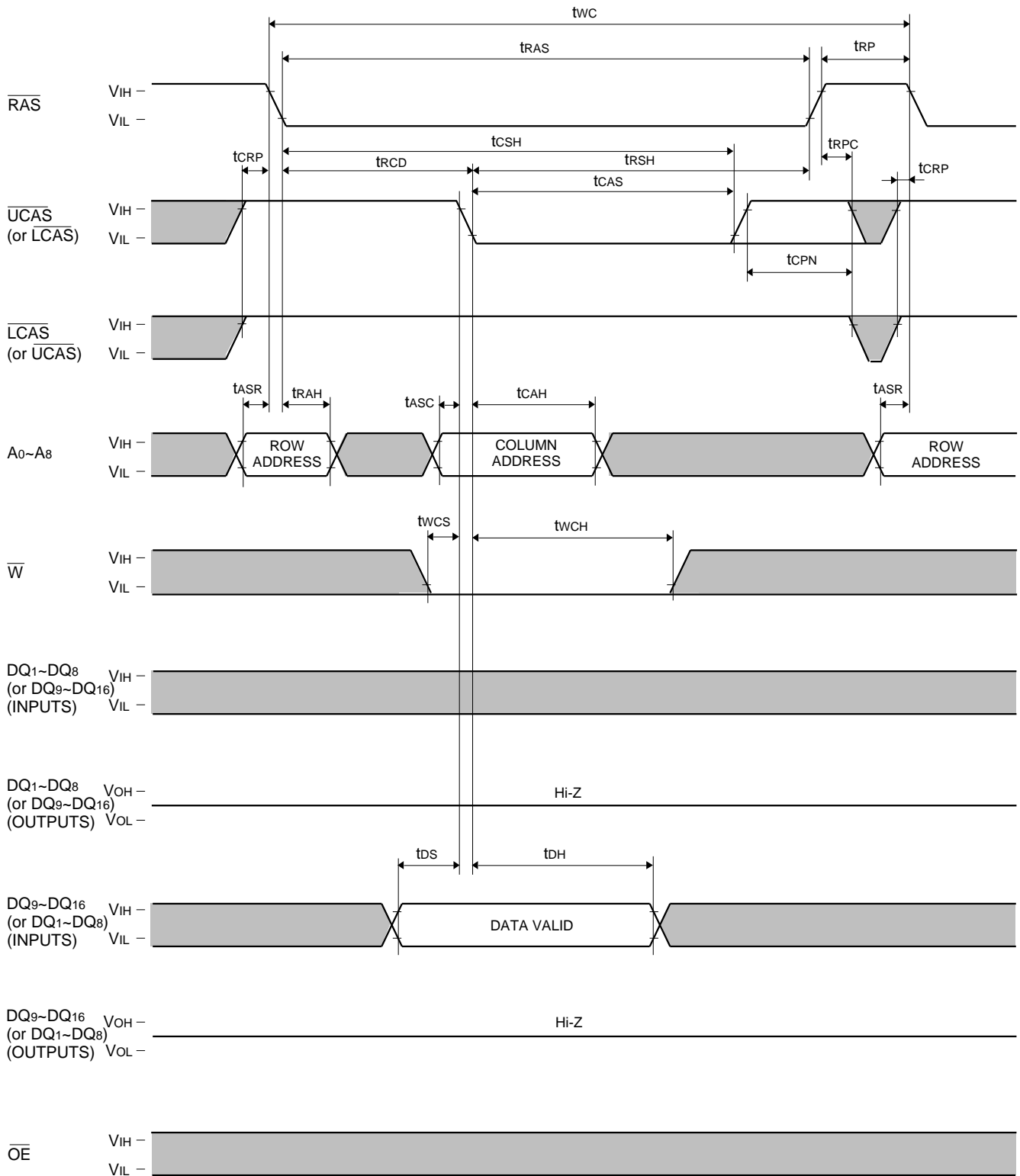
Write Cycle (Early write)



M5M44260CJ, TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

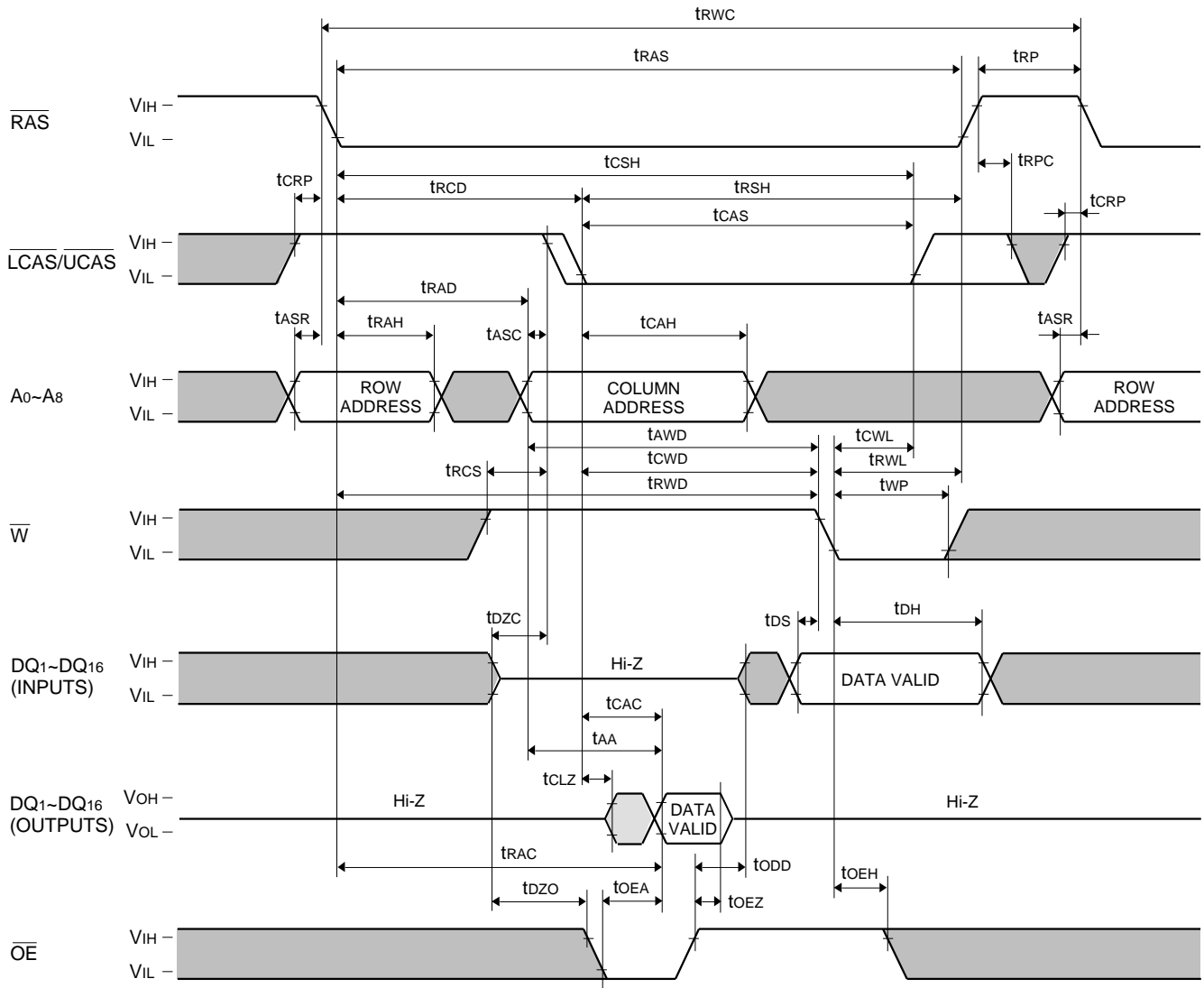
Byte Write Cycle (Early write)



M5M44260CJ, TP-5, -6, -7, -5S, -6S, -7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

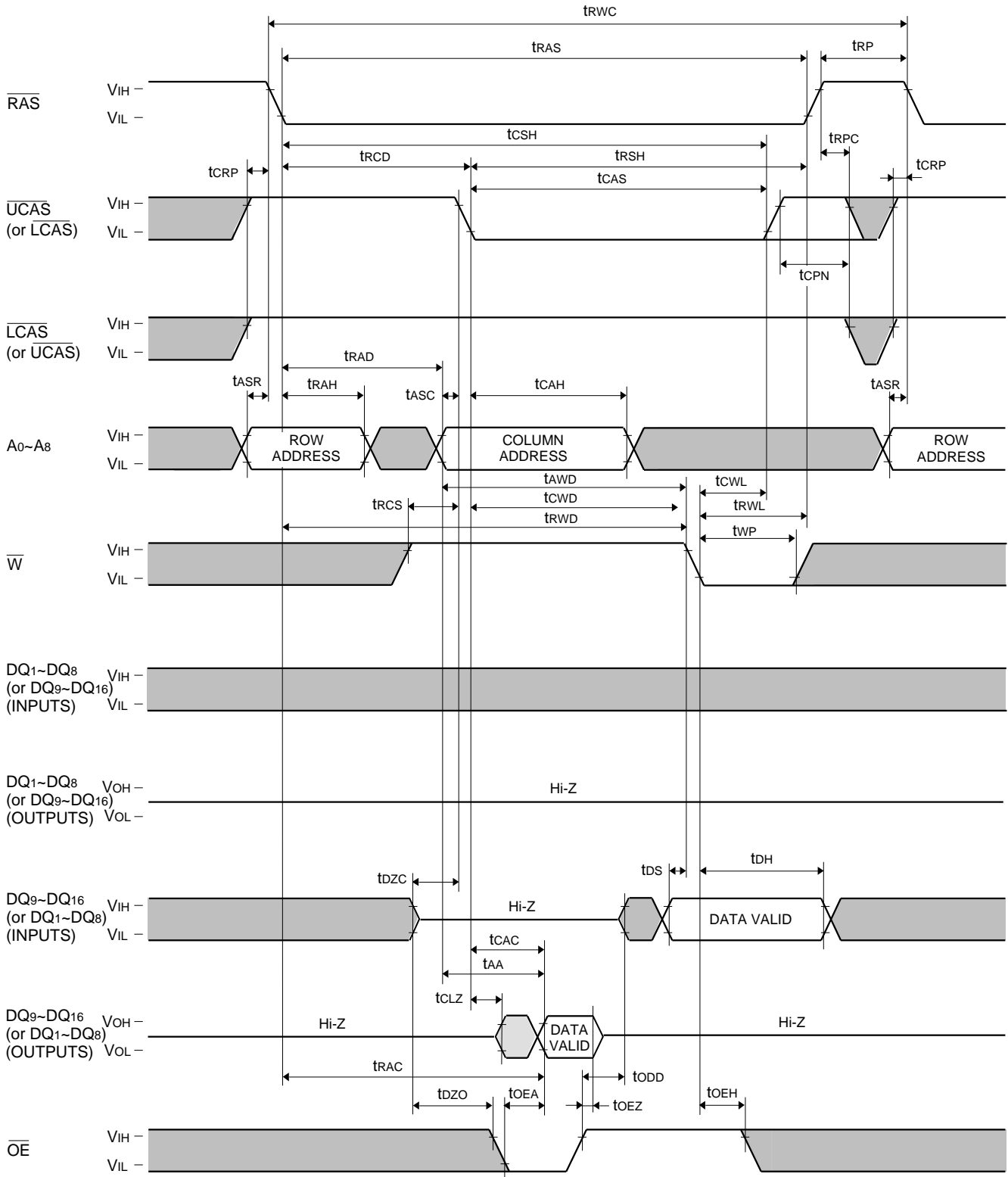
Read-Write, Read-Modify-Write Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

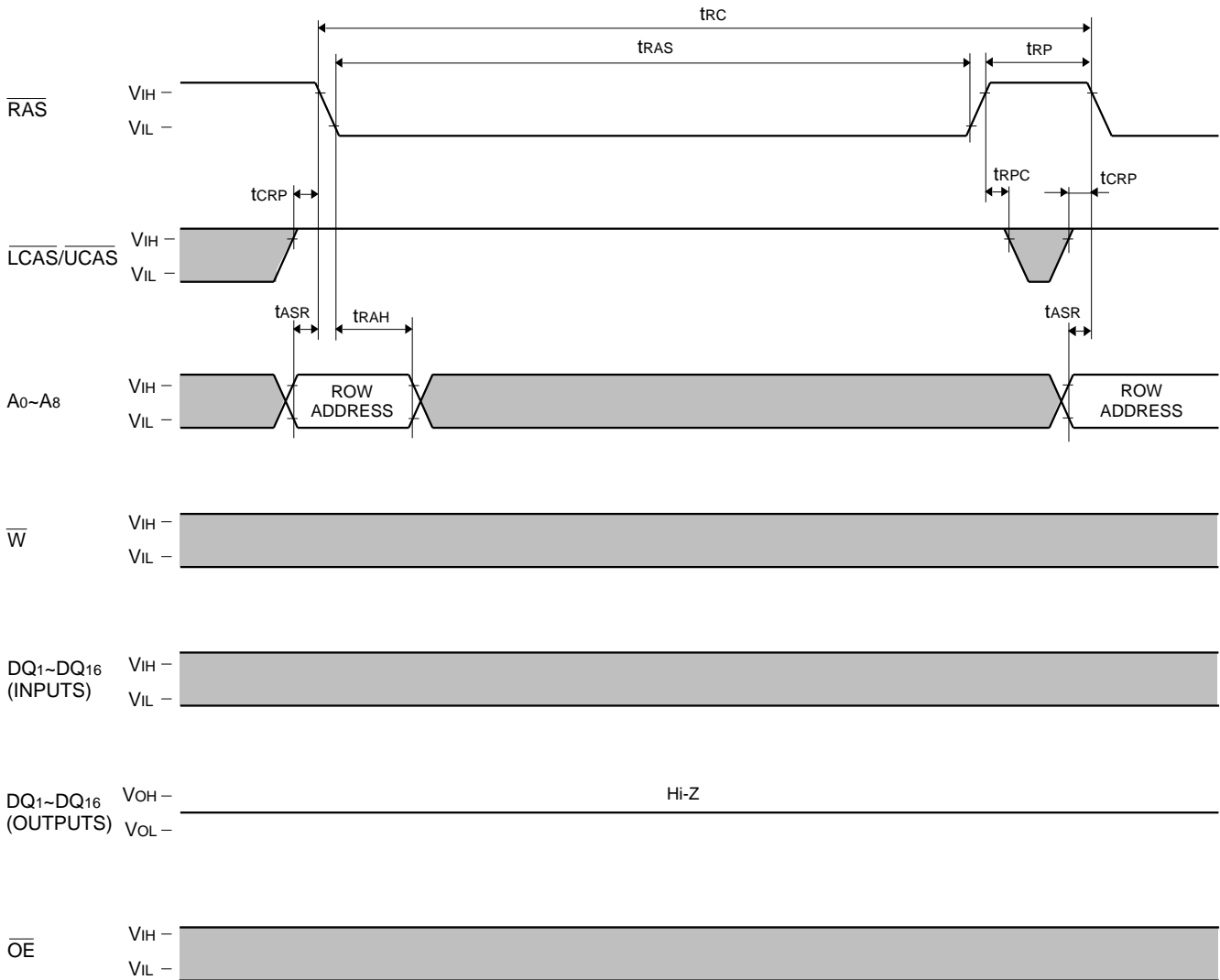
Byte Read-Write, Read-Modify-Write Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

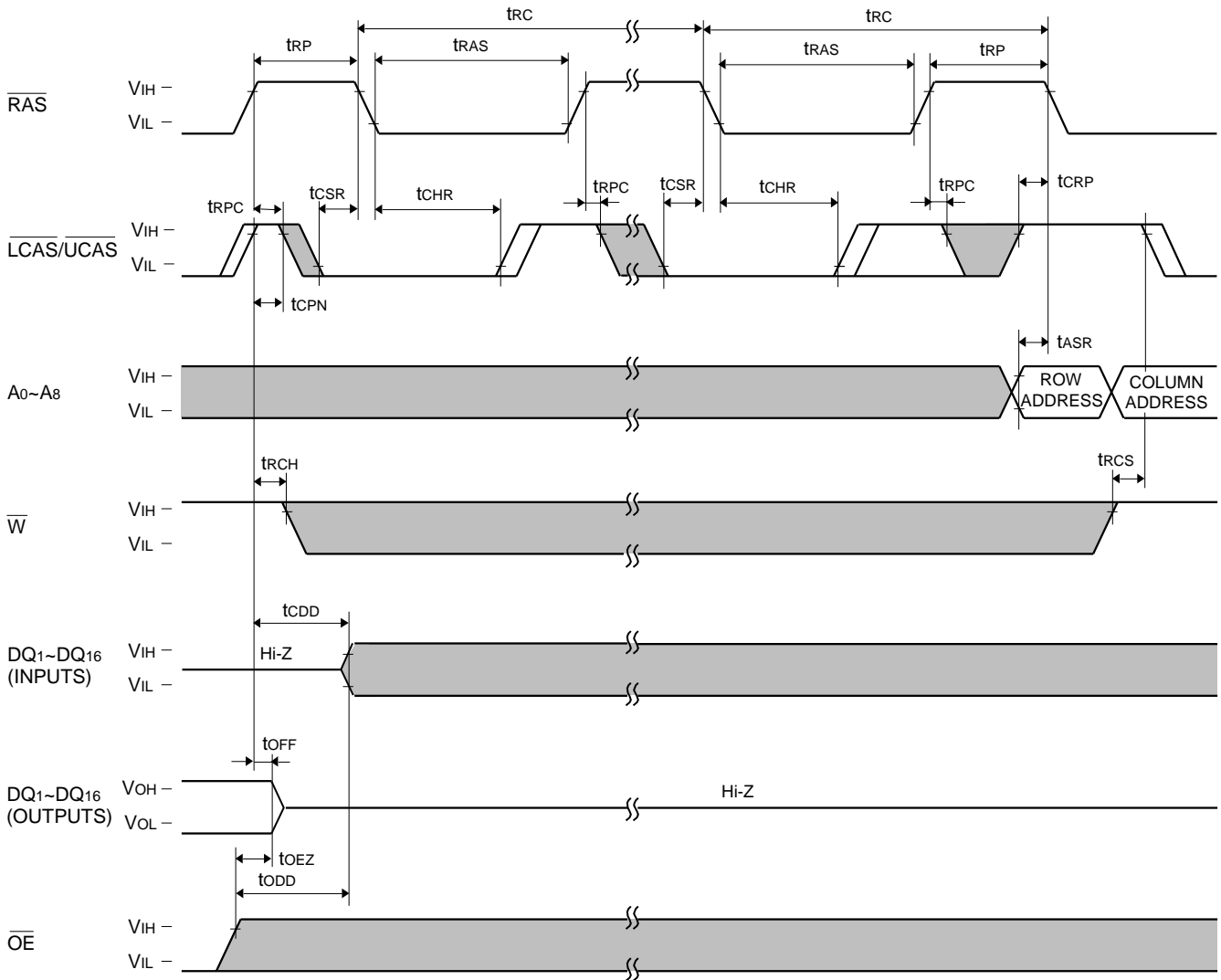
RAS-only Refresh Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

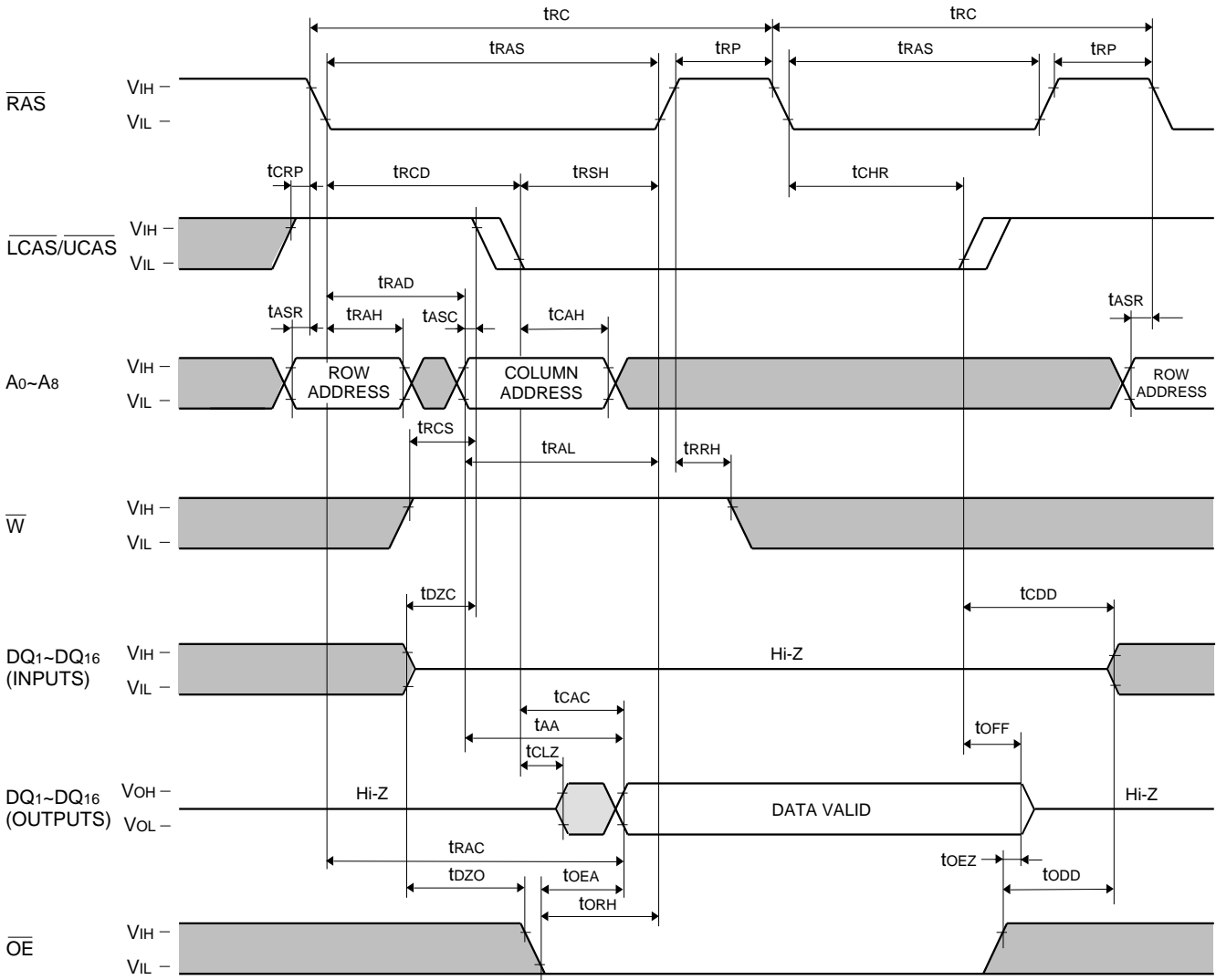
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Extended Refresh Cycle *



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 30)

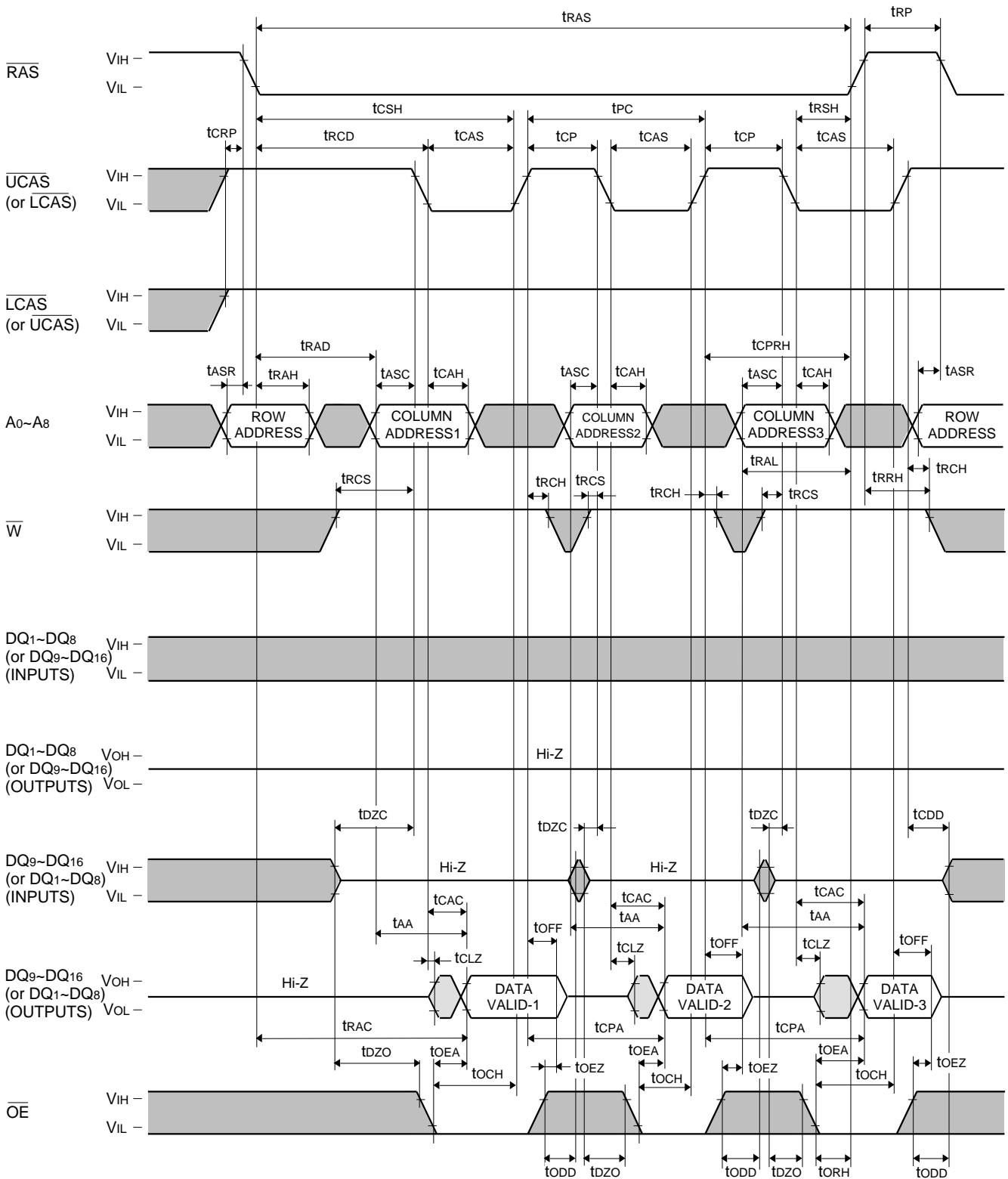


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle described above.

M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

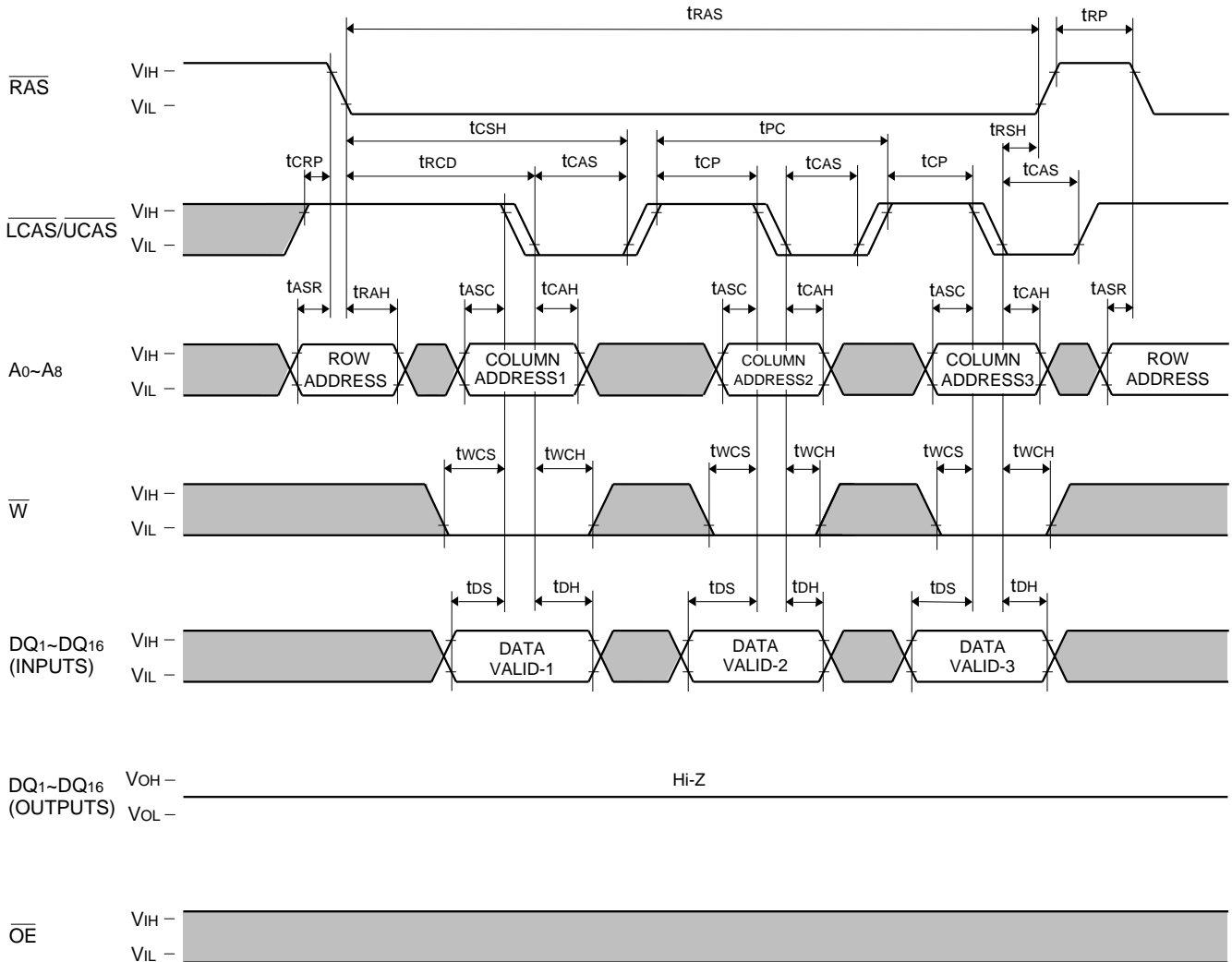
Fast Page Mode Byte Read Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

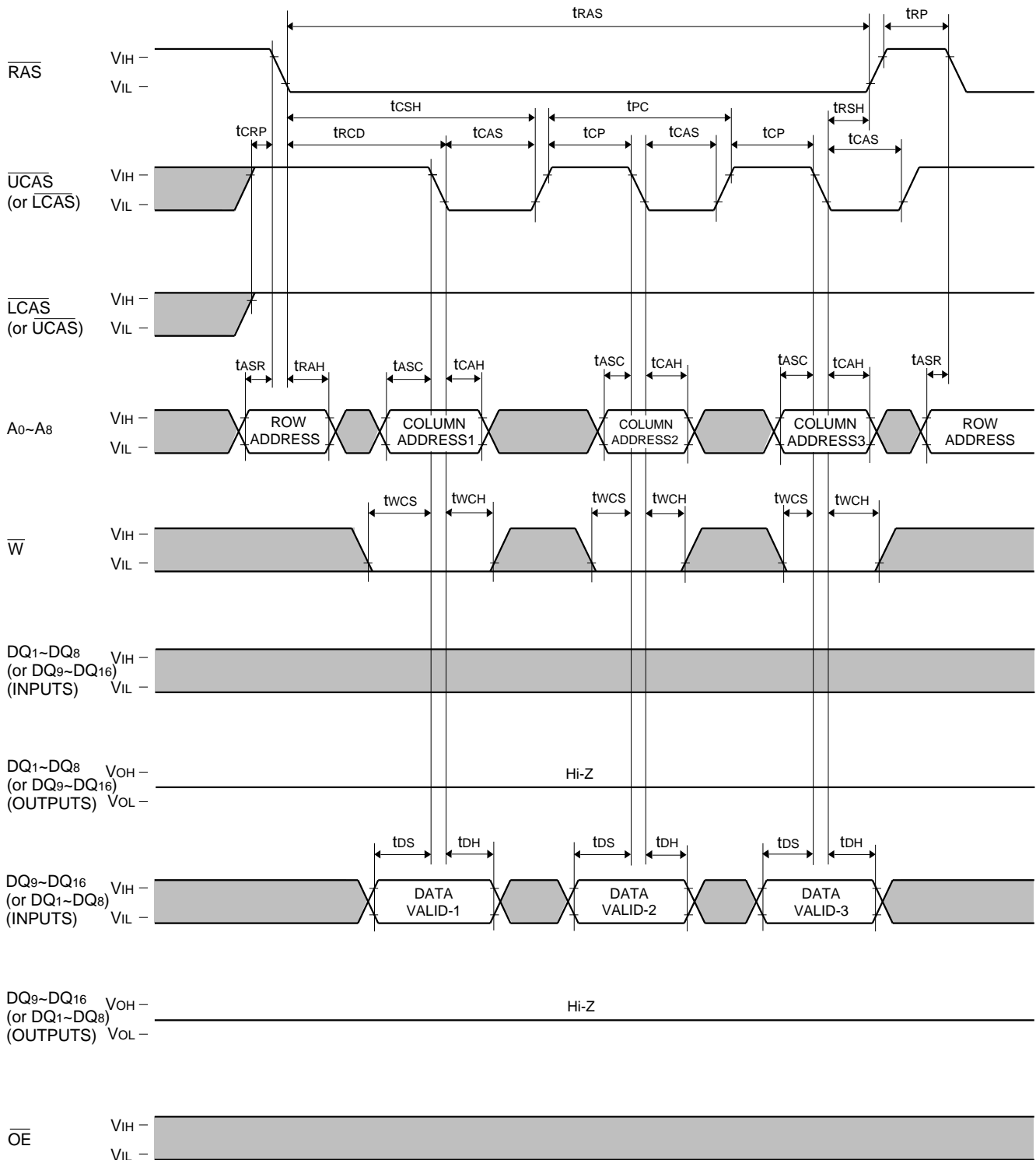
Fast Page Mode Write Cycle (Early Write)



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

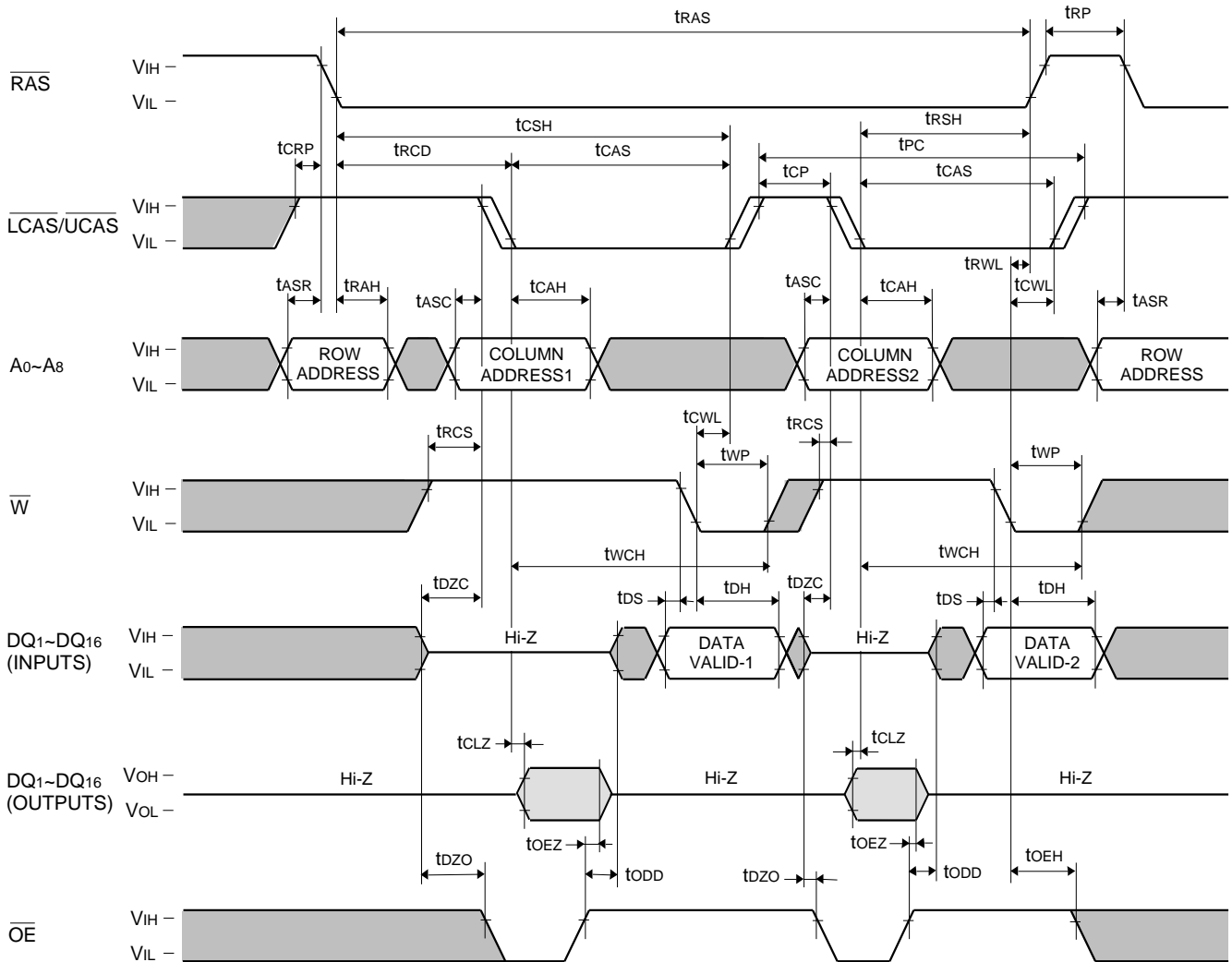
Fast Page Mode Byte Write Cycle (Early Write)



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

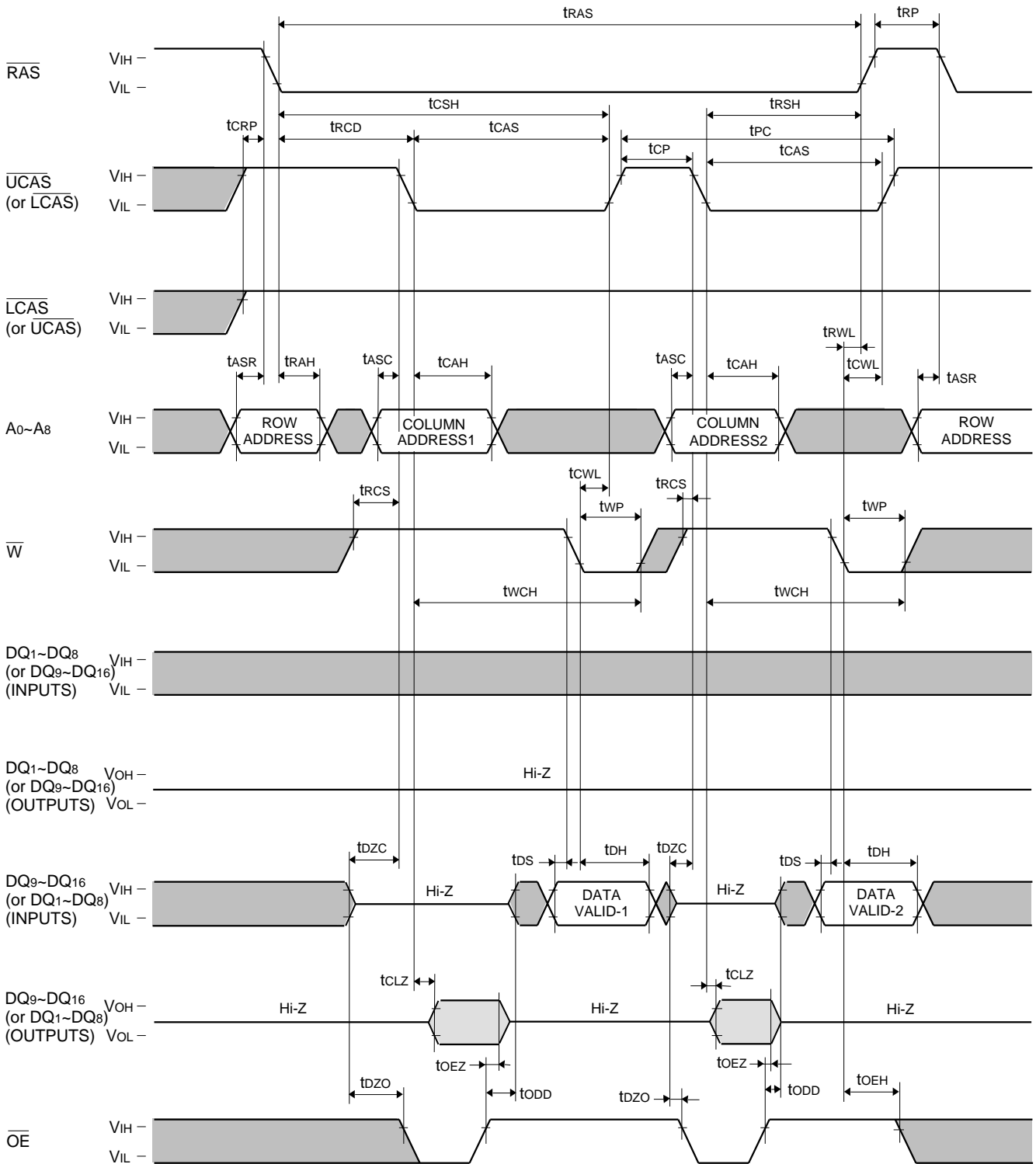
Fast-Page Mode Write Cycle (Delayed Write)



M5M44260CJ, TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

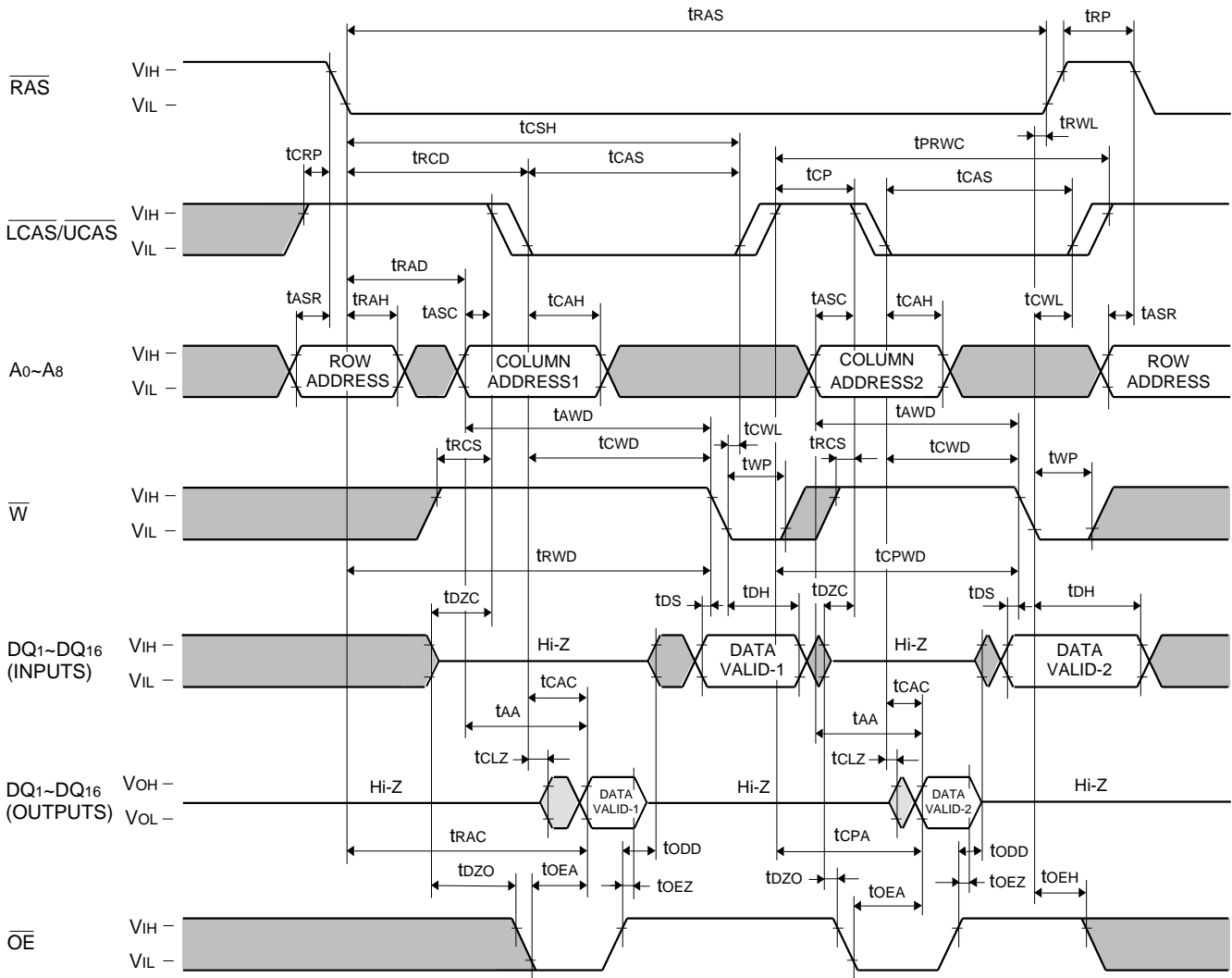
Fast-Page Mode Byte Write Cycle (Delayed Write)



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

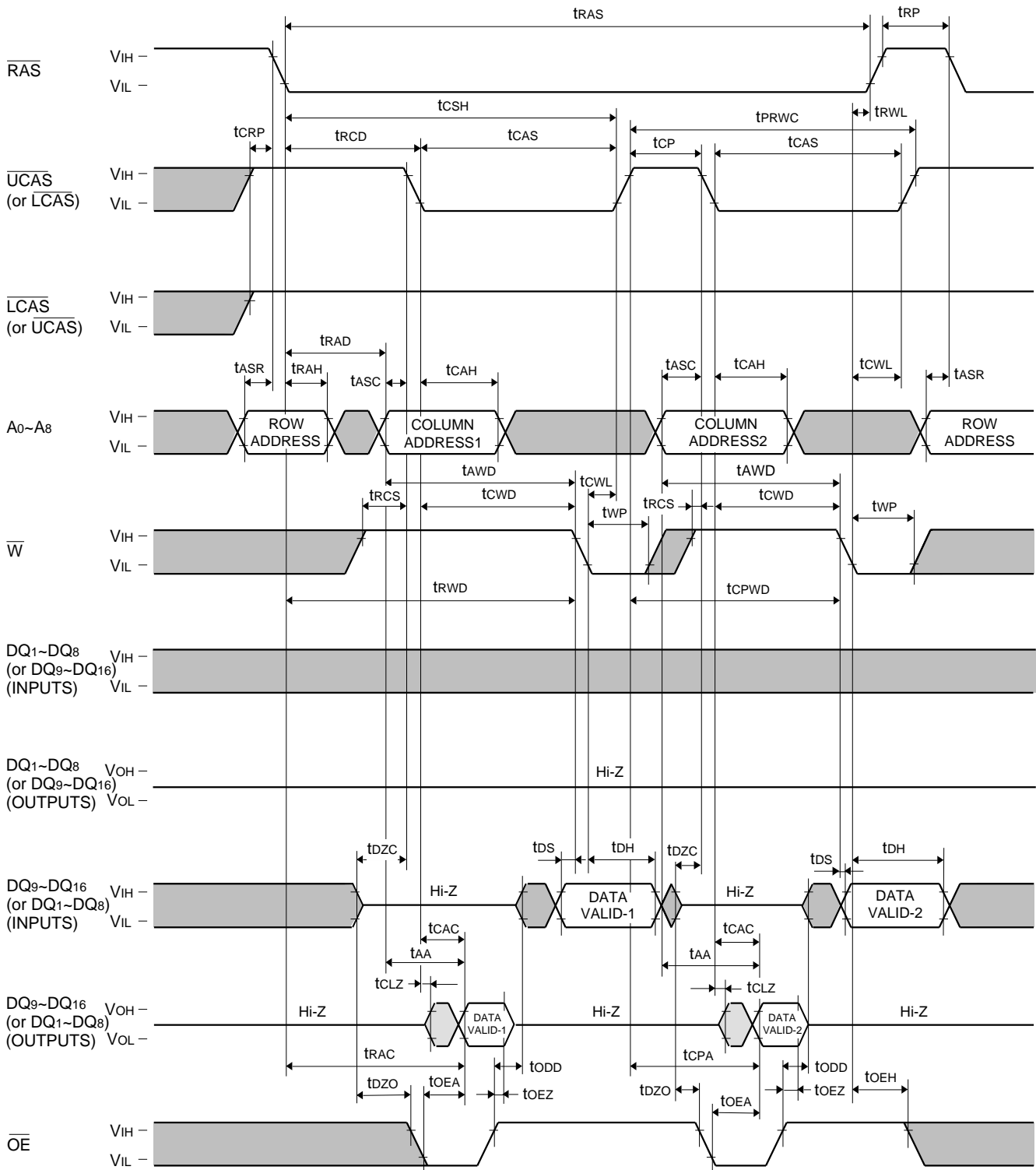
Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

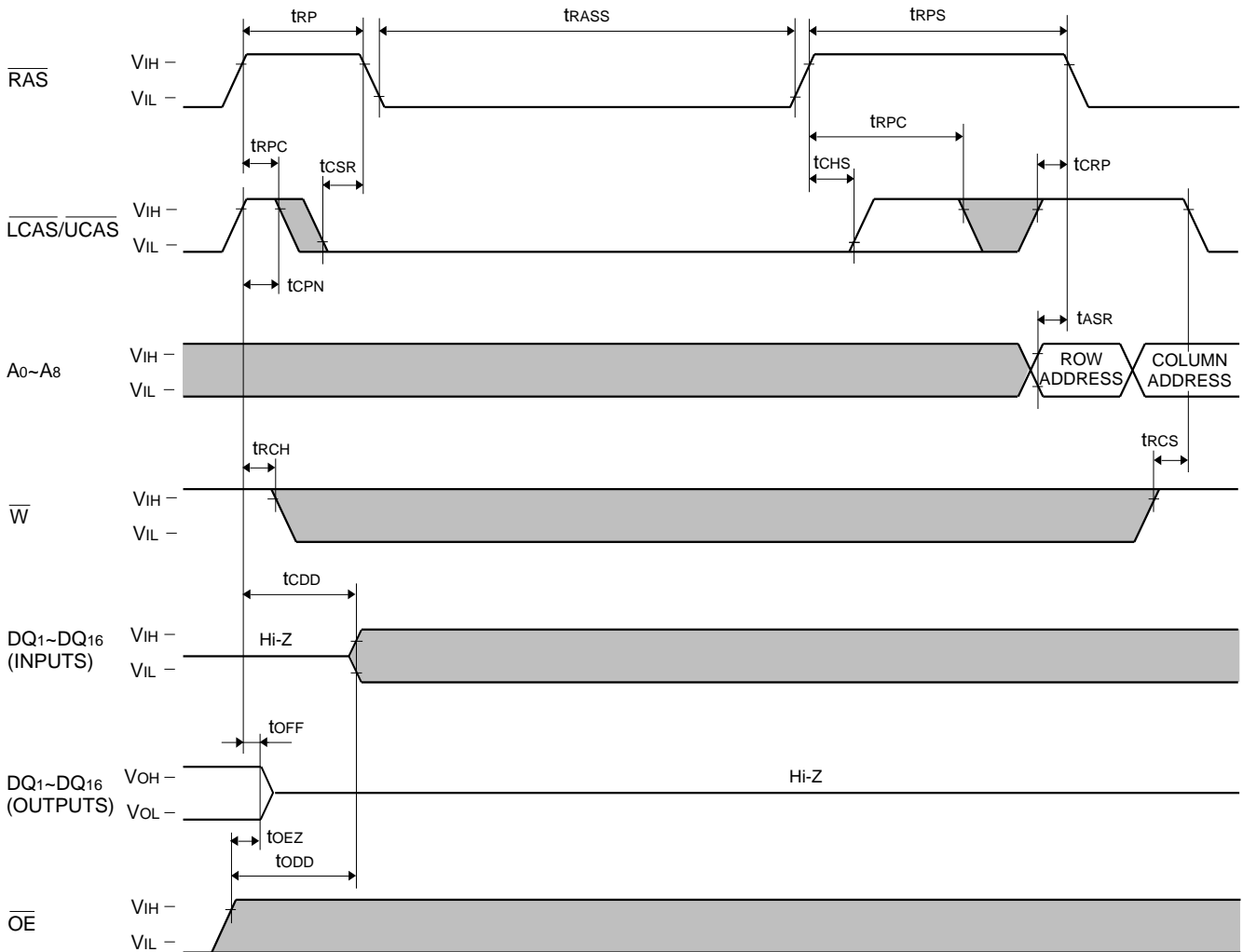
Fast Page Mode Byte Read-Write, Read-Modify-Write Cycle



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle * (Note28)



M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

Note 28 : Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width (t_{RASS}) of \overline{RAS} signal during self refresh period.

1. Distributed refresh during Read/Write operation

(A) Timing Diagram

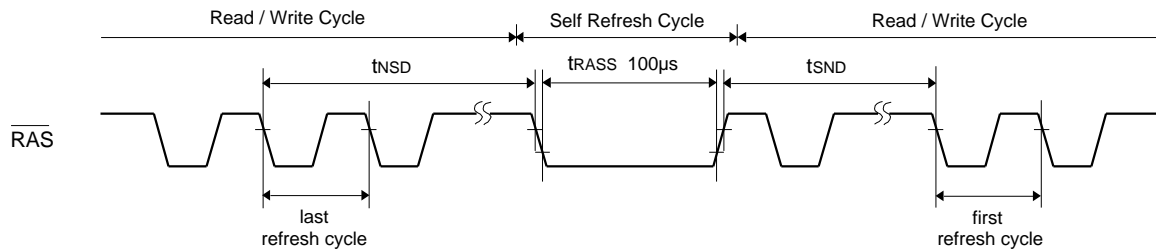
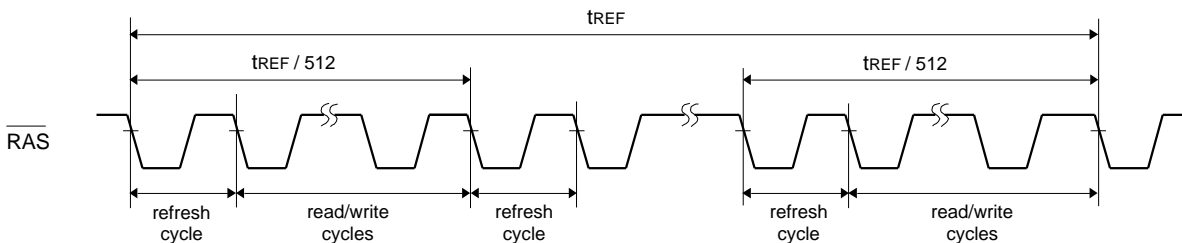


Table 2

| Read / Write Cycle | Read / Write → Self Refresh | Self Refresh → Read / Write |
|---|-----------------------------|-----------------------------|
| CBR distributed refresh | t_{NSD} 250µs | t_{SND} 250µs |
| \overline{RAS} only distributed refresh | t_{NSD} 16µs | t_{SND} 16µs |

(B) Definition of distributed refresh



Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 512 constant period (250µs max.) CBR cycles within 128 ms.

Definition of \overline{RAS} only distributed refresh

All combinations of nine row address signals (A_0 – A_8) are selected during 512 constant period (16µs max.) \overline{RAS} only refresh cycles within 8.2 ms.

Note:

Hidden refresh may be used instead of CBR refresh.

RAS/CAS refresh may be used instead of \overline{RAS} only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

- Switching from self refresh operation to read/write operation. The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.2 \overline{RAS} only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16µs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within 16µs.

M5M44260CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (262144-WORD BY 16-BIT) DYNAMIC RAM

2. Burst refresh during Read/Write operation

(A) Timing diagram

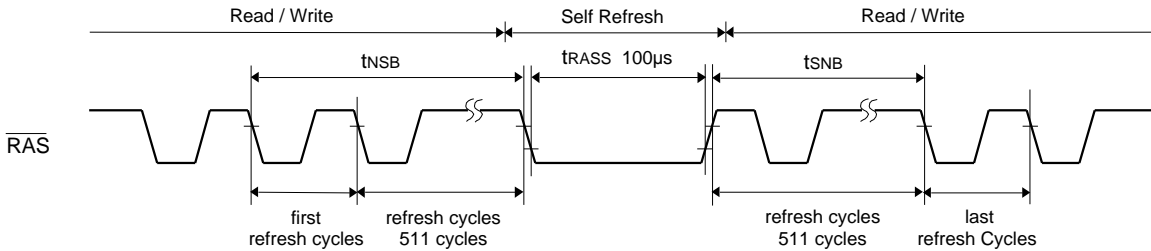
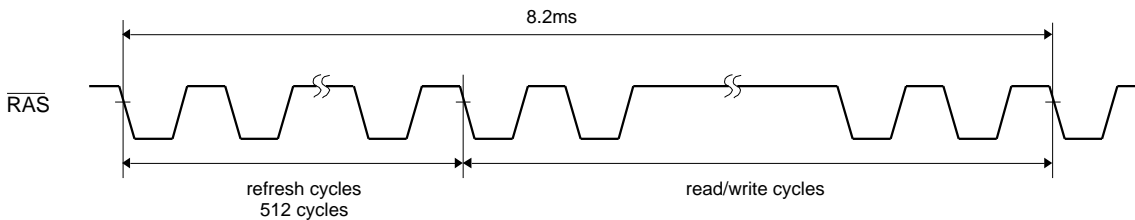


Table 3

| Read / Write Cycle | Read / Write → Self Refresh | Self Refresh → Read / Write |
|-------------------------------------|--------------------------------|--------------------------------|
| CBR burst refresh | t_{NSB} 8.2ms | t_{SNB} 8.2ms |
| \overline{RAS} only burst refresh | $t_{NSB}+t_{SNB}$ 8.2ms | |

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 512 continuous CBR cycles within 8.2 ms.

Definition of \overline{RAS} only burst refresh

All combination of nine row address signals (A_0-A_8) are selected during 512 continuous \overline{RAS} only refresh cycles within 8.2 ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 8.2 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period should be set within 8.2 ms.

2.2 \overline{RAS} only burst refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of \overline{RAS} signal in the first \overline{RAS} only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the last \overline{RAS} only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).