Ordering number : EN7811A

SANYO Semiconductors
DATA SHEET

LV8220FN — Bi-CMOS IC CD/MD System Motor Driver

Overview

The LV8220FN is a system motor driver IC that implements all the motor driver circuits needed for CD and MD products. Since the LV8220FN provides a three-phase PWM spindle driver, a three-phase sled driver, and focus and tracking drivers (as two PWM H-bridge driver channels), it can contribute to further miniaturization, thinner from factors, and lower power in end products. The adoption of the direct PWM sensorless drive method for the spindle driver and the sled driver makes it possible to implement high efficiency motor drive with few external parts.

Features

- Direct PWM drive (low side control)
- Three-phase full-wave sensorless motor driver (spindle and sled blocks)
- Soft switching drive (spindle block)
- Reverse torque braking
- MOS output transistors
- Standby mode power saving function
- FG output

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage 1	V_{CC} max		6.0	V
Power supply voltage 2	VG max		9.6	V
Output block power supply voltage	VS max		6.0	V
Output current	I_O max		0.8	A
Power dissipation 1	Pd max1	Independent IC	0.35	W
Power dissipation 2	Pd max2	Mounted on a specified board	1.1	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 50mm×50mm×0.8mm, glass epoxy

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage 1	V_{CC}		1.9 to 4.0	V
Power supply voltage 2	VG		5.0 to 9.0	V
Output block power supply voltage	VS	VS ≤ VG-3.5(V)	0 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.3V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Power supply current 1	$I_{CC}1$	S/S pin H, SEL1 pin H		1.3	2.0	mA
Power supply current 2	$I_{CC}2$	S/S pin H, SEL1 pin L		1.0	1.5	mA
Power supply current 3	$I_{CC}3$	S/S pin L (standby mode)			20	μA
Power supply current 4	I_G1	S/S pin H, SEL1 pin L		80	150	μA
Power supply current 5	I_G2	S/S pin L (standby mode)			20	μA
CLK Pin						
High level input voltage range	V_{CLKH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{CLKL}		0		0.5	V
VG2 Pin						
Output voltage	V_{REG}	VG1=6.3(V)	3.5		4.5	V
Actuator block (focus and tracking) **Actuator input pin**						
High level input voltage range	V_{AIH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{AIL}		0		0.5	V
Output block ON resistance						
SOURCE1	Ron(H1)	I_O=0.5A, VS=2.3V, VG=6.3V forward TR		0.4	0.6	Ω
SOURCE2	Ron(H2)	I_O=0.5A, VS=2.3V, VG=6.3V reverse TR		0.4	0.6	Ω
SINK	Ron(L)	I_O=0.5A, VS=2.3V, VG=6.3V		0.4	0.6	Ω
SOURCE+SINK	Ron(H+L)	I_O=0.5A, sum of upper and lower outputs		0.8	1.2	Ω
Output transmission delay time (H-bridge)	T_{RISE}	* Design target		0.1		μs
	T_{FALL}	* Design target		0.1		μs
Minimum input pulse width	tmin	Ch1, ch2 output pulse width is 2/3 tmin or more * Design target	200			ns
Sled block **Output block ON resistance**						
SOURCE1	Ron(H1)	I_O=0.5A, VS=2.3V, VG=6.3V forward TR		0.4	0.6	Ω
SOURCE2	Ron(H2)	I_O=0.5A, VS=2.3V, VG=6.3V reverse TR		0.4	0.6	Ω
SINK	Ron(L)	I_O=0.5A, VS=2.3V, VG=6.3V		0.4	0.6	Ω
SOURCE+SINK	Ron(H+L)	I_O=0.5A, sum of upper and lower outputs		0.8	1.2	Ω
Decoder Input Pin (S1 to S3)						
High level input voltage range	V_{SLIH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{SLIL}		0		0.5	V
Position detection comparator						
Input offset voltage	V_{SLOFS}		-5		+5	mV
Common-mode input voltage range	V_{SLCM}		0		V_{CC}	V
High level output voltage	V_{SLFGH}	I_O=-0.5mA	V_{CC}-0.5		V_{CC}	V
Low level output voltage	V_{SLFGL}	I_O=0.5mA			0.5	V
VCO Pin						
VCO high level voltage	V_{SLVCOH}		0.85	1.05	1.25	V
VCO low level voltage	V_{SLVCOL}		0.40	0.60	0.80	V

* Design target value and no measurement is performed.

Continued on next page.

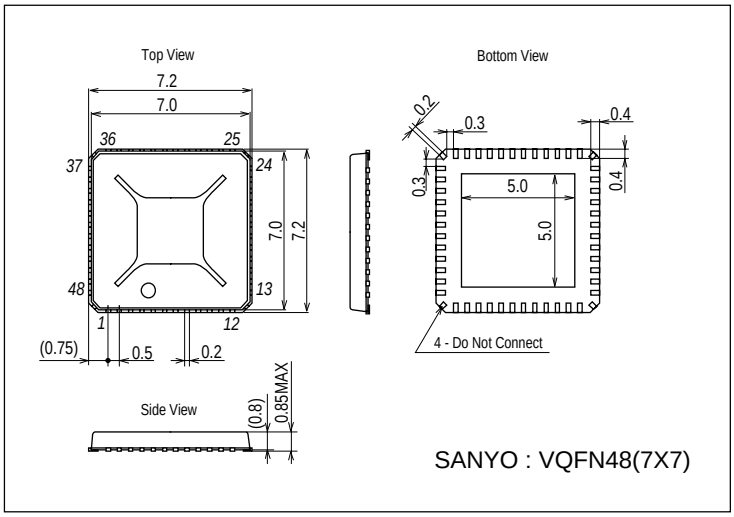
Continued from precceding page.

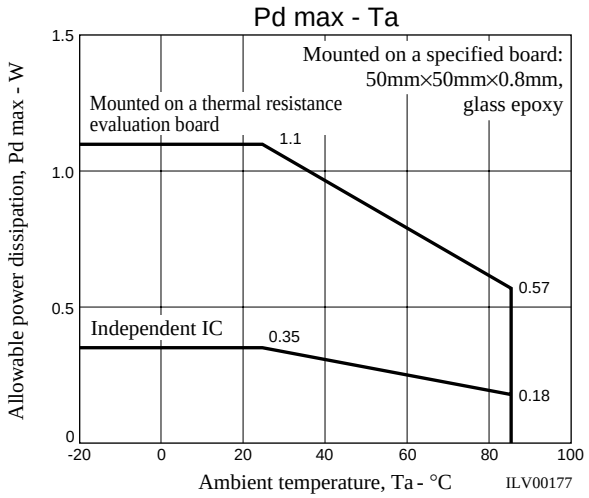
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
PWM Pin						
High level input voltage range	V_{SLPWMH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{SLPWML}		0		0.5	V
PWM input frequency	f_{SLIN}				190	kHz
SEL Pin						
High level input voltage range	V_{SLH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{SLL}		0		0.5	V
Spindle motor driver block						
Output block ON resistance						
SOURCE1	Ron(H1)	I_O=0.5A, VS=2.3V, VG=6.3V forward TR		0.4	0.6	Ω
SOURCE2	Ron(H2)	I_O=0.5A, VS=2.3V, VG=6.3V reverse TR		0.4	0.6	Ω
SINK	Ron(L)	I_O=0.5A, VS=2.3V, VG=6.3V		0.4	0.6	Ω
SOURCE+SINK	Ron(H+L)	I_O=0.5A, sum of upper and lower outputs		0.8	1.2	Ω
Position detection comparator						
Input offset voltage	V_{SOFS}		-5		+5	mV
VCO Pin						
VCO high level voltage	$VSPV_{COH}$		0.85	1.05	1.25	V
VCO low level voltage	$VSPV_{COL}$		0.40	0.60	0.80	V
S/S Pin						
High level input voltage range	V_{SSH}	Start	V_{CC}-0.5		V_{CC}	V
Low level input voltage range	V_{SSL}	Stop	0		0.5	V
BREAK Pin						
High level input voltage range	VSP_{BRH}	Brake OFF	V_{CC}-0.5		V_{CC}	V
Low level input voltage range	VSP_{BRL}	Brake ON	0		0.5	V
PWM Pin						
High level input voltage range	VSP_{PWMH}		V_{CC}-0.5		V_{CC}	V
Low level input voltage range	VSP_{PWML}		0		0.5	V
PWM input frequency	fSP_{IN}				190	kHz
FG Output Pin						
High level output voltage	VSP_{FGH}	I_O=-0.5mA	V_{CC}-0.5		V_{CC}	V
Low level output voltage	VSP_{FGL}	I_O=0.5mA			0.5	V

Package Dimensions

unit : mm (typ)

3272





Logic I/O Truth Tables

Focus and Tracking Blocks

S/S	IN1, 2F	IN1, 2R	OUT1, 2F	OUT1, 2R
H	L	L	L	L
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L
L	×	×	Z	Z

Sled Motor Stepping block

SEL	S/S	S1	S2	S3	SUO	SVO	SWO
L	H	L	L	L	H	L	Z
L	H	H	L	L	H	Z	L
L	H	L	H	L	Z	H	L
L	H	H	H	L	L	H	Z
L	H	L	L	H	L	Z	H
L	H	H	L	H	Z	L	H
L	H	L	H	H	Z	Z	Z
L	H	H	H	H	Z	Z	Z
H	H	×	×	×	Commutation output determined by sensorless logic		
×	L	×	×	×	Z	Z	Z

Z: open

BRK Pin

S2	OUT
H	Acceleration
L	Deceleration

SPBR	OUT
H	Acceleration
L	Deceleration

PWM Pin

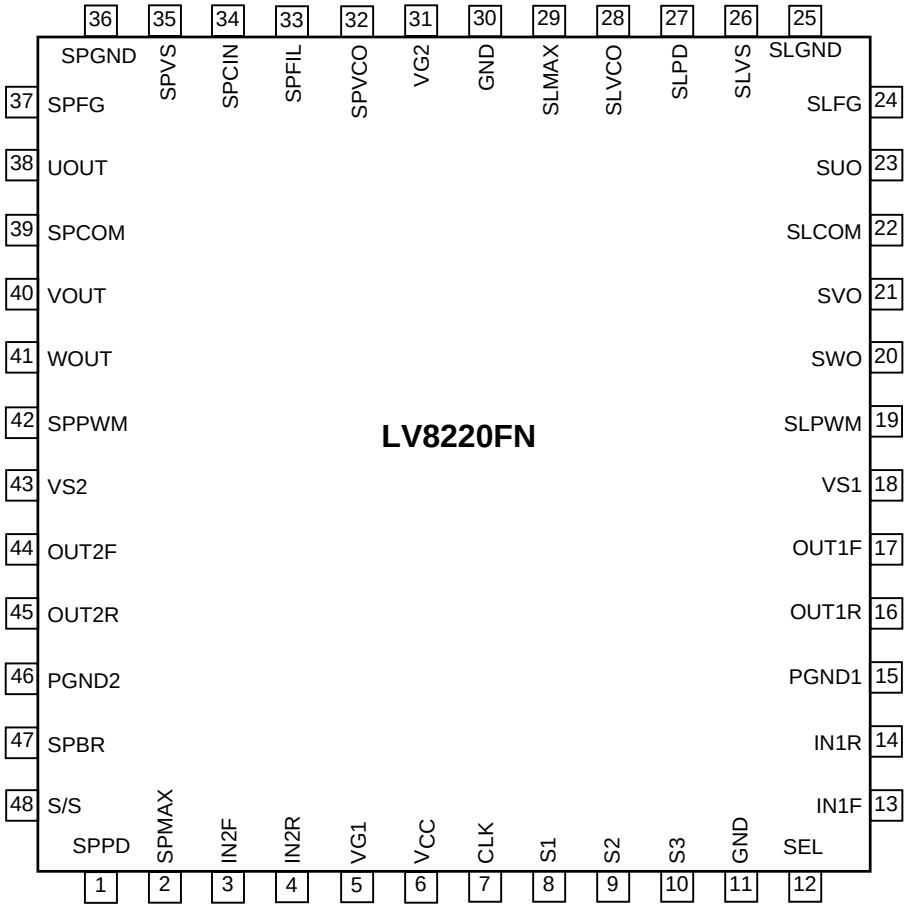
SLPWM	SINKOUT
H	ON
L	OFF

SPPWM	SINKOUT
H	ON
L	OFF

S/S Pin

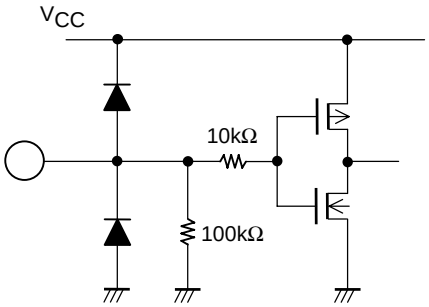
S/S	H-bridge	Sled	Spindle	Remarks
H	Operating	Operating	Operating	Operating mode
L	Stopped	Stopped	Stopped	Power saving mode

Pin Assignment



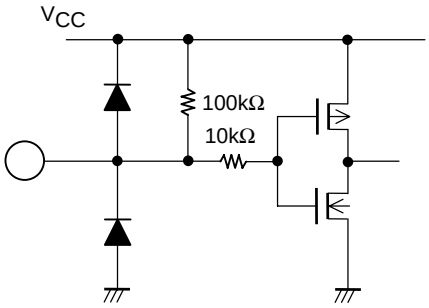
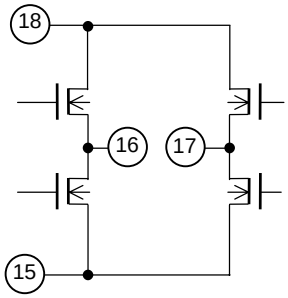
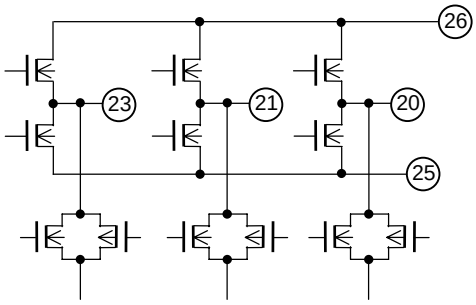
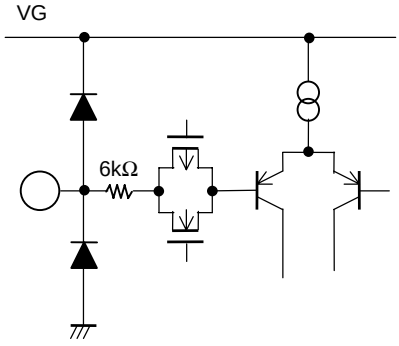
Top view

Pin Functions

Pin No.	Pin Name	Pin Description	Equivalent Circuit
13,14 3,4	IN1F/R IN2F/R	Actuator H-bridge logic input.	
7	CLK	Logic system reference clock input. Provide a frequence that is 32 times that of the PWM frequency.	
12	SEL1	Three-phase sled mode switching input. When high, the block operates in sensorless drive mode, and when low, the block operates in stepping drive mode.	
19	SLPWM	Sled drive block PWM signal input. When high, the control output transistor (SINK) is turned on.	
42	SPPWM	Spindle drive block PWM signal input. When high, the control output transistor (SINK) is turned on.	
47	SPBR	Spindle drive block brake input. When low, reverse torque braking is applied.	
48	S/S	Start/stop input. When high, all of the spindle, sled, and actuator blocks operate. When low, the IC goes to the standby state (power saving mode).	

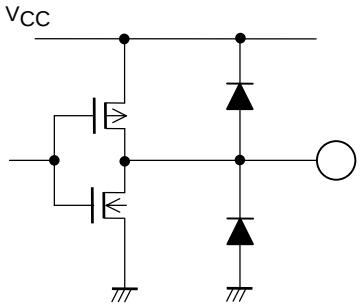
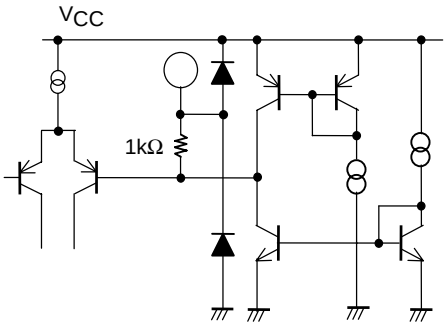
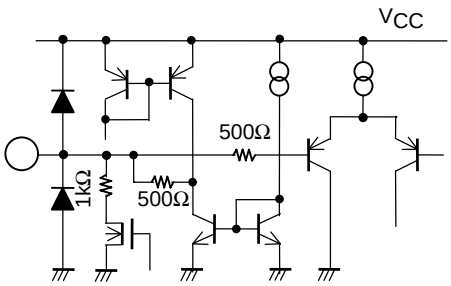
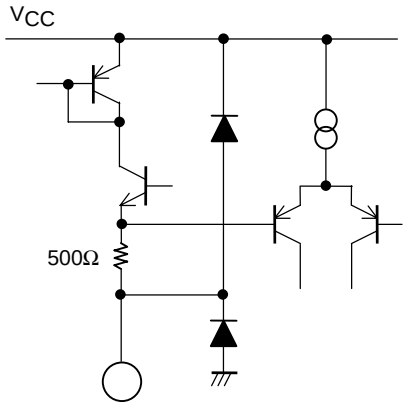
Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Pin Description	Equivalent Circuit
8	S1	Decoder input in sled stepping motor mode. Functions as the forward/reverse switching input in sensorless mode (SEL1: high, SEL2: low) and in H-bridge mode (SEL2 high).	
9	S2	Decoder input in sled stepping motor mode. Functions as the BRK (braking) switching input in sensorless mode (SEL1: high, SEL2: low). (A high-level input applies braking.)	
10	S3	Decoder input in sled stepping motor mode.	
5	VG1	Predriver power supply. Used as the power supply for the source side predrivers, the internal regulator (VG2), and the sensorless driver position detection comparator. Insert a capacitor between this pin and ground.	
6	V_{CC}	Small- signal system power supply. Insert a capacitor between this pin and ground.	
18	VS1	H-bridge circuit 1 power supply. Insert a capacitor between this pin and PGND1 (pin 15).	
16,17	OUT1F/R	H-bridge circuit 1 output.	
15	PGND1	H-bridge circuit 1 ground.	
26	SLVS	Sled drive block power supply. Insert a capacitor between this pin and SLGND (pin 25).	
23 21 20	SUO SVO SWO	Sled driver output. Connect this pin to the sled motor coil.	
25	SLGND	Sled drive block ground.	
22	SLCOM	Three-phase sled block position detection comparator common side input. Connect this pin to the sled motor center point connection.	
39	SPCOM	Spindle block position detection comparator common side input. Connect this pin to the spindle motor center point connection.	

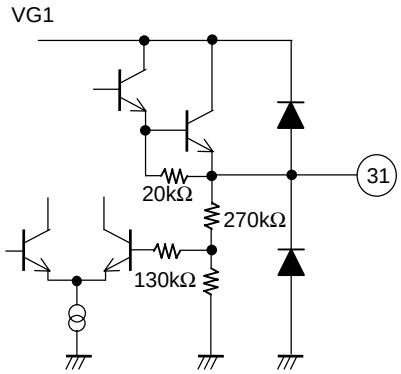
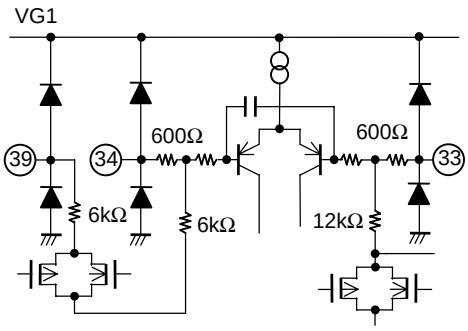
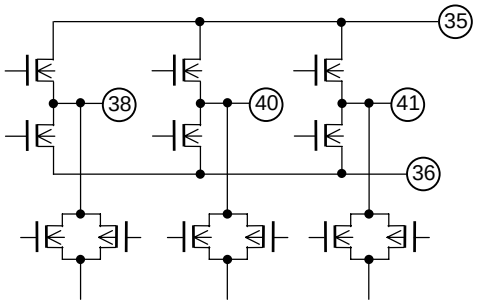
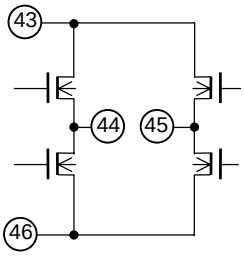
Continued on next page.

Continued from preceding page.

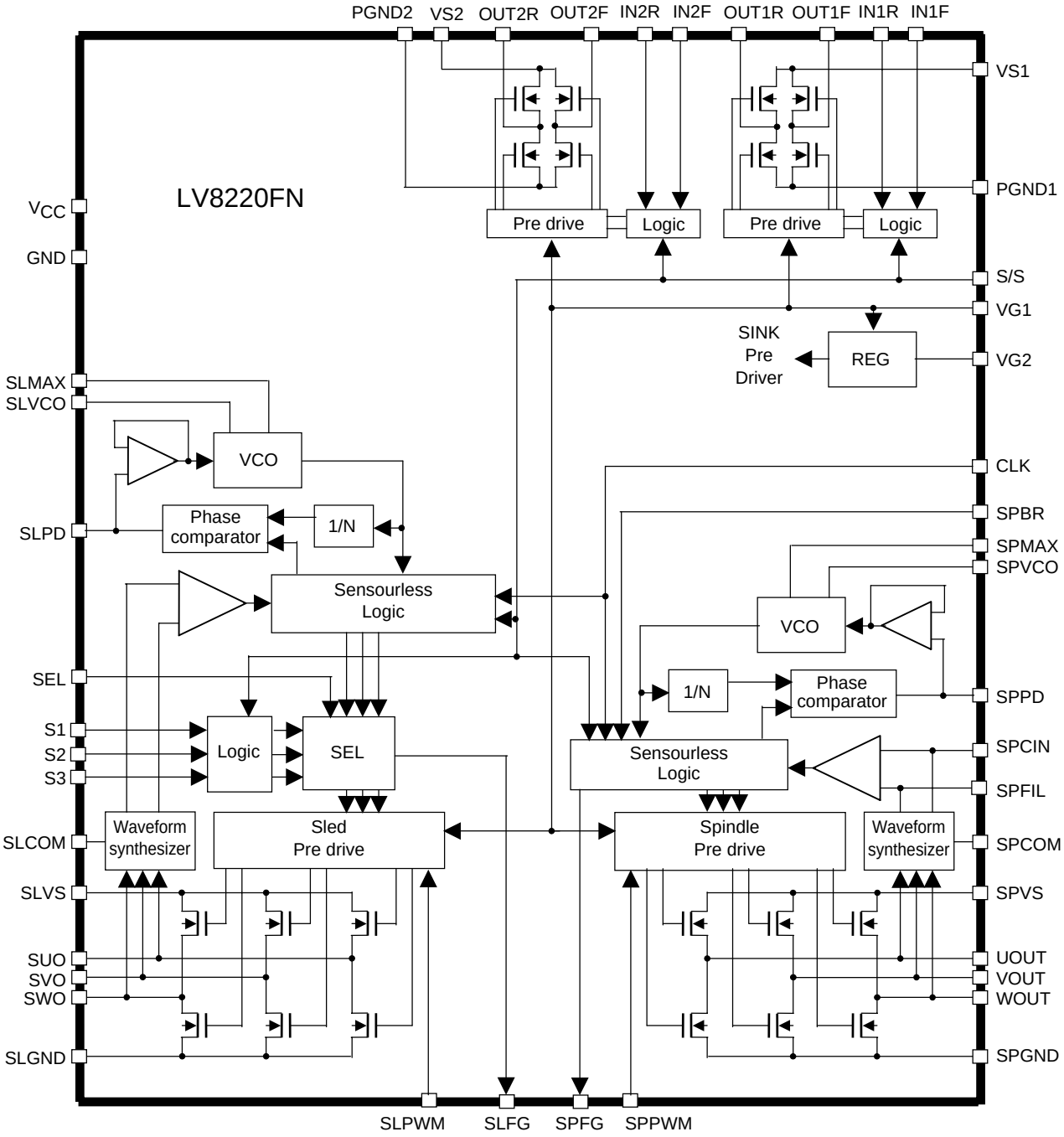
Pin No.	Pin Name	Pin Description	Equivalent Circuit
24	SLFG	Sled block position detection comparator output. When a stepping mode is used, this pin outputs a comparator signal equivalent to that provided in systems that use three Hall sensors, and when sensorless mode is used, the output is equivalent to a single Hall sensor system FG output. This pin outputs the low level in H-bridge mode.	
37	SPFG	Spindle block FG pulse output. This pin outputs a signal equivalent to a single Hall sensor system.	
27	SLPD	Sled sensorless block VCO control voltage input. Insert a capacitor between this pin and ground. In sensorless operating mode, a control voltage (the VCO control voltage) proportional to the motor speed is created.	
1	SPPD	Spindle block VCO control voltage input. Insert a capacitor between this pin and ground. A control voltage (the VCO control voltage) proportional to the motor speed is created.	
28	SLVCO	Sled block sensorless mode VCO oscillator connection. Insert a capacitor between this pin and ground. The VCO oscillator frequency follows the sled motor speed (the SLPD pin voltage).	
32	SPVCO	Spindle block VCO oscillator connection. Insert a capacitor between this pin and ground. The VCO oscillator frequency follows the spindle motor speed (the SPPD pin voltage).	
29	SLMAX	Sled block sensorless mode VCO maximum oscillator frequency setting. Reducing the value of the resistor connected to this pin increases the VCO oscillator frequency.	
2	SPMAX	Spindle block VCO maximum oscillator frequency setting. Reducing the value of the resistor connected to this pin increases the VCO oscillator frequency.	
11,30	GND	Small signal system ground	

Continued on next page.

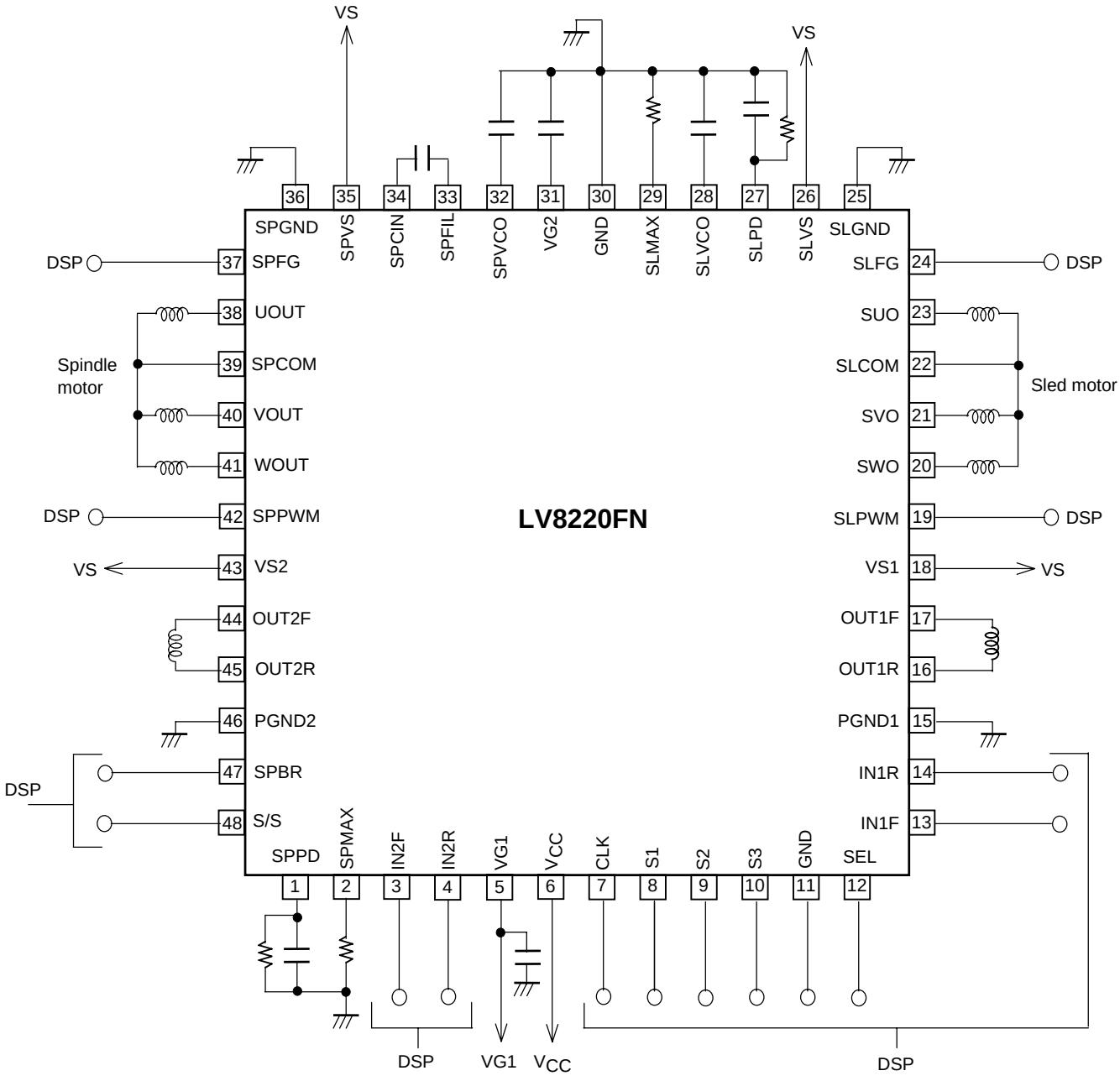
Continued from preceding page.

Pin No.	Pin Name	Pin Description	Equivalent Circuit
31	VG2	SINK side predrive drive regulator pin. Insert a capacitor between this pin and ground.	
39	SPCOM	Spindle motor common point connection.	
33	SPFIL	Spindle block position detection comparator waveform synthesizing signal filter connection. Insert a capacitor between this pin and SPCIN (pin 34).	
34	SPCIN	Spindle block position detection comparator differential input. Insert a capacitor between this pin and SPFIL (pin 33).	
35	SPVS	Spindle drive block power supply. Insert a capacitor between this pin and SPGND (pin 36).	
38 40 41	UOUT VOUT WOUT	Spindle driver outputs. Connect these pins to the spindle motor coil.	
36	SPGND	Spindle drive block ground.	
43	VS2	H-bridge circuit 2 drive power supply. Insert a capacitor between this pin and PGND2 (pin 46).	
44,45	OUT2F/R	H-bridge 2 outputs.	
46	PGND2	H bridge 2 output block ground connections	

Block Diagram



Sample Application Circuit



Insert a capacitor between VS and PGND and between V_{CC} and GND.

LV8220FN Functional Description and Notes on External Components

The LV8220FN is a system motor driver IC that can implement, with just a single chip, the motor driver circuits required for CD and MD systems. Since the LV8220FN provides not only a spindle driver, but drivers (with an H-bridge structure) for sled, focus, and tracking motors, it can contribute to miniaturization and thinner form factors in end products. Since the spindle and sled drivers adopt a direct PWM sensorless drive technique, they provide high efficiency motor drive with a minimal number of external components.
Read the following notes before designing driver circuits using the LV8220FN to design a system with fully satisfactory characteristics.

1. Channel Structure
   The LV8220FN drive circuits have the 4-channel structure shown below. To minimize power loss in the output blocks, this IC adopts synchronous commutation direct PWM (the recommended PWM frequency is 132kHz) in all channels, and at the same time, adopts low on-resistance DMOS devices (total high and low side on-resistance: 0.8Ω, typical) as the output transistors.
   Furthermore, this IC's sled driver channel can operate in either three-phase sensorless or three-phase stepper drive mode as selected by the SEL pin.

Applications	Three-pahse sensorless	Three-phase stepping	H-bridge	Remarks
Spindle	○			
Sled	○	○		Select the mode on SEL pin
Focus			○	
Tracking			○	

2. Power Supply Pins
   The LV8220FN has six power supply pins: the small signal system circuit power supply V_{CC} (pin 6), the source output gate drive power supply VG1 (pin 5), and power supplies for each of the output transistors, namely SPVS (pin 35), SLVS (pin 26), VS1 (pin 18), and VS2 (pin 43). All of these pins must be connected to an external power supply. (Since this IC does not include a built-in charge pump circuit for output gate drive, power must also be supplied to the VG1 pin.) Since VG2 (pin 31) is the output of an internal 4V regulator, there is no need to connect a power supply to this pin. Note that capacitor must be inserted between each power supply pin and ground.
   When power is first applied, it is desirable to apply power in the order VS first, then VG1, and finally V_{CC}. Although no problems with IC operation will occur of any other order is used, note that circuit current (I_{CC}) may flow during the period until all power supply levels have been provided.

3. S/S Circuit
   The S/S pin (pin 48) functions as the system start/stop pin. A high level starts IC operation and causes all channels to operate in drive mode. A low level switches the IC to the standby state (power saving mode). In the standby state, all power supply currents go to zero. Total system power consumption can be reduced by manipulating the S/S pin to operate the drivers intermittently.
   Note that the S/S pin must be held at the low level while the V_{CC} power supply level is first applied.

4. CLK Pin
   The LV8220FN CLK pin (pin 7) must be connected to the reference clock signal supplied by the DSP. The CLK signal is used as the reference clock for spindle block and sled block sensorless drive logic operation. Therefore, the CLK signal is always required in start mode. A frequency 32 times that of the PWM input signal must be provided as the CLK input signal. (Example: when the SPPWM and SLPWM input frequency is 132kHz, the CLK signal must be 4.224MHz.)

5. Spindle Driver Circuit

5.1 Speed Control Techniques

Spindle clock speed control uses the BRK control signal and the PWM control signal supplied by the external DSP. The PWM control signal from the DSP is input to the SPPWM pin (pin 42), and the sink (low) side transistor's duty is controlled according to the duty of the input signal to control the motor speed. When a high level is input to the SPPWM pin, the sink side transistor is turned on (i.e., acceleration is applied to the motor). The motor is decelerated by either applying short-circuit braking (by turning off the PWM signal), or by applying reverse torque braking by inputting a brake command to the SPBR pin (pin 47). The SPBR pin switches the direction of the torque applied by the driver; when a low level is input to the SPBR pin, the IC switches to reverse torque braking mode. When the motor has slowed to an adequately low speed in reverse torque braking mode (when SPBRK is low), the circuit switches to short-circuit braking to stop the motor.

Note that when stopping the motor with the braking function, if the timing with which this circuit switches to short-circuit braking is too fast and problems such as the motor remaining in motion occur, the value of the resistor connected to the SPMAX pin (pin 2) must be reduced. If the motor moves back and forth without stopping and the IC does not switch to short-circuit braking when the speed approaches zero, insert a resistor with a value from a few kΩ up to under 100kΩ at the SPCOM pin (pin 39). (Verify that insertion of this resistor does not degrade the startup characteristics.)

The spindle driver circuit uses variable-duty soft switching to reduce motor drive noise for quiet operation.

5.2 Spindle Block Position Detection Comparator Circuit

The spindle block position detection comparator circuit is provided to detect the position of the rotor using the back EMF generated when the motor turns. The IC determines the timing with which the output block applies current to the motor based on the position information acquired by this circuit. Startup problems due to comparator input noise can be resolved by inserting a capacitor (about 1000 to 4700pF) between the SPCIN pin (pin 34) and the SPFIL pin (pin 33). Note that if this capacitor is too large, the output commutation timing may be delayed at higher speeds and efficiency may be lowered.

5.3 VCO Circuit Constants

The LV8220FN spindle block adopts a sensorless drive technique. Sensorless drive is implemented by detecting the back EMF signal generated by the motor and setting the commutation timing accordingly. Thus the timing control uses the VCO signal. We recommend using the following procedure to determine the values of the VCO circuit's external components.

(1) Connect components with provisional values.
Connect a 1μF capacitor and a 4.7MΩ resistor in parallel between the SPPD pin (pin 1) and ground, connect a 68kΩ resistor between SPMAX (pin 2) and ground, and connect a 3300pF capacitor between SPVCO (pin 32) and ground.

(2) Determine the value of the SPVCO pin (pin 32) capacitor.
Select a value such that the startup time to the target speed is the shortest and such that the variations in startup time are minimized. If the value of this capacitor is too large, the variations in the startup time will be excessive, and if too small, the motor may fail to turn. Since the optimal value of the SPVCO pin constant differs with the motor characteristics and the startup current, the value of this component must be verified again if the motor used or any circuit specifications are changed.

(3) Determine the value of the SPMAX (pin 2) resistor.
Select a resistor value such that the SPPD pin voltage is about V_{CC}-1.0V or lower with the motor operating at the target maximum speed. If the value of this resistor is too large, the SPPD pin voltage may rise excessively.

(4) Determine the value of the SPPD pin (pin 1) capacitor.
If the SPFG output (pin 37) pulse signal becomes unstable at the lowest motor speed that will be used, increase the value of the SPPD pin capacitor.

(5) Determine the value of the resistor connected between the SPPD pin (pin 1) and ground.
The LV8220FN generates a VCO control voltage that corresponds to the spindle motor speed at the SPPD pin. When the S/S pin is used to implement intermittent drive to reduce system power consumption, the potential of the SPPD pin in power saving mode remains fixed at the level determined by the charge stored on the capacitor. Therefore, it is necessary to attach a large resistor (several MΩ) for voltage discharge to the SPPD pin. Choose a value for this resistor such that the time for complete discharge is longer than the motor free-running deceleration time. Note that if an oscilloscope probe is attached to the SPPD when determining the value of this constant, the discharge characteristics will differ due to the probe impedance. This issue requires care when testing in an actual system. (We recommend using an FET probe.) If intermittent drive (free-running deceleration) is not used, this discharge resistor is not required.

5.4 Spindle FG Output Circuit

The SPFG pin (pin 37) is the spindle block FG output, and outputs a pulse signal equivalent to a single Hall sensor FG output. This pin goes to the low level (MOS output circuit) in power saving mode and short braking stop mode. Note that the SPFG pin is susceptible to damage from ESD, and requires care during handling. (This only applies to the SPFG pin; the SLFG pin does not have this issue.)

6. Sled Driver Circuit

6.1 Mode Settings

The LV8220FN sled driver circuit has two modes, three-phase sensorless and three-phase stepper drive mode. The mode is selected with the SEL pin (pin 12). The functions of this IC's S1 to S3 pins (pins 8, 9, and 10) are switched according to the drive mode as shown in the table.

Operation mode	Mode settings	Pin name and function			Remarks
	SEL1	S1	S2	S3	
Three-phase stepping	L	Decoder input			SLFG outputs three Hall sensor equivalent.
Three-phase sensorless	H	F/R	BRK	-	SLFG outputs a Hall sensor equivalent

Note: When a low level is input to the S2 pin (F/R function), this circuit has the same commutation logic as the spindle block.

This IC’s sled driver can operate in speed control (torque control) mode controlled by a PWM signal input to the SLPWM (pin 19) pin. Like the sensorless block, torque control is applied to the sink side transistor, and the sink side transistor is turned on (for acceleration) when the SLPWM pin is high.

6.2 Stepping Mode Operation

Set the SEL pin low to use the sled driver in three-phase stepping mode.

Sled Motor Stepping Logic (When SEL is low)

S/S	S1	S2	S3	SUO	SVO	SWO	Inner area FG	Outer area FG	Inner area	Outer area
H	L	L	L	H	L	Z	L→H	H→L	↑	↓
H	H	L	L	H	Z	L	H→L	L→H	↑	↓
H	L	H	L	Z	H	L	L→H	H→L	↑	↓
H	H	H	L	L	H	Z	H→L	L→H	↑	↓
H	L	L	H	L	Z	H	L→H	H→L	↑	↓
H	H	L	H	Z	L	H	H→L	L→H	↑	↓
H	L	H	H	Z	Z	Z	L	L	Change to the decoder input	Change to the decoder input
H	H	H	H	Z	Z	Z	L	L		
L	×	×	×	Z	Z	Z	L	L		

Notes: Z: Open (both the high side and low side transistors off)

The inner/outer changes follow the specifications of the Sanyo LC896442 DSP.

The stepping mode drive logic operates as shown in the table. The S1 to S3 pins (pins 8, 9, and 10) are the sled driver decoder inputs and include internal pull-up resistors. These pins are connected to the DSP. The LV8220FN allows the drive torque to be controlled by the signal input to the SLPWM pin (pin 19). (This circuit supports synchronous commutation.)

The SLFG pin (pin 24) is the sled driver position detection comparator output, and has a MOS output circuit. In stepping mode, it outputs a signal equivalent to a three-phase FG signal. This pin's output signal is used to feed back the sled motor speed information (position information) to the DSP or microcontroller.

6.3 Sensorless Mode Operation and Determining External Component Values

When the sled driver is used in three-phase sensorless mode, set the SEL1 pin high and the SEL2 pin low. Although basic operation in sensorless mode is the same as that of the spindle block, the sled sensorless mode has a forward/reverse function and uses a hard switching drive method.

The S1 pin (pin 8) is used for forward/reverse switching in sled sensorless mode, and the S2 pin (pin 9) is used for braking. The IC applies reverse torque braking when S2 is set high. (Note: this has the reverse phase input from that of the spindle block braking pin, SPBRK.)

Like the spindle driver, reverse torque braking mode (when S2 is high) slows the motor to and adequately slow speed, switches to short-circuit braking state, and stops. Note that when stopping the motor with the braking function, if the timing with which this circuit switches to short-circuit braking is too fast and problems such as the motor remaining in motion occur, the value of the resistor connected to the SLMAX pin (pin 29) must be reduced. If the motor moves back and forth without stopping and the IC does not switch to short-circuit braking when the speed approaches zero, insert a resistor with a value from a few kΩ up to under 100kΩ at the SLCOM pin (pin 22). (Verify that insertion of this resistor does not degrade the startup characteristics.)

Although the sled driver can be set to the standby state by stopping the motor with the S2 (brake) pin, the internal circuits used for sensorless drive will continue to operate. Therefore, it is desirable to set the circuit to the standby state in stepping mode to minimize circuit current.

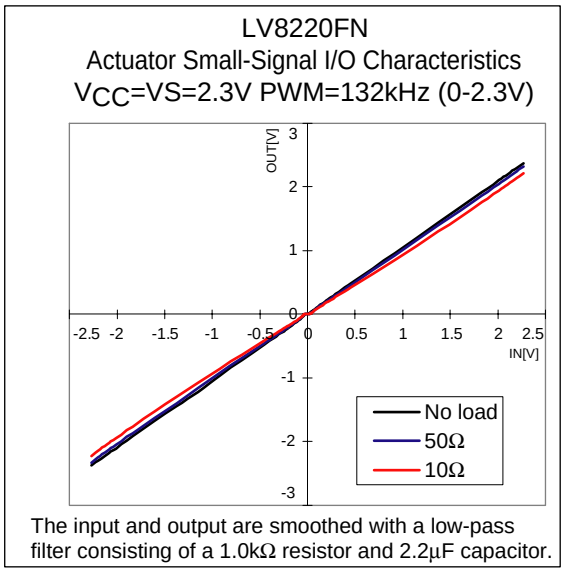
The procedure for determining the VCO circuit external component values for sled sensorless mode is essentially the same as that for the spindle block VCO external components. (See the description of that procedure earlier in this document.) For the initial provisional component values, connect a 1μF capacitor and a 4.7MΩ resistor in parallel between the SLPD pin (pin 27) and ground, connect a 56kΩ resistor between SLMAX (pin 29) and ground, and connect a 1500pF capacitor between SLVCO (pin 28) and ground. Then determine the optimal capacitance for SLVCO, the optimal resistance for SLMAX, and the optimal capacitance and resistance for SLPD.

In sled sensorless mode, the SLFG pin outputs a pulse signal equivalent to a single Hall sensor FG signal.

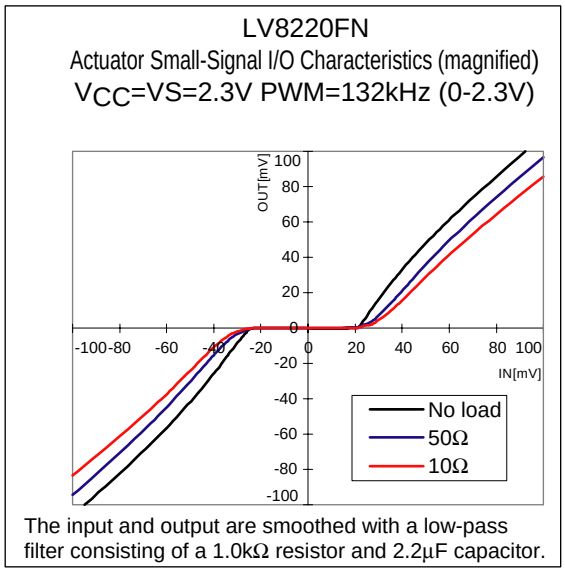
7. Actuator Block

The LV8220FN incorporates three H-bridge channels for use as actuator drivers for the focus and tracking systems. The logic input pin include built-in pull-down resistors. A PWM signal is used for control, and the circuit supports synchronous commutation.

The figures below show reference data related to the dead band during control.



The input and output are smoothed with a low-pass filter consisting of a 1.0kΩ resistor and 2.2μF capacitor.



The input and output are smoothed with a low-pass filter consisting of a 1.0kΩ resistor and 2.2μF capacitor.

8. Notes on PCB Pattern Design

The LV8220FN is a system driver IC implemented in a Bi-DMOS process; the IC chip includes bipolar circuits, MOS logic circuits, and MOS drive circuits integrated on the same chip. As a result, extreme care is required with respect to the pattern layout when designing application circuits.

1) Ground and V_{CC}/VS wiring layout

The LV8220FN ground and power supply pins are classified as follows.

Small-signal system ground pins → GND (pin 30)

Large-signal system ground pins → PGND1 (pin 15), PGND2 (pin 46), SPGND (pin 36), SLGND (pin 25)

Small-signal system power supply pin → V_{CC} (pin 6)

Large-signal system power supply pins → VS1 (pin 18), VS2 (pin 43), SPVS (pin 35), SLVS (pin 26)

A capacitor must be inserted, as close as possible to the IC, between the small-signal system power supply pin (pin 6) and ground pins (pin 30).

The large-signal system ground pins (PGND system) must be connected with the shortest possible lines, and furthermore in a manner such that there is no shared impedance with the small-signal system ground lines.

Capacitors must also be inserted, as close as possible to the IC, between the large-signal system power supply (VS system) pins and the large-signal system ground pins.

2) Positioning the small-signal system external components

The small-signal system external components that are also connected to ground must be connected to the small-signal system ground with lines that are as short as possible.