SH Graphics/Speech Processing Demonstration System NAV-DS4

Application Note

HITACHI

ADE-502-058
Rev. 1.0
Preliminary
11/25/99
Hitachi, Ltd.

Hitachi semiconductor

Notice

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

Preface

This Application Note covers the hardware and software of the NAV-DS4 navigation SH graphics/speech processing demonstration system developed by Hitachi, Ltd. It includes a number of practical examples intended for use as reference material when designing a navigation system using an SH3 microcomputer and Q2 graphics renderer (however, note that NAV-DS4 does not support GPS (Global Positioning System)).

The NAV-DS4 uses a variety of Hitachi semiconductor devices, including an SH3 (SH7708) 32-bit RISC processor, Q2 (HD64411) 2-dimensional (2D) graphics renderer, 16M DRAM (HM51W18165), and 8M flash memory (HN29WT800).

Demonstration application software provided with the NAV-DS4 comprises map drawing and display, YUV natural image display, ADPCM speech output. All of this software runs on an HI-SH77 real-time operating system conforming to the µITRON standard.

Operation, performance, and standards as a product are not guaranteed for the NAV-DS4. The operation of the electronic circuits and software included in this Application Note must be evaluated and confirmed by the user before use in an actual application system.

Contents

Section 1 Overview

1.1 System Specifications

Table 1.1 summarizes the specifications of the navigation graphics demonstration system covered in this Application Note.

Table 1.1 Navigation Graphics Demonstration System Specifications

Item		Specifications	Notes
Product code		NAV-DS4	
Product name		Navigation graphics demonstration system	
Mother board	CPU	SH-3 (SH7708)	Internal operating frequency: 60 MHz
	RAM	EDO-DRAM (4 Mbyte) *1	
		SRAM (256 kbyte) *2	
	ROM	Flash memory (8 Mbyte)	
Daughter board	Graphics renderer	Q2 *3	Operating frequency: 30 MHz
	UGM	EDO-DRAM (4 Mbyte)	
CD-ROM drive		Max. 10X (SCSI) *4	Data transfer speed: 1.5 Mbytes/sec
Embedded OS		HI-SH77	Real-time multitasking OS conforming to µITRON specifications Ver. 2.02
Graphics processing	Map data	Conforms to Navigation System Researcher's Association unified standard	
	Display colors	8 bits/pixel: 256 of 260,000 colors	
		16 bits/pixel: 60,000 colors	
	Display size	320 × 240	
	Functions	5-level reduction/enlargement	
		4-directional smooth scrolling	Dot units (up/down/left/right)
		360-degree rotation	Degree units (left rotation/ right rotation)
		Restoration and playback of ΔYUV-compressed natural images	Q2 hardware

Table 1.1 Navigation Graphics Demonstration System Specifications (cont)

Item		Specifications	Notes
Speech processing	Functions	Restoration and playback of ADPCM-compressed speech *6	SH3 software

Notes:
1. EDO: Extended Data Out—Dynamic Random Access Memory
2. SRAM: Static Random Access Memory
3. Q2: Quick 2D Graphics Renderer
4. SCSI: Small Computer System Interface
5. TRON: The Real Time Operating System Nucleus
   µITRON: Micro Industrial TRON
6. ADPCM: Adaptive Delta Pulse Code Modulation

1.2 System Configuration

Figure 1.1 shows the system configuration.

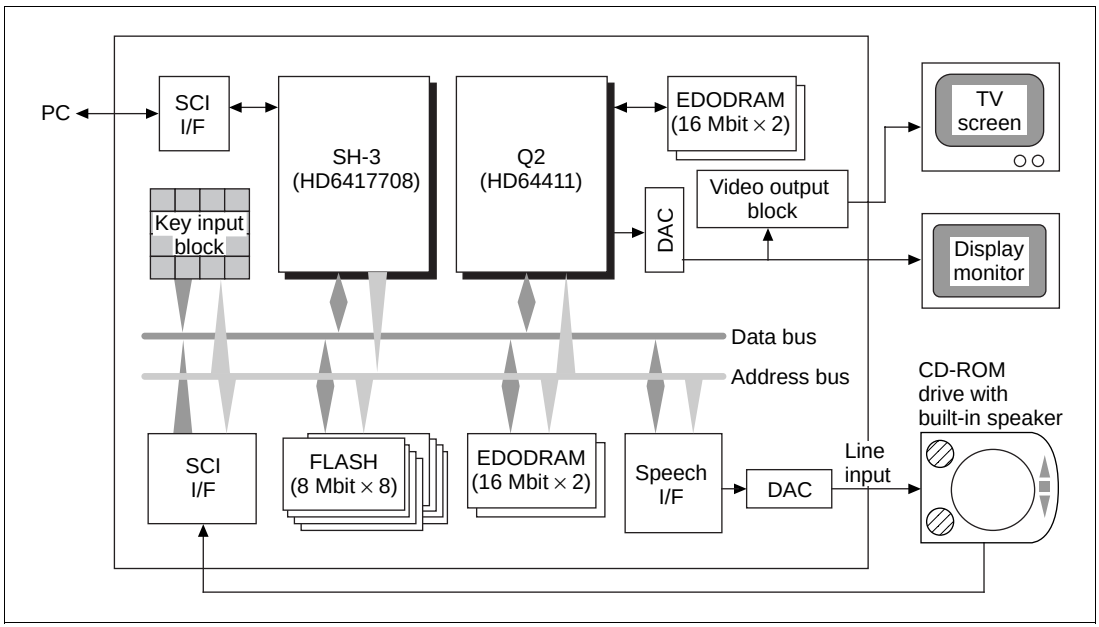


Figure 1.1 System Configuration

This demonstration system consists of a mother board holding a 32-bit RISC processor (SH7708: 60 MHz operation), a daughter board holding a graphics renderer (Q2: 30 MHz operation), and a CD-ROM drive that reads map data from a CD-ROM.

In graphics processing, the SH7708 handles geometrical operations while the Q2 is responsible for rendering (drawing) operations. This reduces the processing load on the SH processor and improves system bus utilization.

In speech processing, real-time regeneration of ADPCM speech data is possible by means of high-speed processing using the SH7708, enabling the number of dedicated devices used, and system cost, to be reduced.

A real-time multitasking OS (operating system) conforming the µITRON specifications is incorporated, enabling both independent and parallel processing, and increasing the real-time capabilities of the system.

1.3 Drawing and Display Processing Procedure

Figure 1.2 shows the map drawing flow in the NAV-DS4. The procedure is outlined below.

1. Management information, text, and map data are read from CD-ROM and stored in DRAM.

2. The SH7708 performs coordinate conversion on the map data and transfers the converted data to DRAM.

3. The SH7708 regenerates the display list (list of Q2 drawing commands) from the coordinate map data in DRAM, and transfers this to the Q2's UGM.

4. The SH7708 enables drawing execution by the Q2. The Q2. performs drawing in accordance with the display list. The SH7708 can execute other tasks while the Q2 is drawing.

5. The Q2 uses a double-buffering system with a drawing plane and a display plane , so that the display plane can be displayed during drawing. Display control is performed by the Q2 itself, without involving the SH7708.

6. When drawing ends, the drawing plane and display plane are switched. Screen switching control by the Q2 or the SH7708 can be selected.

7. In 8-bit/pixel mode, dot-unit data is converted to any of 256 colors from among 260,000 colors with the color palette (CPLT: ColPalet). In 16-bit/pixel mode, 60,000 colors can be displayed.

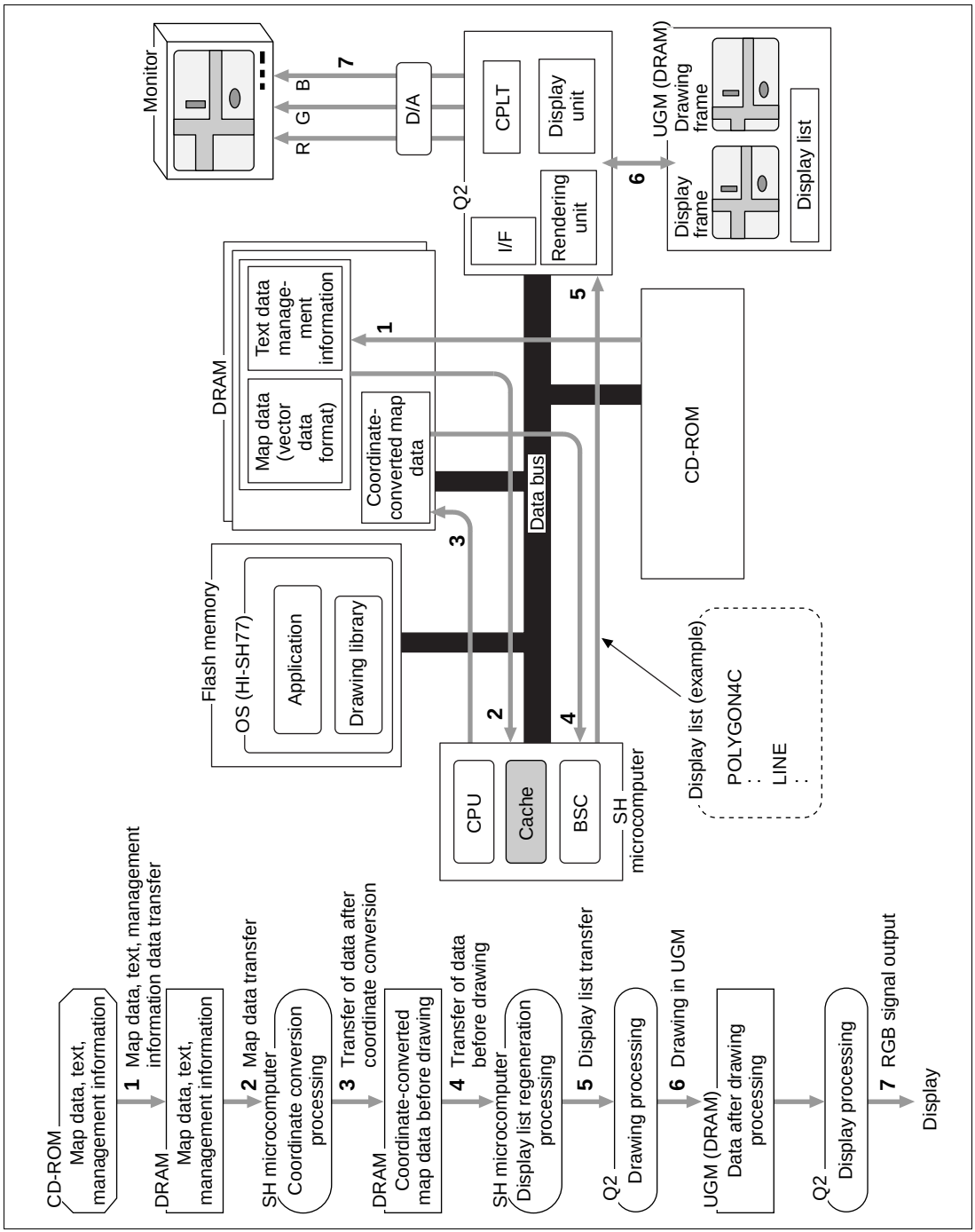


Figure 1.2 Drawing and Display Processing Flow

1.4 External Appearance of NAV-DS4

Figure 1.3 shows an external view of the NAV-DS4. The NAV-DS4 consists of a mother board, a daughter board, a CD-ROM drive, and a monitor. The system is operated by means of operating key switches on the mother board. The operating keys are shown in figure 1.4.

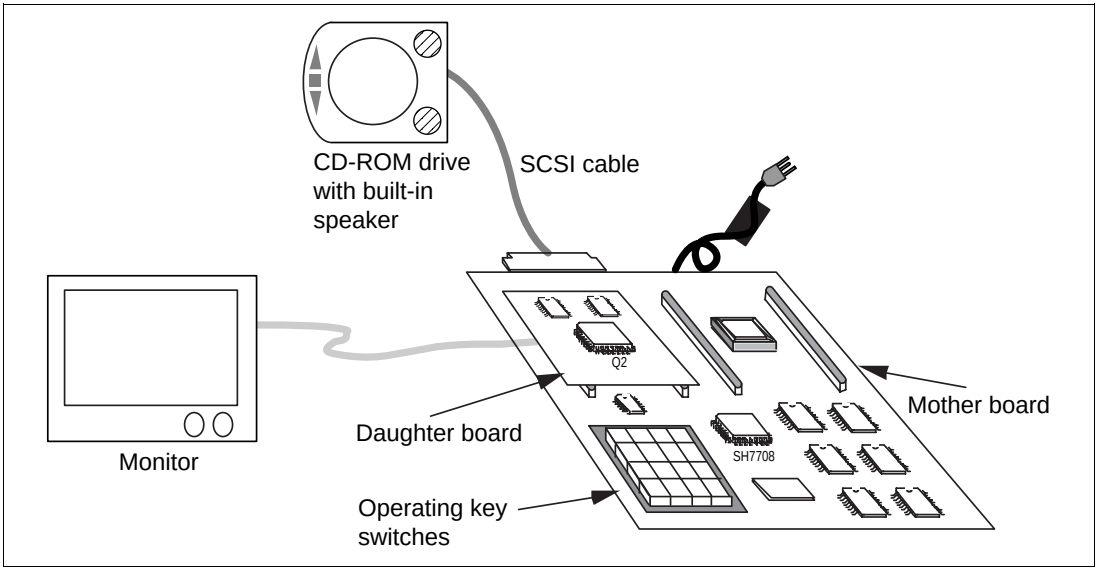


Figure 1.3 External View of NAV-DS4

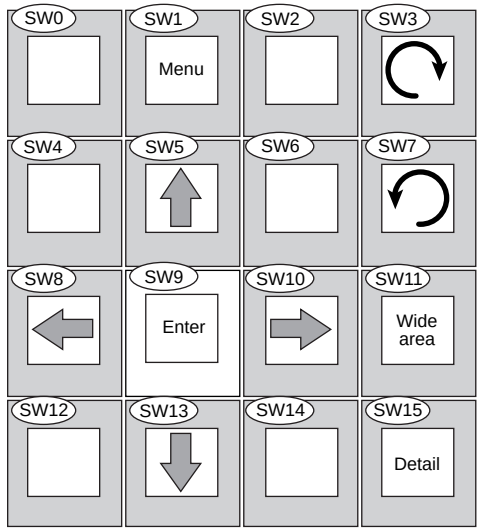


Figure 1.4 NAV-DS4 Operating Key Panel Layout

1.5 Operating Procedures

NAV-DS4 operating procedures are described here. Be sure to read the Usage Notes in the following section before operating the NAV-DS4.

(1) Demonstration System Setup Procedure (See Figure 1.5)

1. Place the mother board, CD-ROM drive, and monitor on a table, desk, or similar flat surface as shown in the figure below.
2. Connect the daughter board to the mother board connector as shown in the figure.
3. Connect the SCSI cable and monitor cable.
4. Connect the power cords to the CD-ROM drive and monitor, plug them into a 100 VAC power outlet, and turn on the power.
5. Insert a Navigation System Research Association format CD-ROM in the prescribed position in the CD-ROM drive, and turn on the CD-ROM drive power.
6. Check steps 2 to 5 again, then plug the power cord connected to the mother board into a 100 VAC power outlet, and turn on the power.

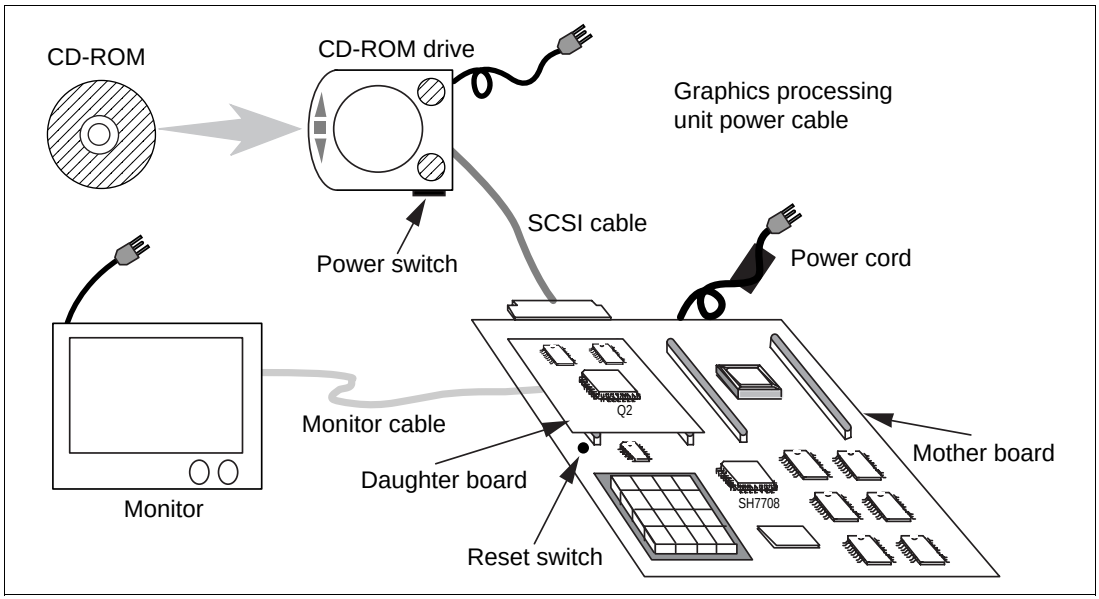
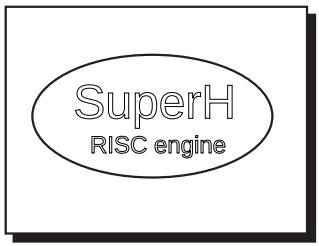
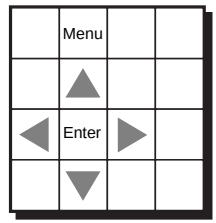
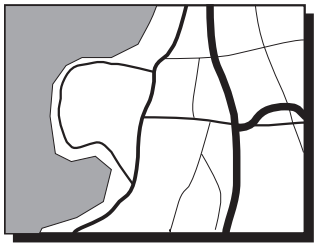
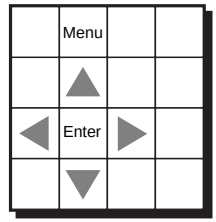
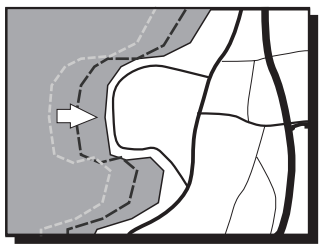
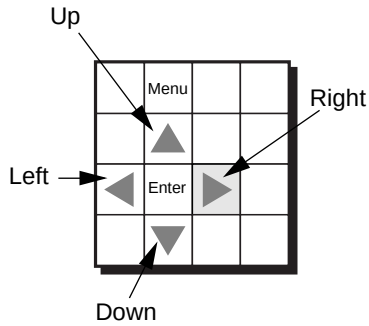


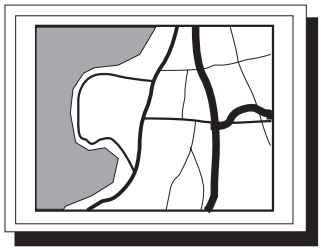
Figure 1.5 NAV-DS4 Setup Procedure Diagram

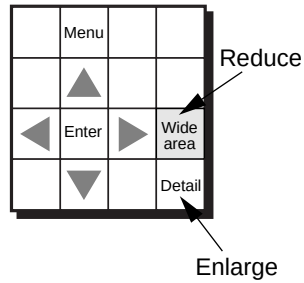
(2) Operations after Setup (Examples)

Display Screen	SW Board Operations	Description
Initial screen on powering on		
Initial screen 	No operation necessary 	When power is turned on, the initial screen is displayed. (Automatic)
Map screen display		
Map screen is displayed 	No operation necessary 	After the initial screen is displayed, map data is read from the CD-ROM, drawing is performed, and the result is displayed on the screen. (Automatic)
Map screen scrolling		
		Scrolling (in any of 4 directions) continues while the up, down, left, or right key is pressed on the SW board, and stops when the key is released.

Display Screen	SW Board Operations	Description

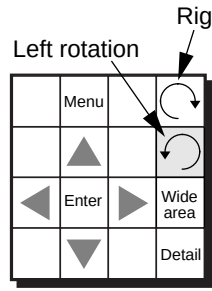
Map screen enlargement/reduction





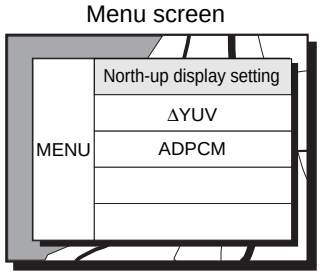
Pressing the Detail key in the SW board displays a map enlarged by one level; pressing the Wide Area key displays a map reduced by one level. (5 enlargement/reduction levels available)

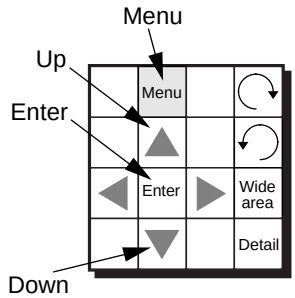
Map screen rotation



The map is rotated (in degree units) about the center of the screen while a rotation key on the SW board is pressed. Rotation stops when the key is released.

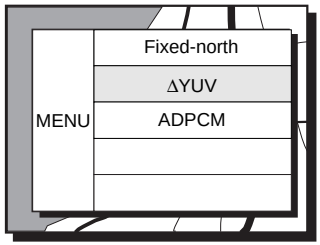
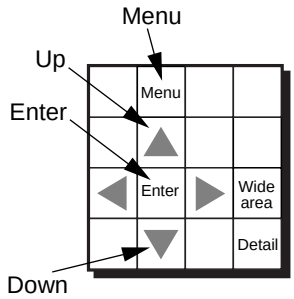
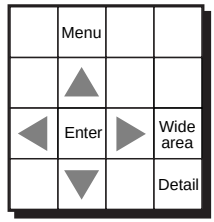
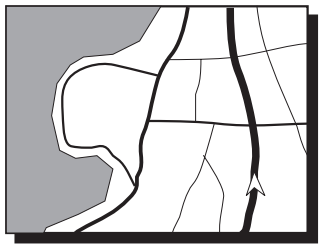
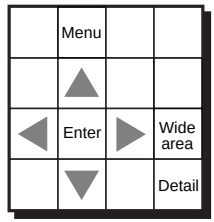
Setting after rotation





After a map rotation demonstration, press the Menu key on the SW board, select “North-up display setting,” and press the Enter key. The display will return to its state prior to the rotation.

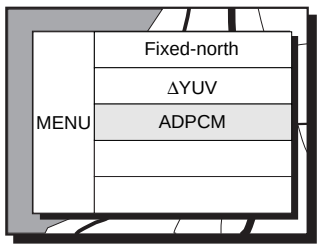
(3) YUV Demonstration Operations

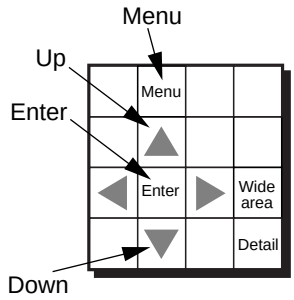
Display Screen	SW Board Operations	Description
Starting ΔYUV demonstration		
		Press the menu key to display the menu screen, and move the cursor to "ΔYUV" with the up/down keys. The ΔYUV demonstration is started by pressing the Enter key.
ΔYUV demonstration		
		The ΔYUV natural image display demonstration is an automatic demonstration (no key input required).
End of ΔYUV demonstration		
		The automatic demonstration ends after approximately one minute, and the map screen is displayed again.

(4) ADPCM Demonstration Operations

Display Screen	SW Board Operations	Description

Starting ADPCM demonstration

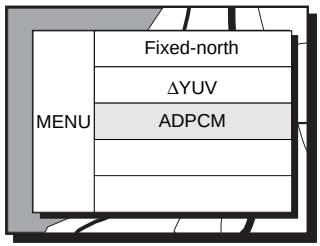


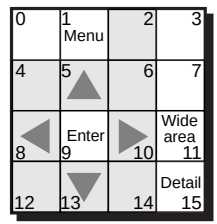


Press the menu key to display the menu screen, and move the cursor to “ADPCM” with the up/down keys. The ADPCM demonstration is started by pressing the Enter key.

Phrase playback

: Phrase playback keys





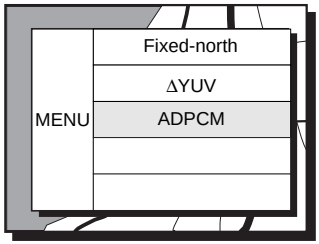
Pressing a phrase playback key plays the phrase assigned to that key. The phrase playback keys arranged so that a sentence can be constructed from four phrases (including chimes) by selecting a phrase from each row in turn, starting at the top row and moving downward. (The phrase arrangement is shown on the left.)

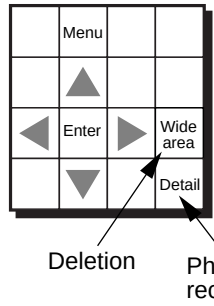
Keys and corresponding phrases

Key No.	Phrase	Meaning
2	Pin-pon	Chimes
4	O-yo-so	Approximately
5	Ko-no-sa-ki	Ahead
6	Ryou-ki-n-jo-no-sa-ki	Beyond the tollbooth
8	Ichi-ki-ro-mei-to-ru-de	1 km
10	Ni-ki-ro-mei-to-ru-de	2 km
12	Ji-ta-ku-de-su	Your home
13	Mo-ku-te-ki-chi-de-su	Your destination
14	De-gu-chi-de-su	The exit

Display Screen	SW Board Operations	Description

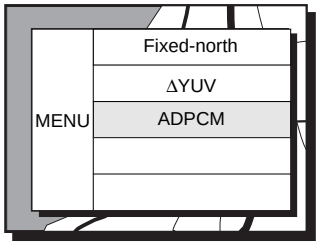
Phrase recording/deletion

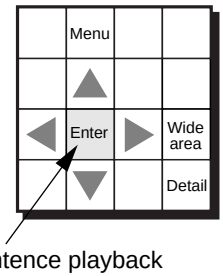




Pressing the record key (Detail) will record the phrase played immediately before. The maximum number of recordings is set at 5.
Pressing the delete key (Wide Area) will delete the phrase recorded immediately before. This is used to delete a phrase recorded by mistake.

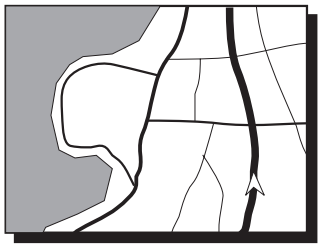
Sentence playback

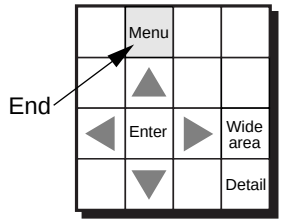




Pressing the sentence playback key (Enter) will play the recorded phrases as a sentence.

Ending ADPCM demonstration





Pressing the end key (menu) will end the ADPCM demonstration and display the map screen again.

1.6 Usage Notes

1. The power supply must be 100 VAC. The NAV-DS4 can be used in both 50 Hz and 60 Hz regions.

2. Always grip the plug when connecting or removing a power cord.

3. System damage, fire, or electric shock may result if a power cord, power cable, or flat cable is stretched, bent, extended, touched with wet hands, or inserted the wrong way round.

3. This system is a navigation demonstration unit, and is not covered by the same after-sales service warranty as other Hitachi products.

5. This system has been developed for use under normal environmental conditions (normal temperature and humidity). Special consideration has not been given to variations in environmental conditions or secular change.

6. If a demonstration does not operate normally (fails to work when power is turned on) or halts, press the Reset button. If this does not restore normal operation, disconnect and the reconnect the mother board power supply. If repeated use of these methods fails to restore normal operation, consult the manufacturer.

7. If the CD-ROM drive races out of control, turn of the power immediately.

8. Remove any dust from CD-ROM disks before use, as this may prevent data from being read.

Section 2 NAV-DS4 Software

2.1 Overview of Demonstration System

The NAV-DS4 can execute the following four kinds of demonstration.

1. Map drawing and display demonstration (scrolling, zooming, rotation)

   Map data is read from a Navigation System Researcher's Association format CD-ROM and drawing and display are performed. The drawn map can be scrolled up, down, left, or right in dot units, enlarged or reduced in 5 stages, and rotated through 360 degrees.

2. Natural image (YUV image) display demonstration

   Natural image data that has undergone YUV compression is read from a Navigation System Researcher's Association format CD-ROM, high-speed conversion from YUV data to RGB data is performed using the Q2, and the result is displayed. During display, the converted data is enlarged/reduced, transformed, rotated, etc., using the high-speed drawing functions of the Q2.

3. ADPCM speech playback demonstration

   Speech data that has undergone ADPCM compression is read from a Navigation System Researcher's Association format CD-ROM, restored using ADPCM restoration middleware, and played via the speaker.

Operations for these demonstrations are carried out by means of the key switches on the board. Table 2.1 lists the key functions, and figure 2.1 shows the overall NAV-DS4 demonstration software configuration.

Table 2.1 Key Functions

Function	Key		Functions		
	Mark	Assigned No.	In Map Drawing	In Menu Selection	In ADPCM Demonstration
Scrolling		5	To look above display map screen	Selects item above	Reads ADPCM speech data
		d	To look below display map screen	Selects item below	Reads ADPCM speech data
		8	To look to left of display map screen	—	Reads ADPCM speech data
		a	To look to right of display map screen	—	Reads ADPCM speech data
Rotation		7	Left (anticlockwise) rotation	—	—
		3	Right (clockwise) rotation	—	—
Enlargement/ reduction	Wide area	b	Reduces display map	—	Deletes data recorded immediately before
	Detail	f	Enlarges display map	—	Records selected data
Menu selection	Enter	9	—	Starts selected application	Outputs recorded data as sentence
	MENU	1	Displays menu screen	—	Ends ADPCM demonstration
Other		2	—	—	Reads ADPCM speech data
		4	—	—	Reads ADPCM speech data
		6	—	—	Reads ADPCM speech data
		c	—	—	Reads ADPCM speech data
		e	—	—	Reads ADPCM speech data
		0	—	—	—

—: Invalid (pressing this key has no effect).

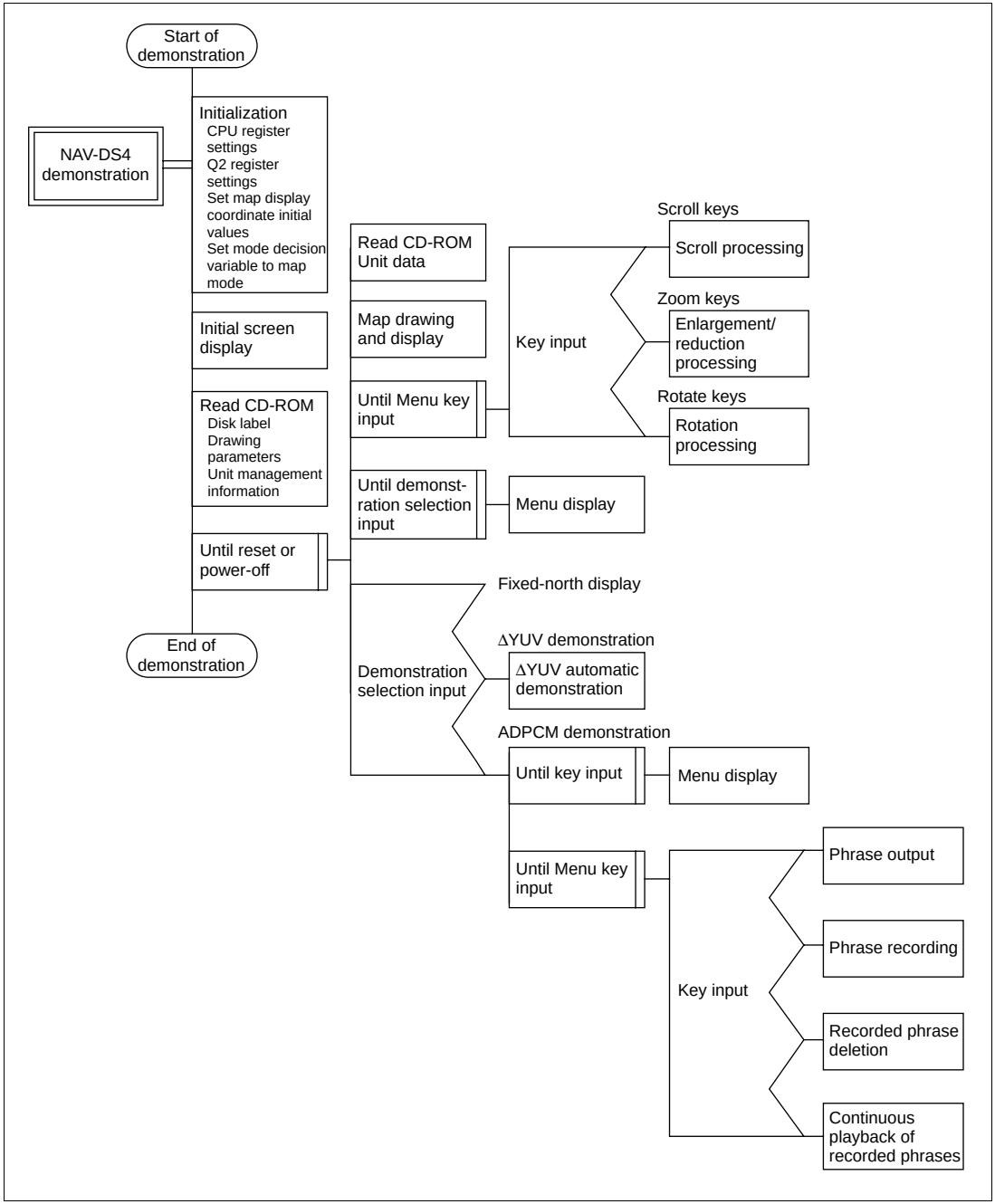


Figure 2.1 Overall NAV-DS4 Demonstration Software Configuration

2.2 Overall Software Configuration

The NAV-DS4 incorporates an HI-SH77 real-time multitasking operating system conforming to the µITRON standard. Application programs are divided into processing units which are recorded in the kernel as “tasks.” A maximum of 1023 tasks can be recorded. The kernel identifies and manages each task by means of a number from 1 to 1023 called the task ID. Tasks are activated via the kernel by means of asynchronously generated events such as key input operations.

Interrupt handlers are also created to handle processing by interrupts. When an interrupt occurs, control is passed to an interrupt handler via an exception service routine in the kernel. The NAV-DS4 uses a variety of interrupts, including key input, SCSI protocol control, and CD-ROM drive data reads.

Having the operating system manage and control program flow in this way enables efficient, real-time demonstration operations to be implemented. The relationship between tasks and the kernel in the NAV-DS4 is illustrated in figure 2.2. For detailed specifications of the HI-SH77 operating system, refer to the HI-SH77 User’s Manual and Construction Manual.

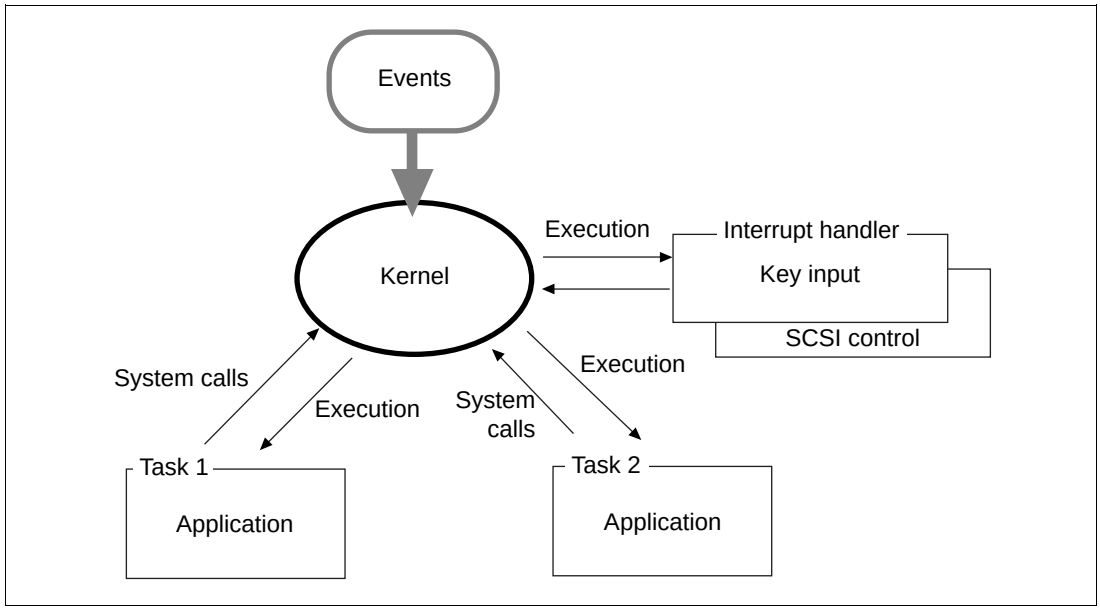


Figure 2.2 Relationship Between Tasks and Kernel

2.3 Task Configuration

Figure 2.3 shows the configuration of the tasks and interrupt handlers recorded in the kernel by the NAV-DS4.

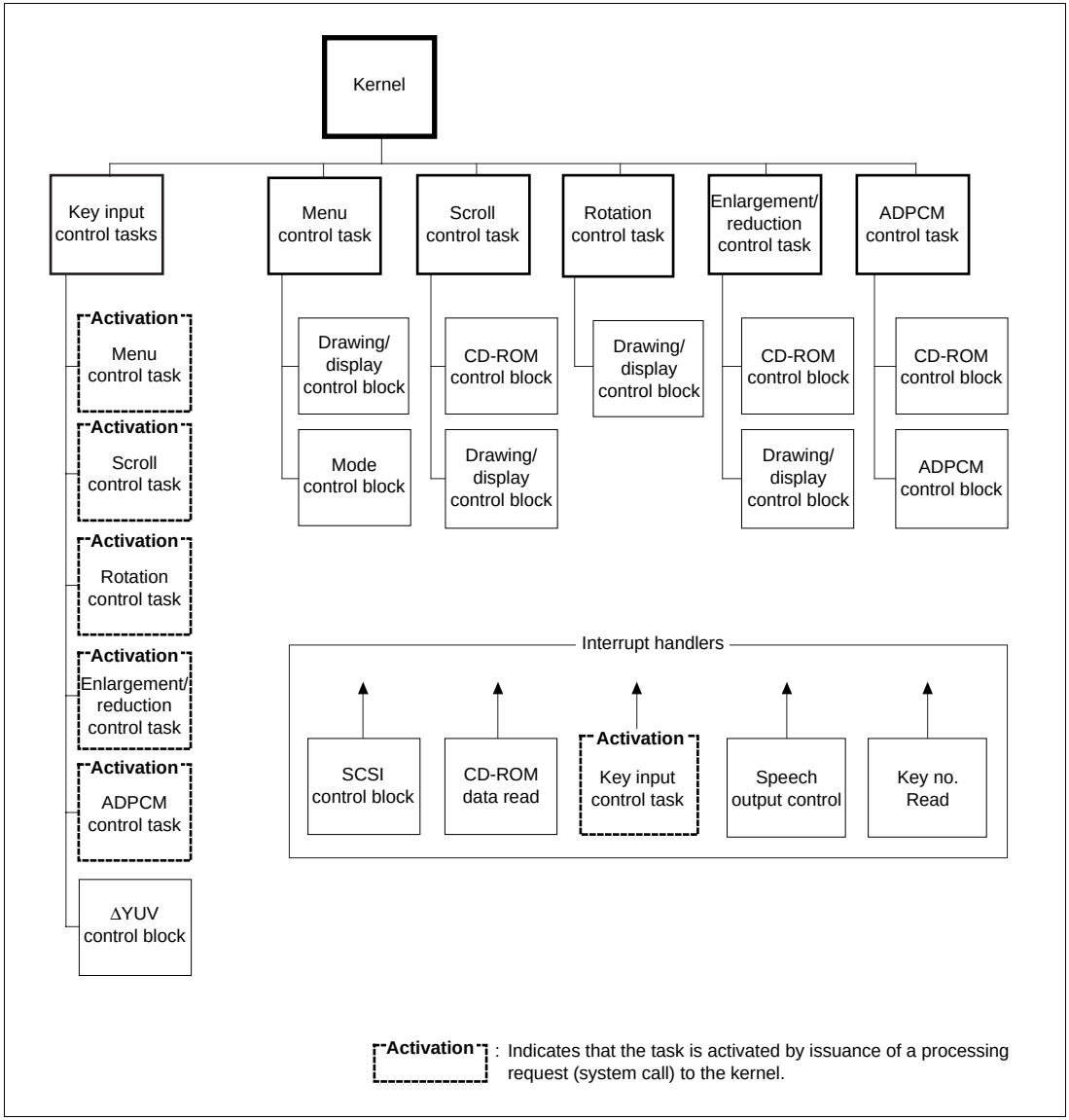


Figure 2.3 Task and Interrupt Handler Configuration

2.4 Task Functions

Table 2.2 summarizes the functions of the tasks and interrupt handlers recorded in the kernel by the NAV-DS4.

Table 2.2 Summary of Functions (1/3)

Task Name	Function
Key input control	Issues a processing request (system call) to the kernel according to the key input, activating a task. The meaning of the keys depends on the key input mode. 1. In map mode (normal mode) Performs scroll control task activation by means of the up/down/left/right arrow keys, rotation control task activation by means of the rotate keys, enlargement/reduction control task activation by means of the Wide Area and Detail keys, and menu control task activation by means of the Menu key. 2. In menu operation mode Selects a menu display item by means of the up/down arrow keys, and activated the task corresponding to the item. 3. In ADPCM mode Performs activation of ADPCM control tasks corresponding to the up/down/left/right arrow keys, rotate keys, Wide Area and Detail keys, and Enter and Menu keys.
Menu selection control	Draws the menu screen, and sets the menu operation mode, ADPCM demonstration mode, or speech synthesis demonstration mode from map mode according to the menu display items
Scroll control	Reads map data from the CD-ROM, creates a display list, and draws a map in the Q2's multi-valued source area. In scroll movement processing, drawing is performed while updating coordinate locations from the multi-valued source area to the display area at each Q2 vertical sync signal.
Rotation control	Performs coordinate conversion of map data by means of affine transformation processing, creates a display list, and draws in the display area with the Q2.
Enlargement/ reduction control	Reads wide-area or detailed map data from the CD-ROM, creates a display list, and draws in the display area with the Q2.
ADPCM control	Reads ADPCM data from the CD-ROM, and performs data expansion processing.

Section 3 NAV-DS4 Hardware

3.1 Hardware Configuration

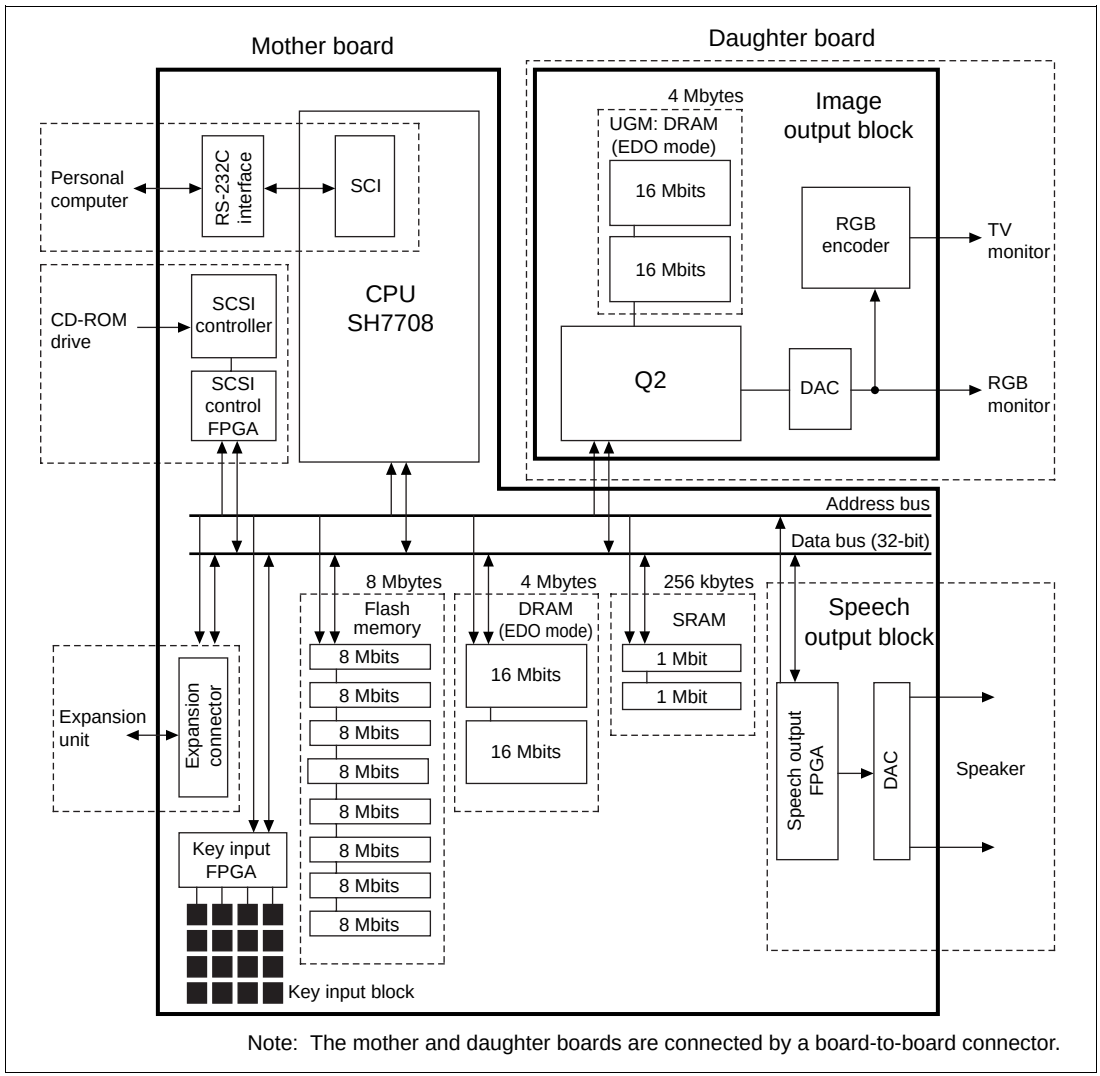
The NAV-DS4 mother board consists of an SH7708 32-bit RISC microcomputer, various kinds of memory (an HM51W18165AJ-6 2-Mbyte DRAM, HN29WB800T-8 8-Mbyte flash memory, and HN67W1664-JP-12 256-kbyte static RAM), an HD151015 level shifter, Hitachi HD74LVC Series CMOS logic semiconductor devices, an RS-232C control IC, SCSI control IC, D/A converter, and three FPGAs (field programmable gate arrays) for key input control, SCSI control, and speech control. The daughter board comprises an HD64411F (Q2), HM5118165ATT-7 2-Mbyte DRAM, and HD153510 F50 (DAC) Hitachi semiconductor devices, and an RGB encoder. Tables 3.1 and 3.2 list the functions of the LSIs mounted on the NAV-DS4's mother board and daughter board, and figure 3.1 shows the hardware configuration.

Table 3.1 Functions of LSIs Mounted on Mother Board

Mounted LSI	Device Function
HD6417708F60A (SH7708)	32-bit RISC microcomputer
HM51W18165AJ-6	16Mbit-EDO-DRAM
HM67W1664-JP-12	1Mbit-SRAM
HN29WB800T-8	8Mbit-FLASH MEMORY
HD151015	Level shifter
HD74LVC244A	Unidirectional level shifter
HD74LVC245A	Bidirectional level shifter
HD74LVC08	AND gate
HD74LVC00	NAND gate
HD74LVC32	OR gate
HD74LVC04	Inverter (NOT)
HD74LVC14	Schmitt trigger inverter
EPF8282ATC100-3	Key input control (FPGA)
EPF8452ATC100-3	Speech output (FPGA)
EPM7032LC44-6	SCSI control (FPGA)
SYM53CF96-2	SCSI controller
µPD6376GS	DAC
MAX233ACWP	RS-232C controller
LTI086CT-3.3	DD conversion LSI
LTI086CT-5	DD conversion LSI

Table 3.2 Functions of LSIs Mounted on Daughter Board

Mounted LSI	Device Function
HD64411F (Q2)	Quick 2D Graphics Renderer
HM5118165ATT-7	16Mbit-EDO-DRAM
HD153510F50	8bit-3chDAC
HD74LS04FP	Inverter (NOT)
CXA1645	RGB encoder



Note: The mother and daughter boards are connected by a board-to-board connector.

Figure 3.1 Hardware Configuration

3.2 Operation of Mother Board and Daughter Board

Mother board operations are as follows:

1. The mother board is controlled by the SH7708.
2. Controls the Q2 on the daughter board.
3. Controls the external CD-ROM drive connected via a SCSI interface.
4. Controls the 16 keys.
5. Outputs 16-bit stereo speech data.
6. When a PC is connected to the SCI connector, performs serial data communication with the PC.

Daughter board operations are as follows:

1. Controls drawing processing and display processing by the Q2.
2. Outputs images to the TV monitor and RGB monitor.

3.3 SH7708 Operating Conditions

(1) Operating Clock: In the NAV-DS4, a 30 MHz crystal oscillator is used for the SH7708's external input clock. The clock operating mode is set to mode 0 by external switching of the mode pins (MD0, MD1, and MD2). The frequency multiplication ratio of the SH7708's on-chip PLL circuit is set to ×2, and the internal clock and peripheral clock division ratios are set to ×1 and ×1/2, respectively, in the frequency control register (FRQCR), so that the SH7708's internal clock (Iø) is 60 MHz and its peripheral clock (Pø) is 30 MHz. The SH7708 clock operating mode pin settings and corresponding operations used in the NAV-DS4 are shown in table 3.3, and the frequency control register (FRQCR) settings and corresponding operations in figure 3.2.

Table 3.3 Clock Operating Mode Pin Settings and Operations

	Pin Names			Clock Input/ Output				
Clock Operating Mode	**MD2**	**MD1**	**MD0**	**Supply Source/ Output**	**PLL Circuit 1 On/Off**	**Divider 1 Input**	**CKI0 Frequency**	**Internal Clock**
Mode 0	0	0	0	EXTAL/ CKIO	ON	PLL circuit 1 output	EXTAL	Frequency resulting from applying PLL circuit 1 frequency multiplication ratio and divider 1 division ratio to CKI0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKOEN	PLLEN	PSTBY	STC1	STC0	IFC1	IFC0	PFC1	PFC0
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Set value	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

- CKOEN = 1 : Clock is output from CKI0 pin.
- PLLEN = 0 : PLL circuit 1 is not used. (As clock operating mode 0 is used, this bit is invalid.)
- PSTBY = 0 : PLL standby is not performed. (As clock operating mode 0 is used, this bit is invalid.)
- STC1, 0 = 01 : PLL circuit 1 frequency multiplication ratio is ×2.
- IFC1, 0 = 00 : Internal clock frequency division ratio is ×1.
- PFC1, 0 = 01 : Peripheral clock frequency division ratio is ×1/2.

Figure 3.2 Frequency Control Register (FRQCR) Settings and Operations

(2) Pin Functions: The SH7708 has a number of multiplex pins. The multiplex pins and pin functions used by the NAV-DS4 are listed in table 3.4.

Table 3.4 Multiplex Pins and Pin Functions

Pin No.	Pin Name			Function	
				On Reset (in)	On Recovery after Reset (in) (After elapse of 50 [ns])
5	D23	PORT7		Data bus	Data bus
8	D22	PORT6		Data bus	Data bus
9	D21	PORT5		Data bus	Data bus
10	D20	PORT4		Data bus	Data bus
11	D19	PORT3		Data bus	Data bus
12	D18	PORT2		Data bus	Data bus
13	D17	PORT1		Data bus	Data bus
14	D16	PORT0		Data bus	Data bus
84	MD2	RXD		Operating mode (clock operating mode setting)	Serial data reception and break state detection
85	MD1	TXD		Operating mode (clock operating mode setting)	Serial data transmission and break state sending
86	MD0	SCK		Operating mode (clock operating mode setting)	Serial clock input/output and I/O port
103	MD4	_CE2B		Operating mode (area 0 bus width setting)	Operating mode (area 0 bus width setting)
104	MD3	_CE2A		Operating mode (area 0 bus width setting)	Operating mode (area 0 bus width setting)
108	_CS6	_CE1B		Chip select 6	Chip select 6
109	_CS5	_CE1A		Chip select 5	Chip select 5
117	_WE3	DQMUU	_ICIOWR	Write strobe signal for D31–D24	Write strobe signal for D31–D24
118	_WE2	DQMUL	_ICIORD	Write strobe signal for D23–D16	Write strobe signal for D23–D16
119	_CASHH	_CAS2H		CAS signal for D31–D24	CAS signal for D31–D24
120	_CASHL	_CAS2L		CAS signal for D23–D16	CAS signal for D23–D16
123	_WE1	DQMLU		Write strobe signal for D15–D8	Write strobe signal for D15–D8
124	_WE0	DQMLL		Write strobe signal for D7–D0	Write strobe signal for D7–D0
126	_CASLL	_CAS	_OE	CAS signal for D7–D0	CAS signal for D7–D0
129	_RAS	_CE		RAS signal	RAS signal
130	MD5	_RAS2		Operating mode (entire-space endian setting)	Operating mode (entire-space endian setting)

(3) Interrupt Handling: The NAV-DS4 uses IRL interrupts. The key input FPGA has an interrupt priority encoder function, and inputs levels to pins _IRL3–_IRL0 according to the _INRQ15–_INRQ0 pin priority levels shown in table 3.5. Figure 3.3 shows the interrupt priority encoder peripheral block diagram.

Table 3.5 _INRQ15–_INRQ0 Pins and Interrupt Priority Order

Pin	Interrupt Priority Level	_IRL3	_IRL2	_IRL1	_IRL0	Interrupt Priority Order
_INRQ15	15	0	0	0	0	High
_INRQ14	14	0	0	0	1	
_INRQ13	13	0	0	1	0	
_INRQ12	12	0	0	1	1	
_INRQ11	11	0	1	0	0	
_INRQ10	10	0	1	0	1	
_INRQ9	9	0	1	1	0	
_INRQ8	8	0	1	1	1	
_INRQ7	7	1	0	0	0	
_INRQ6	6	1	0	0	1	
_INRQ5	5	1	0	1	0	
_INRQ4	4	1	0	1	1	
_INRQ3	3	1	1	0	0	
_INRQ2	2	1	1	0	1	
_INRQ1	1	1	1	1	0	Low

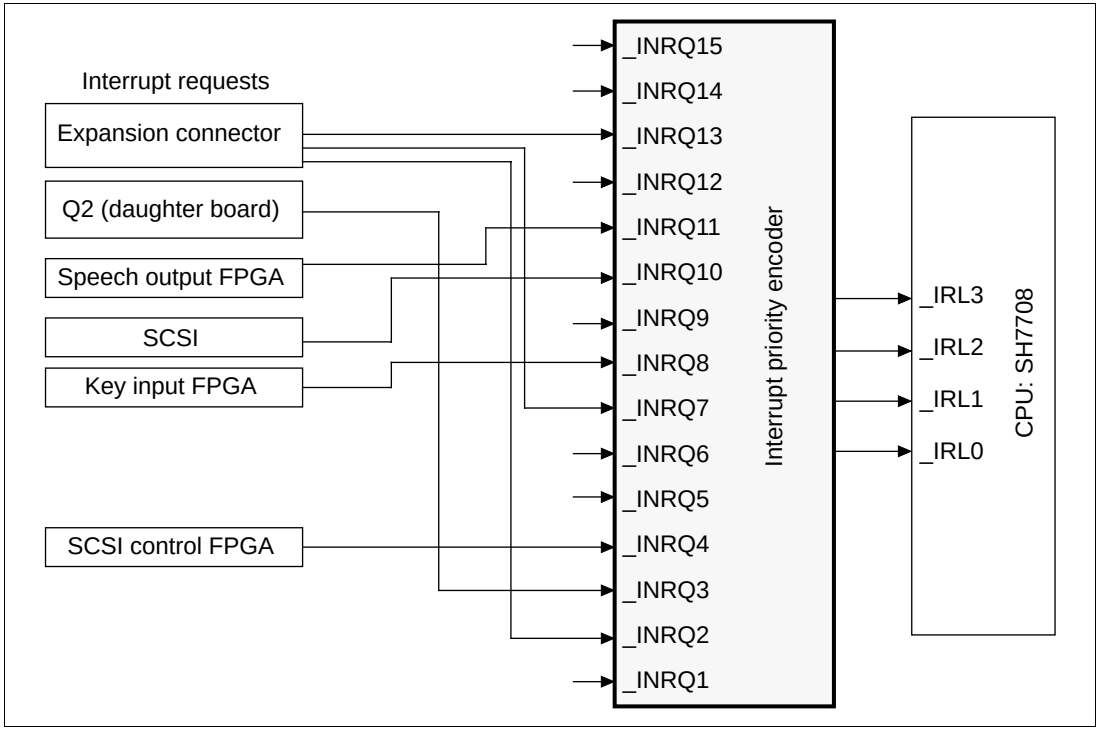


Figure 3.3 Interrupt Priority Encoder Peripheral Block Diagram

(4) Address Map: In the SH7708, the physical address space can be managed as seven separate areas, numbered 0 to 6, each of up to 64 Mbytes in size. The address map of the NAV-DS4 is shown in figure 3.4. The function and bus cycle state of each area are set with the bus control register (BCR1). Bus control register (BCR1) settings and corresponding operations are shown in figure 3.5.

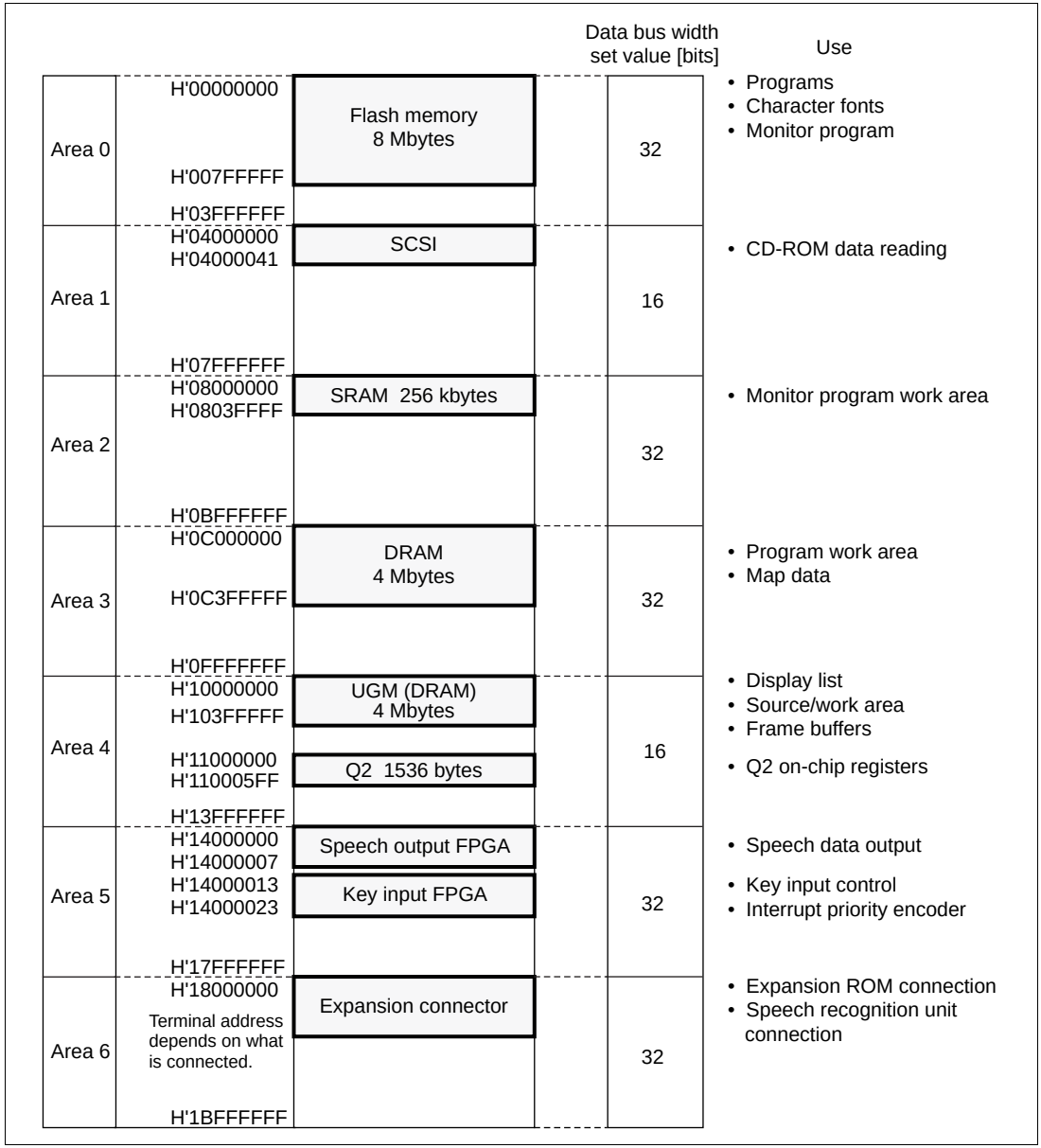


Figure 3.4 NAV-DS4 Address Map

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	HIZ CNT	ENDI AN	A0 BST1	A0 BST0	A5 BST1	A5 BST0	A6 BST1	A6 BST0	DRAM TP2	DRAM TP1	DRAM TP0	A5 PCM	A6 PCM
Initial value	0	0	0	0	0/1	0	0	0	0	0	0	0	0	0	0	0
Set value	0	0	0	0	—	0	0	0	0	0	0	1	0	0	0	0

- HIZCNT = 0 : _RAS and _CAS signals become high-impedance in standby mode and when bus is released.
- A0BST1, 0 = 00 : Area 0 is accessed as ordinary memory.
- A5BST1, 0 = 00 : Area 5 is accessed as ordinary memory.
- A6BST1, 0 = 00 : Area 6 is accessed as ordinary memory.
- DRAMTP2, 1, 0 = 100 : Area 2 is accessed as ordinary memory, and area 3 as DRAM.
- A5PCM = 0 : Area 5 is accessed as ordinary memory.
- A6PCM = 0 : Area 6 is accessed as ordinary memory.

Figure 3.5 Bus Control Register (BCR1) Settings and Operations

(5) Memory Bus Width and Data Format: The SH7708's memory bus width is set for each space. Flash memory is connected to area 0, and mode pins MD3 and MD4 are set by an external switch to give a 32-bit bus width. The MD5 mode pin is set by an external switch to designate a big-endian data format. Mode pin settings and the corresponding operations are shown in table 3.6.

The bus width of areas 1 to 6 is set in bus control register 2 (BCR2). Bus control register 2 (BCR2) settings and the corresponding operations are shown in table 3.6. However, the DRAM interface bus width is set in the individual memory control register (MCR). See (7) below for details of this register.

Table 3.6 Mode Pin Settings and States

Pin Name			Description	
MD5	**MD4**	**MD3**	**Endian**	**Area 0 Bus Width**
0	1	1	Big	32 bits

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A6 SZ1	A6 SZ0	A5 SZ1	A5 SZ0	A4 SZ1	A4 SZ0	A3 SZ1	A3 SZ0	A2 SZ1	A2 SZ0	A1 SZ1	A1 SZ0	—	PORT EN
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
Set value	0	0	1	1	1	1	1	0	1	1	1	1	1	0	0	0

- A6SZ1, 0 = 11 : Area 6 bus width is set to 32 bits.
- A5SZ1, 0 = 11 : Area 5 bus width is set to 32 bits.
- A4SZ1, 0 = 10 : Area 4 bus width is set to 16 bits.
- A3SZ1, 0 = 11 : Area 3 bus width is set to 32 bits.
- A2SZ1, 0 = 11 : Area 2 bus width is set to 32 bits.
- A1SZ1, 0 = 10 : Area 1 bus width is set to 16 bits.
- PORTEN = 0 : D23–D16 are not used as port pins.

Figure 3.6 Bus Control Register 2 (BCR2) Settings and Operations

(6) Wait Control: With some peripheral devices, data bus drive is not immediately switched off when the read signal from the SH7708 is switched off. Therefore, when consecutive accesses that span a number of areas are performed, or when a switch is made to write access immediately after read access, for example, there is a possibility of a data collision on the data bus. For this reason, wait control register 1 (WCR1) is set to provide automatic idle cycle insertion. Wait control register 1 (WCR1) settings and the corresponding operations are shown in figure 3.7.

Wait state insertion cycle specifications for each area are made in wait control register 2 (WCR2). The data access pitch specification for burst access is also made in this register. The flash memory (HN29WB800T-8) connected to area 0, can be accessed in four cycles with two wait states inserted. Wait control register 2 (WCR2) settings and the corresponding operations are shown in figure 3.8.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A6 IW1	A6 IW0	A5 IW1	A5 IW0	A4 IW1	A4 IW0	A3 IW1	A3 IW0	A2 IW1	A2 IW0	A1 IW1	A1 IW0	A0 IW1	A0 IW0
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Set value	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1

When switching from one area to another, or when switching from read access to write access in the same area

- A6IW1, 0 = 01 : For area 6, one idle cycle is inserted.
- A5IW1, 0 = 01 : For area 5, one idle cycle is inserted.
- A4IW1, 0 = 01 : For area 4, one idle cycle is inserted.
- A3IW1, 0 = 01 : For area 3, one idle cycle is inserted.
- A2IW1, 0 = 01 : For area 2, one idle cycle is inserted.
- A1IW1, 0 = 01 : For area 1, one idle cycle is inserted.
- A0IW1, 0 = 01 : For area 0, one idle cycle is inserted.

Figure 3.7 Wait Control Register 1 (WCR1) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	A6 W2	A6 W1	A6 W0	A5 W2	A5 W1	A5 W0	A4 W2	A4 W1	A4 W0	A3 W1	A3 W0	A1–2 W1	A1–2 W0	A0 W2	A0 W1	A0 W0
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Set value	1	1	1	0	0	1	1	0	0	0	0	0	1	0	1	0

- A6W2, 1, 0 = 111 : Number of wait states inserted for area 6 = 10
- A5W2, 1, 0 = 001 : Number of wait states inserted for area 5 = 1
- A4W2, 1, 0 = 100 : Number of wait states inserted for area 4 = 4
- A3W1, 0 = 00 : DRAM _CAS assertion width = 1 state
- A1–2W1, 0 = 01 : Number of wait states inserted for areas 1 and 2 = 1
- A0W2, 1, 0 = 010 : Number of wait states inserted for area 0 = 2

Figure 3.8 Wait Control Register 2 (WCR2) Settings and Operations

(7) Memory Control: In the NAV-DS4, EDO mode 16-Mbit DRAM (HM51W18165AJ-6) is connected to area 3. DRAM access in EDO mode requires a maximum of six cycles, with Tr and Trw cycles inserted, and a minimum of two cycles when consecutive addresses are accessed (using burst access). CAS-before-RAS refreshing is used. The _RAS and _CAS timing, burst control, address multiplex specifications, and refresh control specifications are made in the individual memory control register (MCR). Individual memory control register (MCR) settings and the corresponding operations are shown in table 3.9.

The refresh period, presence or absence of interrupt generation, and the interrupt generation period, are specified in the refresh timer control/status register (RTCSR). The upper limit of the refresh timer counter (RTCNT) is set in the refresh timer constant register (RCTOR). Refresh timer control/status register (RTCSR) settings and the corresponding operations are shown in figure 3.10, and refresh timer constant register (RCTOR) settings and operations in figure 3.11.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCP1	TCP0	RCD1	RCD0	TRWL1	TRWL0	TRAS1	TRAS0	—	BE	SZ	AMX1	AMX0	RFSH	RMODE	EDO MODE
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Set value	0	1	0	1	0	0	0	1	0	1	1	1	0	1	0	1

Settings when DRAM is connected to area 3

- TPC1, 0 = 01 : Minimum number of cycles until _RAS is next asserted after being negated = 2
- RCD1, 0 = 01 : _RAS–_CAS assertion delay time = 2 cycles
- TRWL1, 0 = 00 : Not set
- TRAS1, 0 = 01 : _RAS assertion period in _CAS-before-_RAS refreshing = 3 cycles
- BE =1 : Burst access is performed
- SZ = 1 : Bus size is 32 bits.
- AMX1, 0 = 10 : Address multiplex setting = 10-bit column address product used
- RFSH = 1 : Refresh control specification = refresh performed
- RMODE = 0 : _CAS-before-_RAS refreshing is performed.
- EDOMODE = 1 : Set to EDO mode. (Data sampling timing for read cycle is CKI0 rise. _RAS signal negation timing is 1/2 machine cycle after CKI0.)

Figure 3.9 Individual Memory Control Register (MCR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CMF	CMIE	CKS2	CKS1	CKS0	OVF	OVIE	LMTS
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Set value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

- CMF = 0 : Status flag indicating that the refresh timer counter (RTCNT) and refresh time constant register (RTCOR) values match.
- CMIE = 0 : Interrupt requests by CMF are disabled.
- CKS2, 1, 0 = 001 : Selects refresh timer counter (RTCNT) input clock. (CKI0/4)
- OVF = 0 : Status flag indicating that the number of refresh requests indicated in the refresh count register (RFCR) has exceeded the number indicated by LMTS.
- OVIE = 0 : Interrupt requests by OVF are disabled.
- LMTS = 0 : Count limit value compared with the number of refresh requests indicated in the refresh count register (RFCR) (the count limit value is set to 1024).

Figure 3.10 Refresh Timer Control/Status Register (RTCSR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—								
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Set value	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1

- Sets the upper limit of the RTCNT counter. (Lower 8 bits)
- Calculation formula:

$$\text{RTCNT value} = \frac{\text{DRAM refresh period [s]}}{\text{refresh timer counter (RTCNT) period [s]}}$$

$$= \frac{\dfrac{16 \times 10^{-3}\ [\text{s}]}{1024\ [\text{cycles}]}}{\dfrac{1}{(\text{CKI0/4})\ [\text{cycles}]}} = \frac{16 \times 10^{-3}}{1024} \times \frac{30 \times 10^{6}}{4} = 117.1875 \approx \text{H'75}$$

Figure 3.11 Refresh Time Constant Register (RTCOR) Setting and Calculation Formula

(8) Cache Memory: The SH7708 has on-chip cache memory. Use of 8-kbyte cache (normal mode) or 4-kbyte cache and 4-kbyte RAM (RAM mode) can be selected. A mixed instructions/data type 4-way set-associative configuration (normal mode) or 2-way set-associative configuration (RAM mode) can be selected. With the NAV-DS4, normal mode, using 8-kbyte cache memory, is set. The operating mode is set in the cache control register (CCR). Cache control register (CCR) settings and the corresponding operations are shown in table 3.12.

Bit:	31		5	4	3	2	1	0
	—	—	RA	0	CF	—	WT	CE
Initial value	0	0	0	0	0	0	0	0
Set value	0	0	0	0	1	0	0	1

- RA = 0 : Normal mode (8-kbyte cache)
- CF = 1 : V, U, and LRU bits of all cache entries are cleared to 0.
- WT = 0 : Write-back mode
- CE = 1 : Cache is used.

Figure 3.12 Cache Control Register (CCR) Settings and Operations

3.4 Q2 Operating Conditions

(1) Operating Clocks: There are two Q2 clocks, the drawing clock (CLK0) and the display clock (CLK1). The SH7708's CKI0 (30 MHz) output is input via a level shifter as the drawing clock (CLK0). For the clock operating mode, the mode pins (Mode0, Mode1, are Mode2) are set to mode 3 by means of an external switch. The Q2 clock operating mode pin settings used by the NAV-DS4, and the corresponding operations, are shown in table 3.3.

The Q2 display clock (CLK1) is provided by a 14.318 MHz crystal oscillator. A display dot clock of 7.15 MHz (1/2 the CLK1 clock frequency) provided by the Q2's on-chip frequency divider is set by means of the Q2's display mode register (DSMR). See (2) below for details of this register.

Table 3.3 Clock Operating Mode Pin Settings and States

Clock Operating Mode	Pin Names			Operation	Multiplication On/Off	Internal Clock
	MD2	MD1	MD0			
Mode 3	0	1	1	Normal operating state	Off	Same as external input clock

(2) Interface Control: Overall Q2 control is performed by settings in a group of registers called the interface control registers (FRQCR). These registers are as follows:

- System control register (SYSR): Sets Q2 system operation.
- Status register (SR): Reads the Q2's internal status externally (read-only).
- Status register clear register (SRCR): Clears the corresponding status register contents.
- Interrupt enable register (IER): Sets the conditions for interrupt generation from the Q2 to the CPU.
- Memory mode register (MEMR): Sets the size and number of UGM memories.
- Display mode register (DSMR): Settings related to Q2 display operations.
- Rendering mode register (REMR): Settings related to Q2 drawing operations.
- Input data conversion mode register (IEMR): Settings related to format conversion of input data from the CPU.

Interface control register (FRQCR) settings used by the NAV-DS4, and the corresponding operations, are shown in figures 3.13 to 3.18.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRES	DRES	DEN	—	—	—	DC	RS	DBM		DMA		CCM			
Set value	0	0	1	0	0	0	0 or 1	0 or 1	0 or 1	1 or 0	0	0	0	0	0	0

- SRES = 0 : Command execution is enabled.
- DRES = 0 : Display synchronization operation is started. The values stored in the UGM are DEN = 1 output from the DD pin as display data.
- DC = 0 : Display frame buffer switching is not performed in manual display change mode.
  = 1 : Display frame buffer switching is performed in manual display change mode.
- RS = 0 : Rendering is not started.
  = 1 : Rendering is started.
- DBM = 01 : Auto rendering mode is set.
  = 10 : Manual display change mode is set.
- DMA = 00 : Normal mode is set.
- CCM = 0000 : Normal mode is set.

Note: The values of DC, RS, and DBM are changed according to the processing executed.

Figure 3.13 System Control Register (SYSR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE	FRE	DME	CEE	VBE	TRE	CSE	—	—	—	—	—	—	—	—	—
Set value	0	0	0	0	0 or 1	0	0	0	0	0	0	0	0	0	0	0

- TVE = 0 : TV synchronization error flag interrupt is not enabled.
- FRE = 0 : Frame flag interrupt is not enabled.
- DME = 0 : DMA flag interrupt is not enabled.
- CEE = 0 : Command error flag interrupt is not enabled.
- VBE = 0 : Vertical blanking flag interrupt is not enabled.
  = 1 : Vertical blanking flag interrupt is enabled.
- TRE = 0 : Trap flag interrupt is not enabled.
- CSE = 0 : Command suspend flag interrupt is not enabled.

Note: The value of VBE is changed according to the processing executed.

Figure 3.14 Interrupt Enable Register (IER) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MES			MEA		—	—
Set value	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0

- MES = 010 : Two 16-Mbit DRAMs are used for the UGM.
- MEA = 01 : Number of row address bits = 10

Figure 3.15 Memory Mode Register (MEMR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	YCM	DOT	TVM		SCM		REF			
Set value	0	0	0	0	0	0	0	1	0	0	0 or 1	0	0	1	0	1

- YCM = 0 : RGB/YCrCb conversion is not performed.
- DOT = 1 : 1/2 the frequency of the clock input from the CLK1 pin is used as the display dot clock.
- TVM = 0 : Sets master mode in which HSYNC, VSYNC, and ODDF are output.
- SCM = 00 : Display output is set to non-interlace.
  = 10 : Interlace sync set for video monitor output.
- REF = 0101 : Refresh timing set to 5 cycles.

Note: The value of SCM is changed according to the processing executed.

Figure 3.16 Display Mode Register (DSMR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MWX	—	—	—	—	—	GBM
Set value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0 or 1

- MWX = 1 : The UGM X-direction logical coordinate space is set to 1024 pixels.
- GBM = 0 : Rendering data bit configuration is set to 8 bits/pixel (in map data processing).
  = 1 : Rendering data bit configuration is set to 16 bits/pixel (in natural image data processing).

Note: The value of GBM is changed according to the processing executed.

Figure 3.17 Rendering Mode Register (REMR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	YUV	
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 or 1	0

- YUV = 00 : Sets normal mode in which data conversion is not performed.
  = 10 : Sets mode in which ΔYUV–RGB data conversion is performed.
  (In ΔYUV data processing)

Note: The value of YUV is changed according to the processing executed.

Figure 3.18 Input Data Conversion Mode Register (IEMR) Settings and Operations

(3) Memory Control: The Q2 uses a UGM (unified graphics memory) architecture, in which data of different formats (such as frame buffer area data and font pattern area data) is stored and managed in the same memory. The configuration of the UGM connected to the Q2 is determined by settings in a group of registers called the memory control registers (MECR). These registers are as follows:

- Display size register (DSR): Sets the display screen size.
- Display start address register (DSAR): Sets the frame buffer area.
- Display list start address register (DLSAR): Sets the display list area.
- Multi-valued source area start address register (SSAR): Sets the multi-valued source area.
- Work area start address register (WSAR): Sets the work area.
- DMA transfer start address register (DMASR): Sets the transfer destination UGM address in DMA transfer.
- DMA transfer word count register (DMAWR): Sets the number of words to be transferred in DMA transfer.

Since DMA transfer is not used by the NAV-DS4, no DMA transfer start address register (DMASR) or DMA transfer word count register (DMAWR) settings are made. Memory control register (MECR) settings, and the corresponding operations, are shown in figures 3.19 to 3.23. UGM memory maps are shown in figure 3.24, and 3.25.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DSX									
Set value	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DSY								
Set value	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1

- DSX = 0100111111 : The number of display screen dots in the horizontal direction (X direction) is set to 320.
- DSY = 011101111 : The number of display screen dots in the vertical direction (Y direction) is set to 240.

Figure 3.19 Display Size Register (DSR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DSA0						
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DSA1						
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

- DSA0 = 0000000 : The frame buffer 0 start address is set to UGM address 0h.
- DSA1 = 0000100 : The frame buffer 1 start address is set to UGM address 40000h (in 8-bit/pixel mode).

Note: The values of the frame buffer 0 and 1 start addresses are changed according to the processing executed.

Figure 3.20 Display Start Address Register (DSAR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DLSAH						
Set value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DLSAL											—	—	—	—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- DLSAH = 0001001 : Bits A22 to A16 of the display list start address.
- DLSAL = 00000000000 : Bits A15 to A5 of the display list start address. The display list start address is set to UGM address 90000h (in initialization).

Note: The value of the display list start address is changed according to the processing executed.

Figure 3.21 Display List Start Address Register (DLSAR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	SSAH						—
Set value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

- SSAH = 001000 : The multi-valued source area start address is set to UGM address 100000h (in 8-bit/pixel data processing).
  = 000000 : The multi-valued source area start address is set to UGM address 0h (in natural image data processing).

Note: The value of SSAH is changed according to the processing executed.

Figure 3.22 Multi-Valued Source Area Start Address Register (SSAR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	WSAH						
Set value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

- WSAH = 0001000 : The work area start address is set to UGM address 80000h (in 8-bit/pixel data processing).
  = 0011000 : The work area start address is set to UGM address 180000h (in natural image data processing).

Note: The value of WSAH is changed according to the processing executed.

Figure 3.23 Work Area Start Address Register (WSAR) Settings and Operations

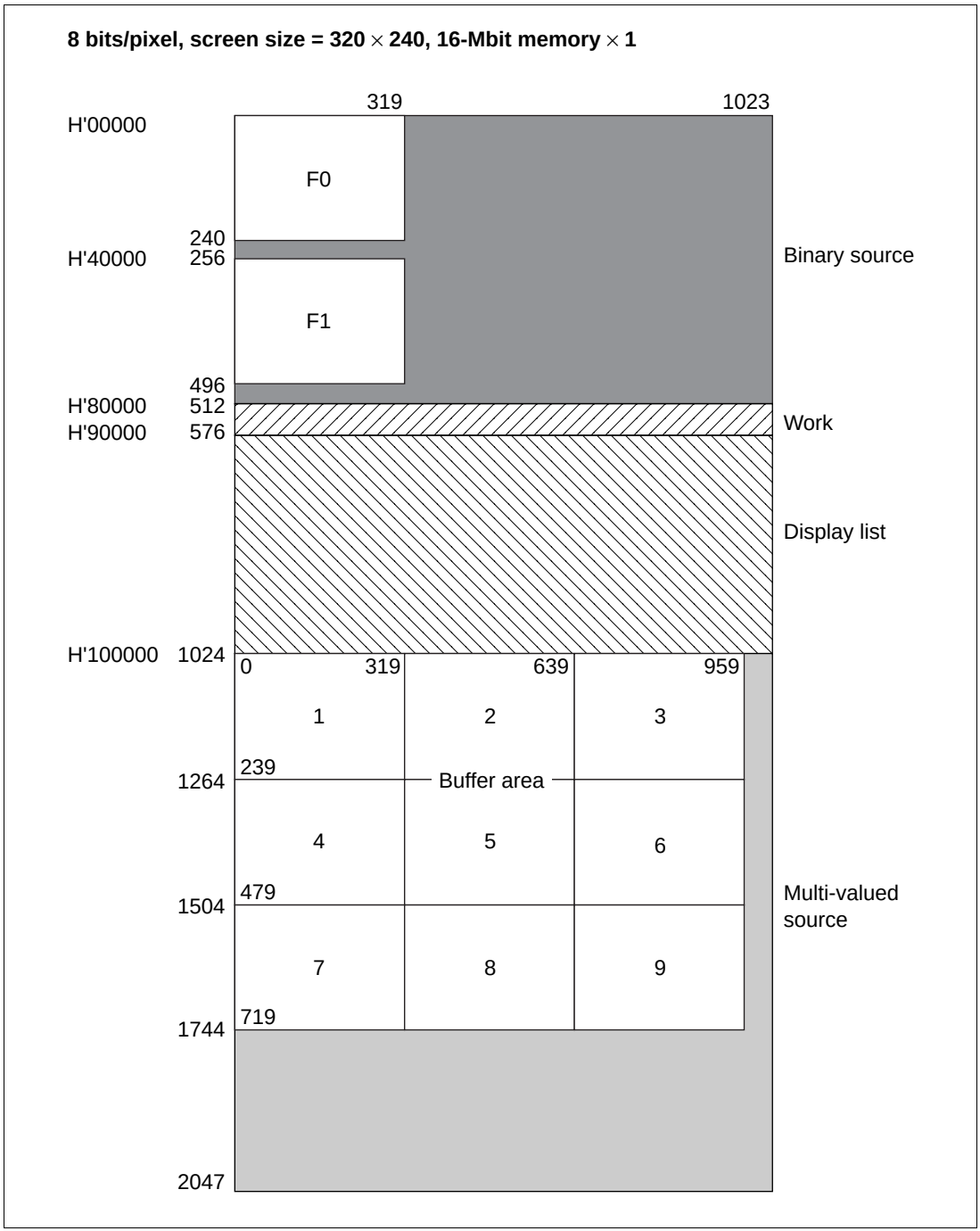


Figure 3.24 UGM Memory Map (8-Bit/Pixel Mode)

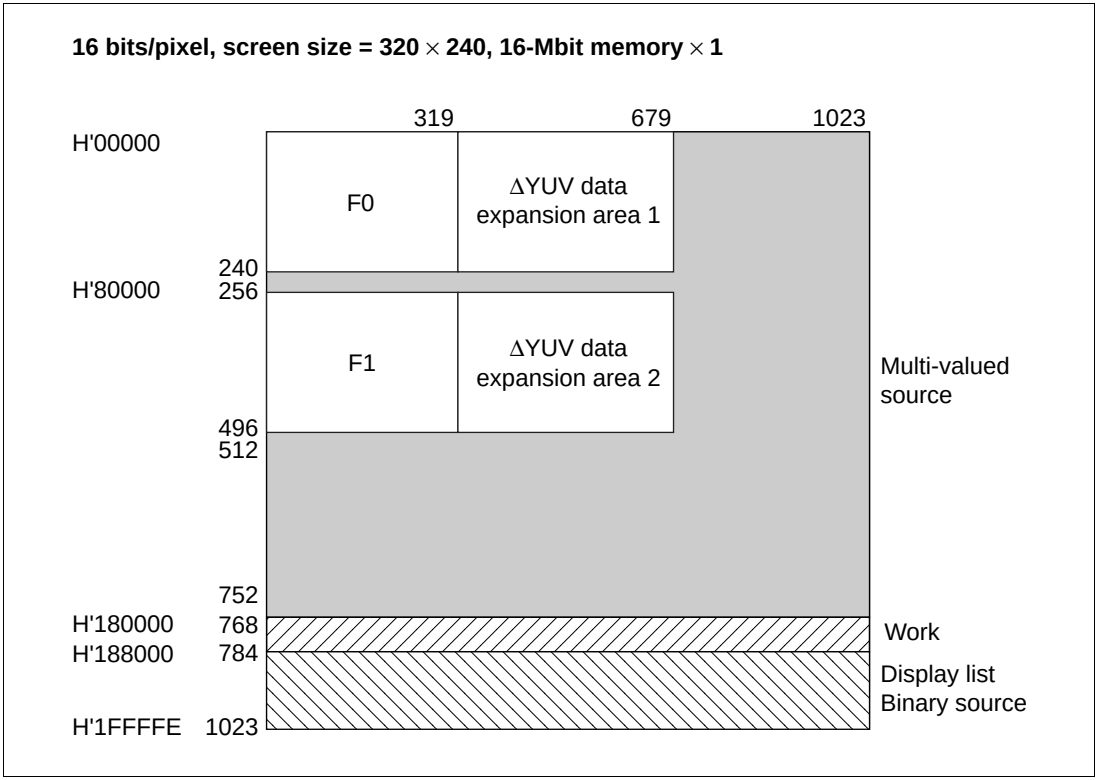


Figure 3.25 UGM Memory Map (16-Bit/Pixel Mode)

(4) Display Control: The Q2 performs double-buffering control that switches alternately between the display area and drawing area located in the UGM, making it possible to alternate between high-speed drawing processing and display processing. Q2-controlled display timing settings are made in a group of registers called the display control registers (DSCR). These registers are as follows:

- Display window register (DSWR): Sets display screen horizontal and vertical output timing.
- Horizontal synchronization pulse width register (HSWR): Sets the low-level pulse width of the horizontal sync signal.
- Horizontal scan cycle register (HCR): Sets the horizontal scan cycle.
- Vertical synchronization position register (VSPR): Sets the start position of the vertical sync signal.
- Vertical scan cycle register (VCR): Sets the vertical scan cycle.
- Display off output register (DOOR): Sets the display data to be output when the display is off.
- Color detection register (CDER): Detects display color data.

Display control register (DSCR) settings used by the NAV-DS4, and the corresponding operations, are shown in figures 3.26 to 3.31.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	HDS									
Set value	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	HDE									
Set value	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VDS									
Set value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VDE									
Set value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

- HDS = 0001011110 : The horizontal display start position is set to 5eh.
- HDE = 0110011110 : The horizontal display end position is set to 19eh.
- VDS = 0000010000 : The vertical display start position is set to 10h.
- VDE = 0100000000 : The vertical display end position is set to 100h.

Note: HDS and HDE are set in dot clock units, and VDS and VDE in raster line units.

Figure 3.26 Display Window Register (DSWR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	HSW						
Set value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

- HSW = 0011111 : The low-level pulse width of the horizontal sync signal is set to 1fh.

Note: HSW is set in dot clock units.

Figure 3.27 Horizontal Synchronization Pulse Width Register (HSWR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	HC										
Set value	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	0

• HC = 111000110 : One horizontal scan cycle, including the horizontal retrace line interval, is set to 1c6h.

Note: HC is set in dot clock units.

Figure 3.28 Horizontal Scan Cycle Register (HCR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VSP									
Set value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

• VSP = 0100000011: The start position of the vertical sync signal is set to 103h.

Note: VSP is set in dot clock units.

Figure 3.29 Vertical Synchronization Position Register (VSPR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VC									
Set value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

• VC = 100000110 : One vertical scan cycle, including the vertical retrace line interval, is set to 106h.

Note: VC is set in raster line units.

Figure 3.30 Vertical Scan Cycle Register (VCR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DOR						—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOG						—	—	DOB						—	—
Set value	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0

- DOR = 000000 : The R component of the data output in the display-off state is set to 0h.
- DOG = 000000 : The G component of the data output in the display-off state is set to 0h.
- DOB = 011111 : The B component of the data output in the display-off state is set to 1fh.

Figure 3.31 Display Off Output Register (DOOR) Settings and Operations

(5) Input Data Control: The NAV-DS4 uses the YUV–RGB data conversion function of the Q2 to implement high-speed natural image drawing. To control YUV data conversion by the Q2, settings are made in a group of registers called the input data control registers (IDCR). These registers are as follows:

- Image data transfer start address register (ISAR): Sets the transfer destination address for image data transfer.
- Image data size register (IDSR): Sets the image data size.
- Image data entry register (HCR): Used to input the image data to be converted,

Input data control register (IDCR) settings used by the NAV-DS4, and the corresponding operations, are shown in figures 3.32 to 3.34.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	ISAH						
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ISAL															—
Set value	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

- ISAH = 0000000 : Image data transfer destination physical address bits A22 to A16 are set to 0h.
- ISAL = 001010000000000 : Image data transfer destination physical address bits A15 to A0 are set to 2800h.

Note: The values of ISAH and ISAL are changed according to the processing executed.

Figure 3.32 Image Data Transfer Start Address Register (ISAR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	IDSX										
Set value	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IDSY									
Set value	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0

- IDSX = 00101101000 : The image data X-direction size is set to 360 dots.
- IDSY = 1001000000 : The image data Y-direction size is set to 240 dots.

Note: IDSX and IDSY are set in pixel units.

Figure 3.33 Image Data Size Register (IDSR) Settings and Operations

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDE															
Set value																

- IDE : Used to input image data.

Figure 3.34 Image Data Entry Register (IDER) Setting and Operation

(6) Color Palette: The NAV-DS4 uses the Q2's on-chip color palette for map drawing in 8-bit/pixel mode, enabling simultaneous display of 256 colors out of a total of 260,000. Color palette settings are made using a group of 256 registers called color palette registers (CP000–CP255). Colors are set using 6 bits for each of R, G, and B. Color palette register values are cleared when drawing is performed after changing from 8-bit/pixel mode to 16-bit/pixel mode, so the settings must be made again when returning to 8-bit/pixel mode. Color palette register (CP000–CP255) settings used by the NAV-DS4 are shown in figure 3.35.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	R000						—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	G000						—	—	B000						—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

⋮

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	R255						—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	G255						—	—	B255						—	—
Set value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: Due to space limitations, it is not possible to show all the color palette set values.

Figure 3.35 Color Palette Register (CP000–CP255) Settings

3.5 Interfaces between SH7708 and Peripherals

(1) Interface to 5 V Operation Units: The NAV-DS4 includes both 5 V and 3.3 V operation units. As the SH7708 operates at 3.3 V, it is connected directly to the 3.3 V operation units, but is connected to the 5 V operation units via a level shifter. A decoder using TLL circuitry is provided to prevent signal contact between the 3.3 V and 5 V operation units (bidirectional bus only). Figure 3.36 shows a block diagram of the interface between the SH7708 and the 5 V operation units.

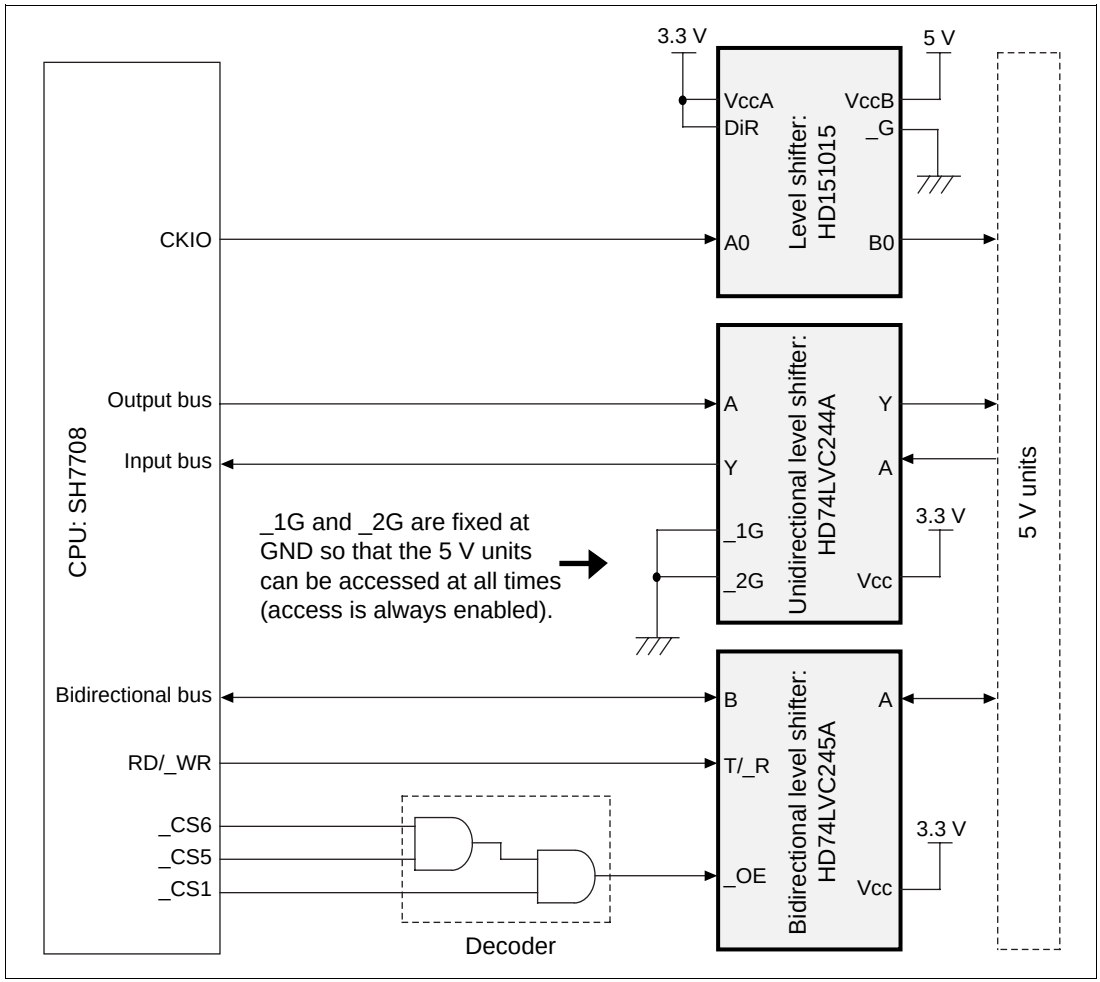


Figure 3.36 Block Diagram of Interface to 5 V Operation Units

(2) Flash Memory Interface: The NAV-DS4 is equipped with 8 Mbytes of flash memory (HN29WB800T-8), used in byte mode, to hold programs and character fonts. Figure 3.37 shows a block diagram of the interface between the SH7708 and the flash memory. A TTL decoder is provided to allow separate access to the upper 4 Mbytes and lower 4 Mbytes of the 8-Mbyte memory. Figure 3.38 shows a logic diagram of the flash memory decoder, and table 3.8 gives the corresponding truth table.

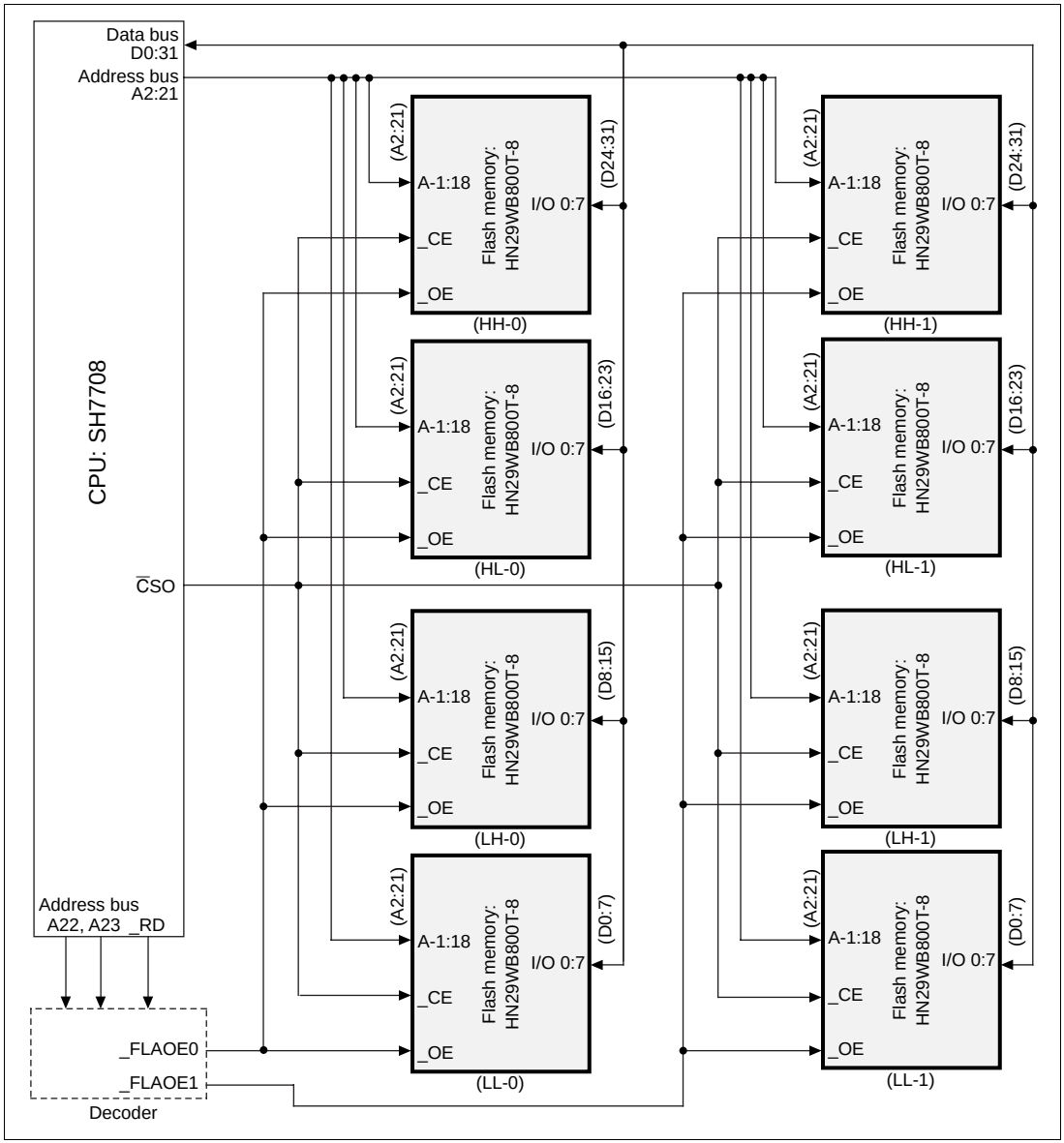


Figure 3.37 Block Diagram of Flash Memory Interface

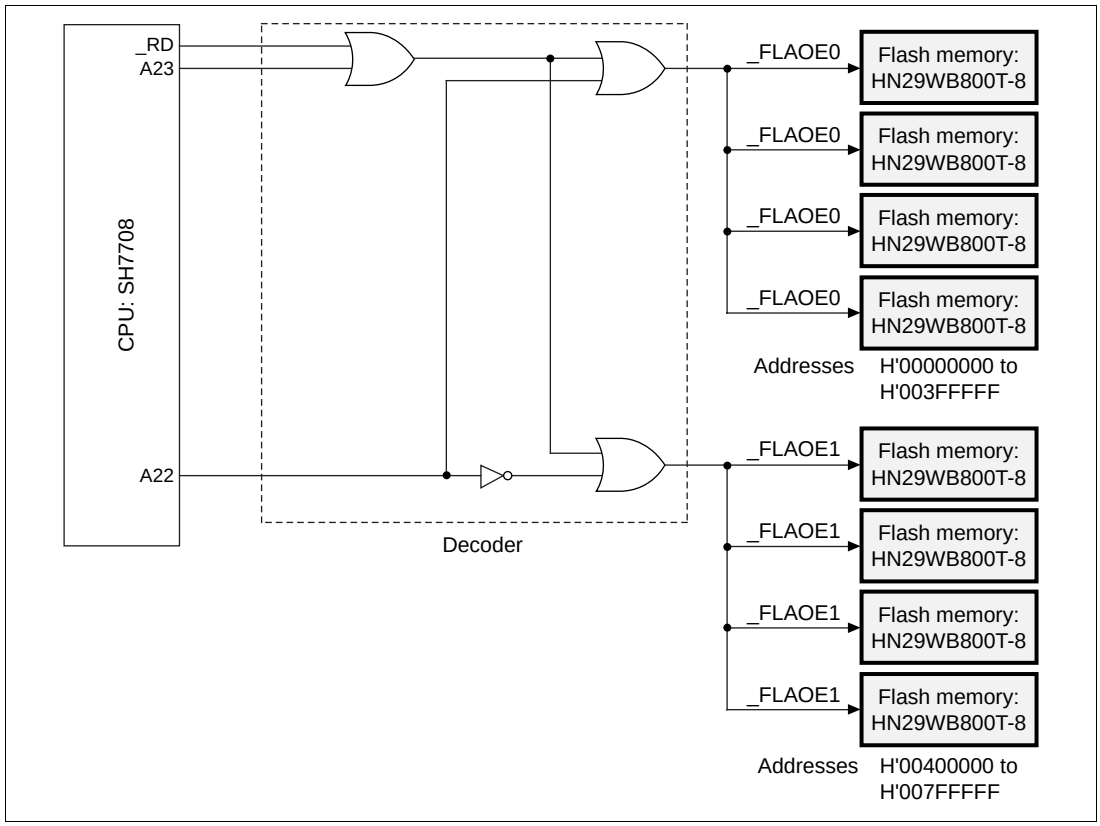


Figure 3.38 Flash Memory Decoder Logic Diagram

Table 3.8 Flash Memory Decoder Truth Table

Input			Output		
_RD	**A23**	**A22**	**_FLAOE0**	**_FLOE1**	
L	L	L	L	H	←Address H'00000000–H'003FFFFF selection
L	L	H	H	L	←Address H'00400000–H'007FFFFF selection
L	H	L	H	H	
L	H	H	H	H	
H	L	L	H	H	
H	L	H	H	H	
H	H	L	H	H	
H	H	H	H	H	

(3) DRAM Interface: The NAV-DS4 is equipped with two EDO mode 16-Mbit DRAMs (HM51W18165AJ-6), giving a total of 4 Mbytes, for use as working memory, used with a 32-bit bus width. CAS-before-RAS mode is used for refreshing. Figure 3.39 shows a block diagram of the interface between the SH7708 and the DRAMs.

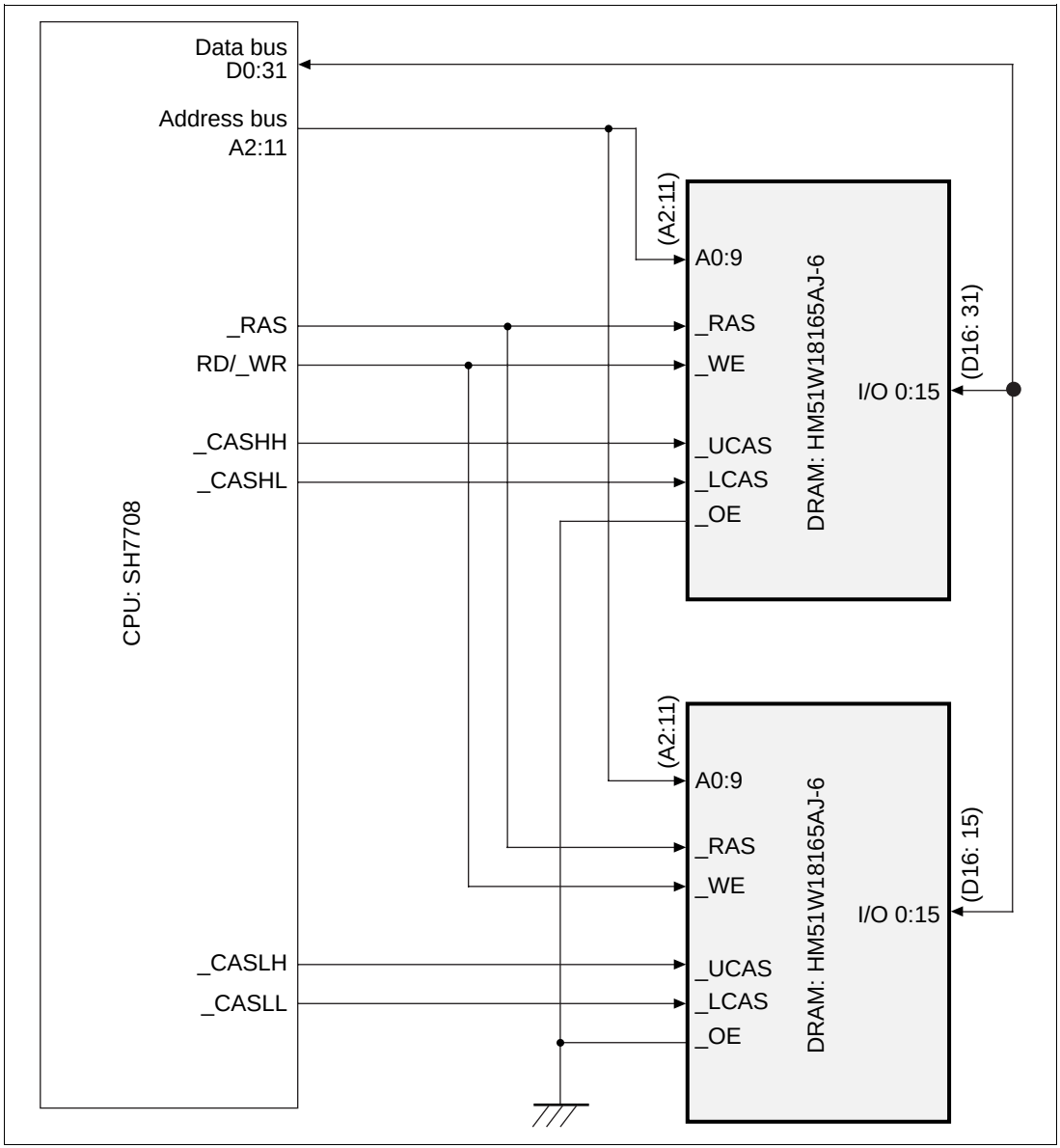
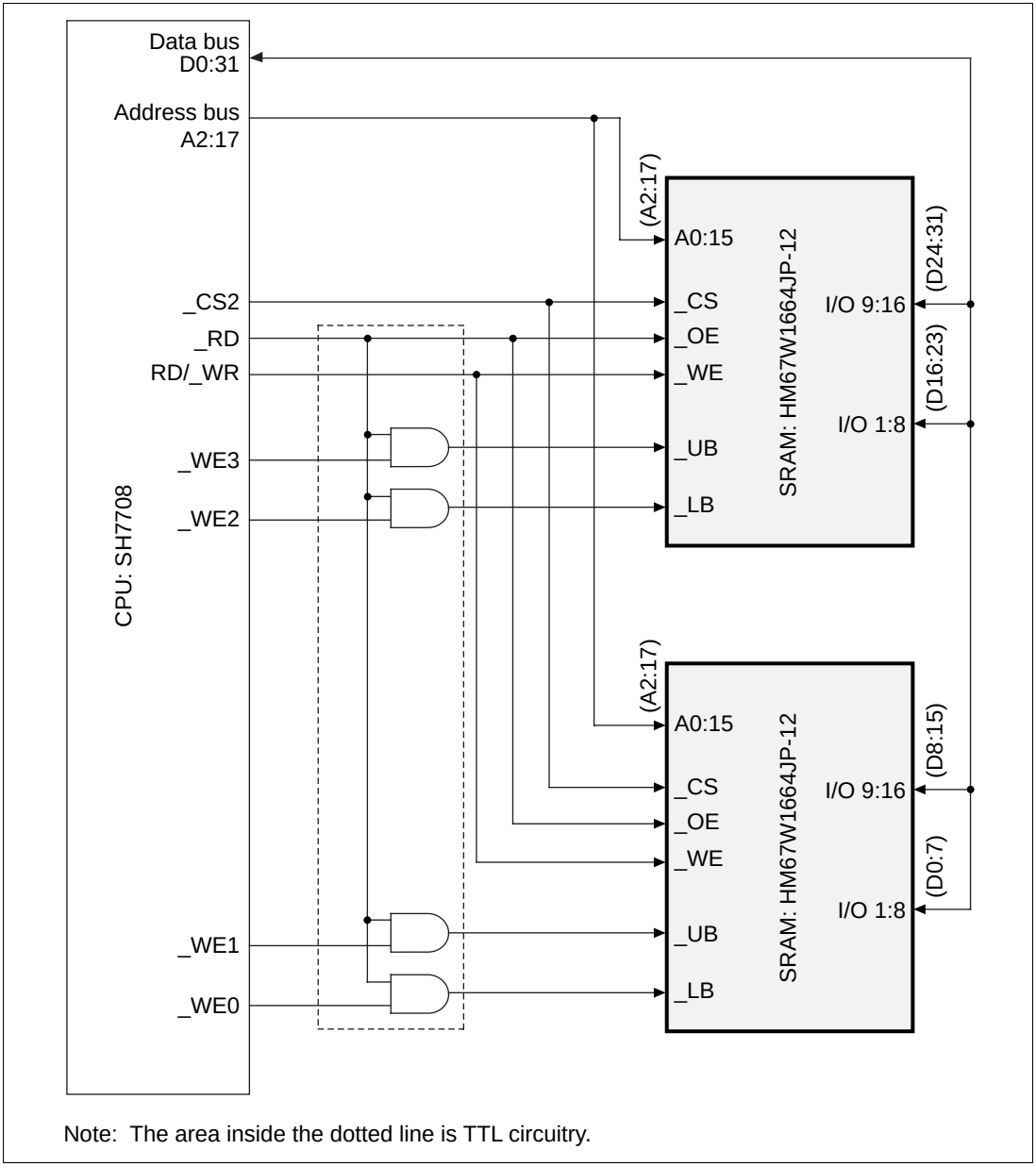


Figure 3.39 Block Diagram of EDO-DRAM Interface

(4) SRAM Interface: The NAV-DS4 is equipped with two 1-Mbit SRAMs (HM67W1664JP-12), giving a total of 256 kbytes, for use as working memory, used with a 32-bit bus width. Figure 3.40 shows a block diagram of the interface between the SH7708 and the SRAMs.



Note: The area inside the dotted line is TTL circuitry.

Figure 3.40 Block Diagram of SRAM Interface

(5) Q2-UGM Interface: The NAV-DS4 has a Q2 (HD64411F) and two EDO mode 16-Mbit DRAMs (HM5118165ATT-7) (4 Mbytes), used as the UGM, mounted on its daughter board. A 30 MHz clock is supplied from the SH7708 on the mother board as the drawing clock (CLK0). Accesses from the SH7708 to the Q2 are of two kinds: UGM accesses and accesses to the Q2's on-chip registers. The decoder for access selection consists of TTL circuitry. Figure 3.41 shows a logic diagram of the UGM/Q2 on-chip register selection decoder, and table 3.9 gives the corresponding truth table. As UGM access is performed by CPU transfer, and does not use the DMA controller, the Q2's _DACK pin is fixed high and the _DREQ pin is left open. Figure 3.42 shows a block diagram of the Q2 peripheral interface.

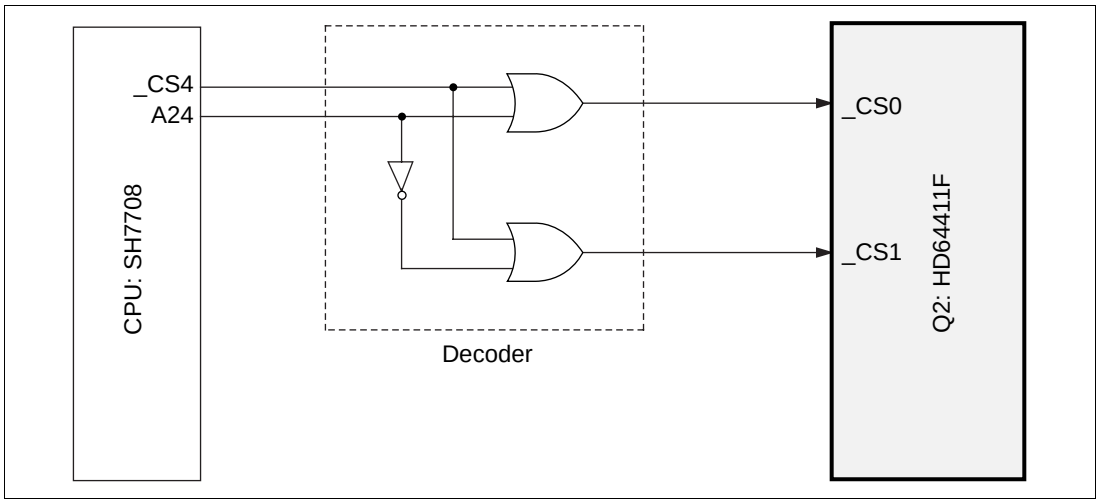
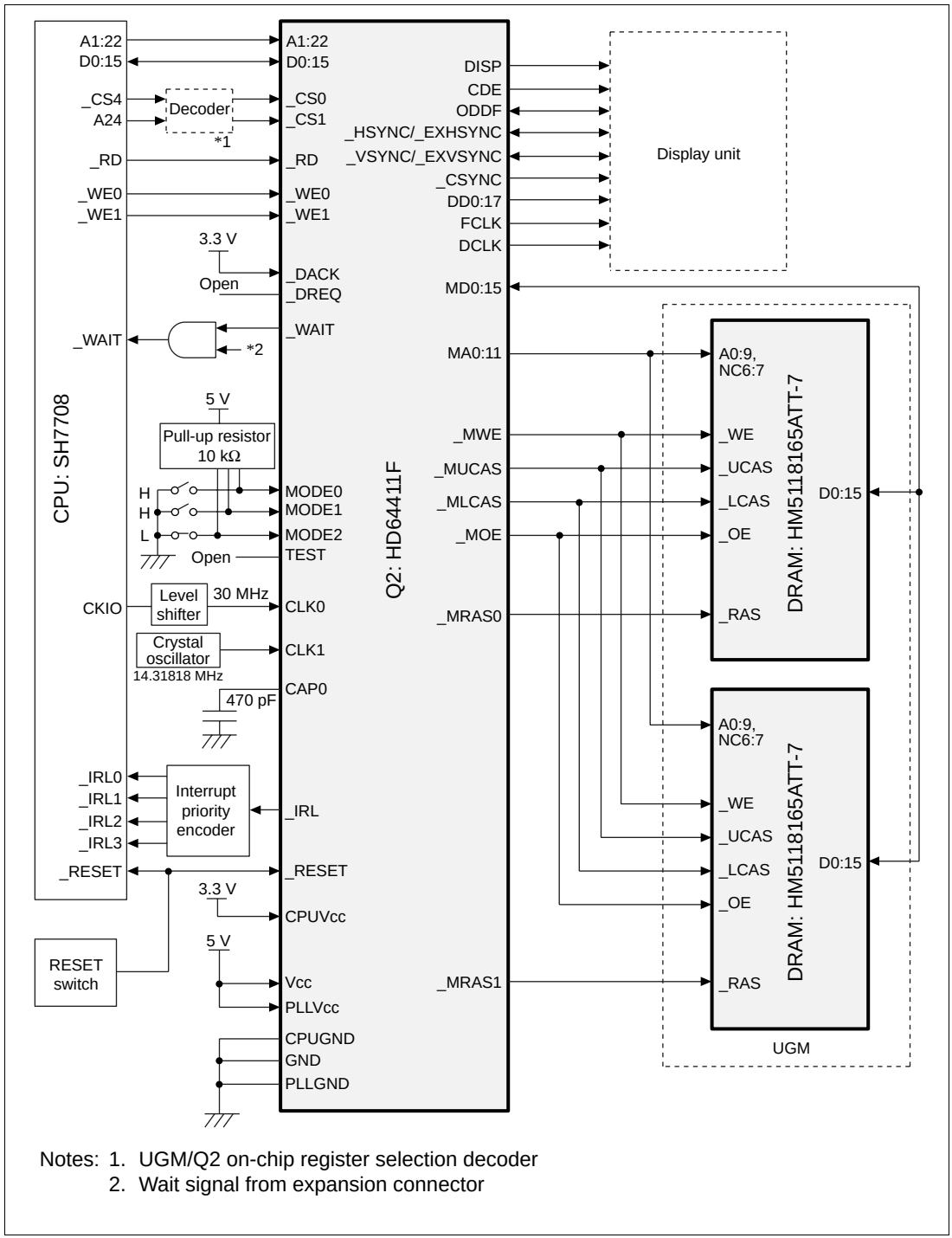


Figure 3.41 UGM/Q2 On-Chip Register Selection Decoder Logic Diagram

Table 3.9 UGM/Q2 On-Chip Register Selection Decoder Truth Table

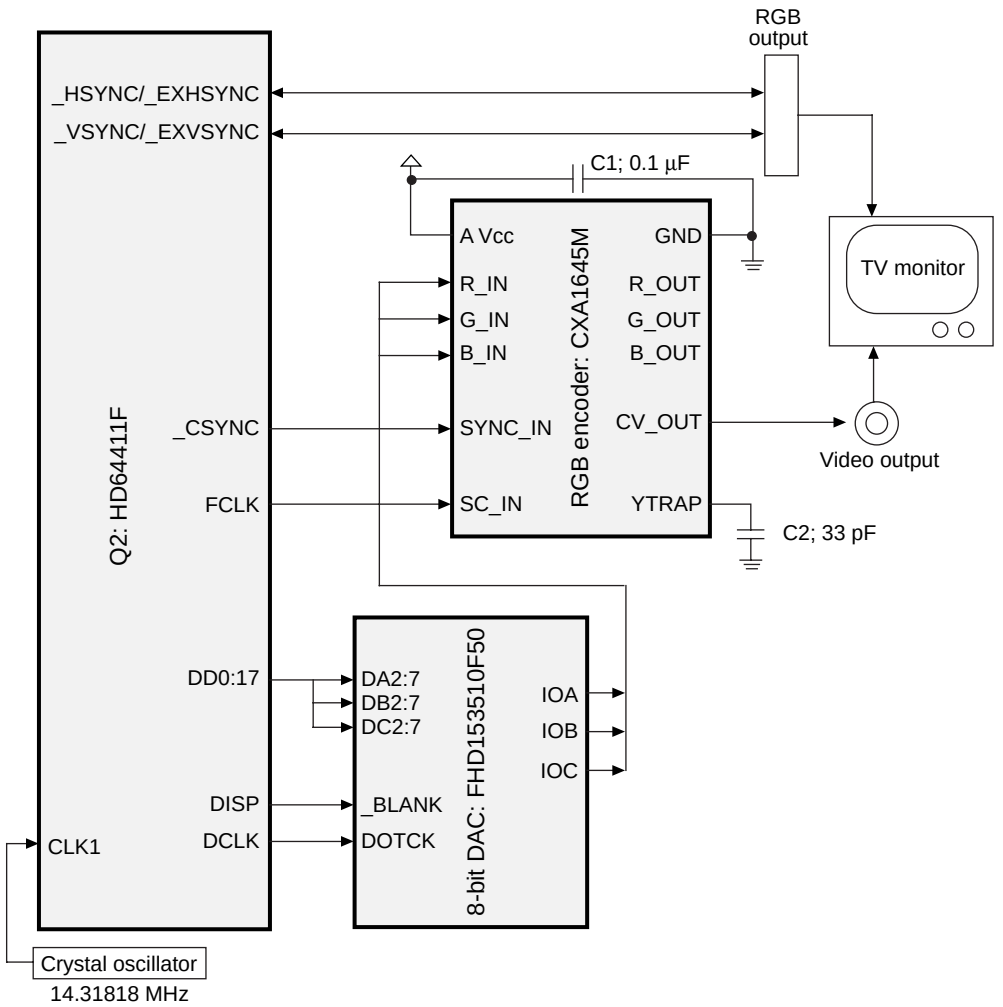
Input		Output		
_CS4	**A24**	**_CS0**	**_CS1**	
L	L	L	H	←UGM selection
L	H	H	L	←Q2 on-chip register selection
H	L	H	H	
H	H	H	H	



Notes: 1. UGM/Q2 on-chip register selection decoder
2. Wait signal from expansion connector

Figure 3.42 Block Diagram of Q2 Peripheral Interface

(6) Q2-display Unit Interface: An 8-bit 3-channel DAC (HD153510F50) and an RGB/video encoder (CXA1645) are mounted on the daughter board, and connected to the Q2, as the display unit. The display unit generates analog RGB signals and NTSC video signals from the 18-bit output from Q2 pins DD0 to DD17. Control of the resolution, the horizontal and vertical sync signals, etc., is performed by the Q2. A 14.318 MHz signal is supplied from the crystal oscillator on the daughter board as the display clock (CLK1). Figure 3.42 shows a block diagram of the display unit.



- Connect C1 (0.1 µF) and C2 (33 PF) between AVcc and GND and to the YTRAP pin. If C1 and C2 are not provided, color drift may occur in NTSC display images.
- With NTSC video output, set bit 5 = 1 and bit 4 = 0 (interlace sync mode) as the scan mode (SCM) setting in the Q2 display mode register (DSMR).

Figure 3.43 Q2 Display Unit Block Diagram

(7) Speech Output: Using the FPGA, the NAV-DS4's speech output unit converts 32-bit stereo speech data (16 bits each for left and right channels) transferred from the SH7708 into serial speech data, which it outputs via a DAC. The devices used are a µPD6376GS (manufactured by NEC) for the DAC and an EPF8452ATC100-3 for the FPGA. Figure 3.44 shows the speech output unit peripheral block diagram, and figure 3.45 shows an internal block diagram of the speech output FPGA.

The main components of the FPGA are a clock generator, an interrupt controller, and a parallel-to-serial converter. The clock generator generates clocks LRCK (selected by the status register) and CLK (7.5 MHz) for output to the DAC, using CLK_SH (30 MHz). The interrupt controller issues interrupt requests to the SH7708 in synchronization with LRCK. Each time an interrupt is generated, the SH7708 transfers parallel data to the 32-bit buffer in the FPGA. The transferred data is converted to serial data by the parallel-to-serial converter in synchronization with CLK. Then data synthesis is performed, and serial speech data is output to the DAC.

Figure 3.46 and 3.47 show the functions of the speech output FPGA registers. Figure 3.48 shows the speech output unit timing chart.

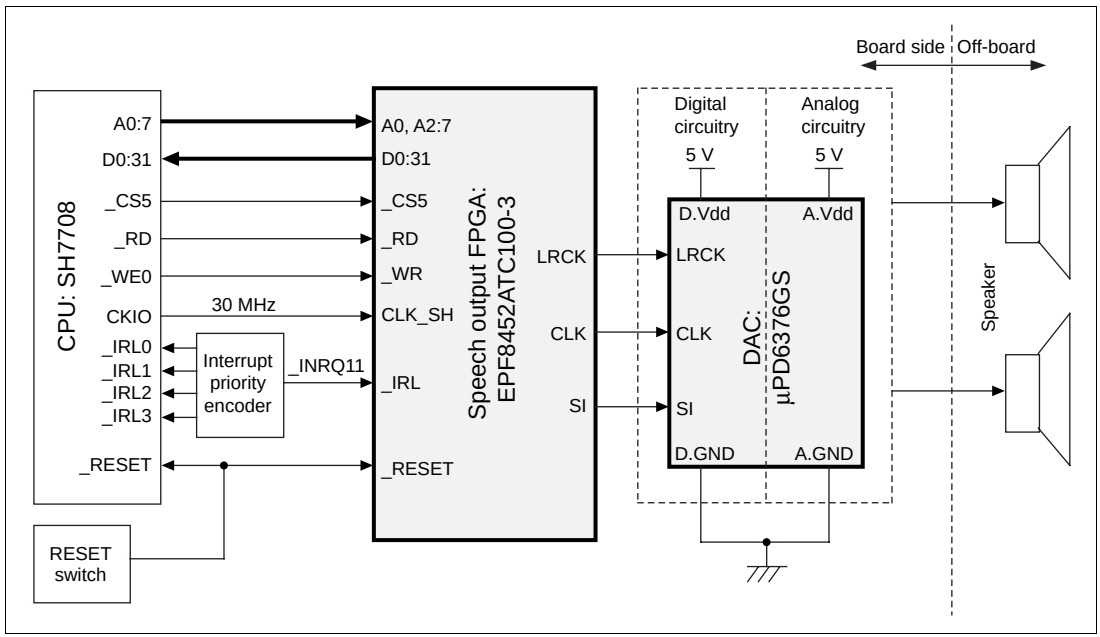


Figure 3.44 Speech Output Unit Peripheral Block Diagram

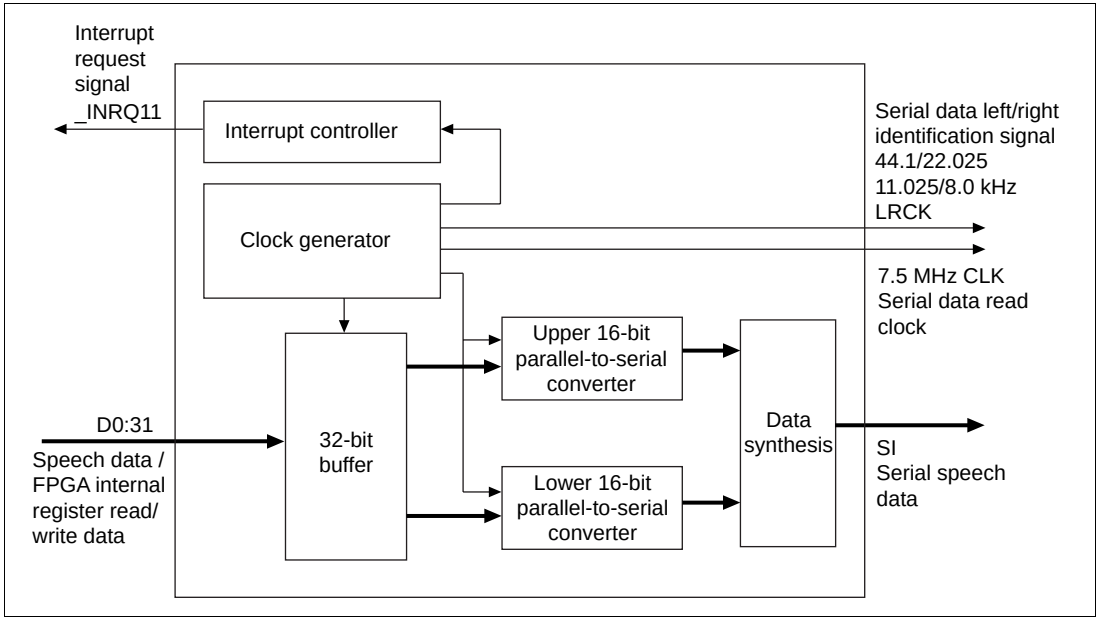


Figure 3.45 Speech Output FPGA Internal Block Diagram

Bit	D31	D30	D29 · · · D2	D1	D0
Bit name	DR31	DR30	· · ·	DR1	DR0
Initial value	0	0	· · ·	0	0

The receive register is used to input speech data. It is a write-only register, and _IRL is cleared after data is written.

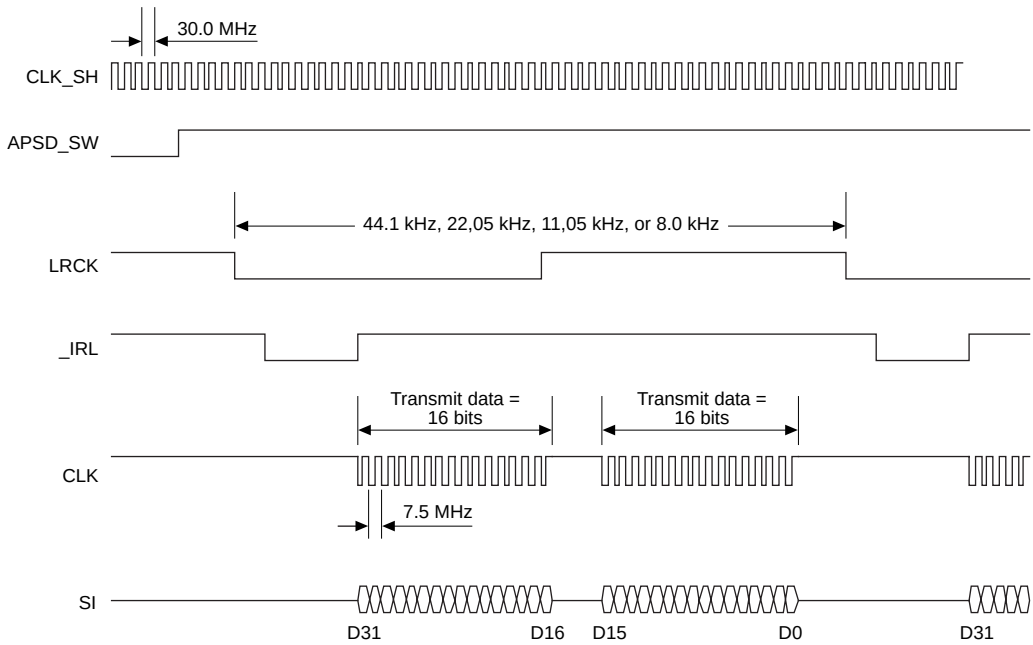
Figure 3.46 Receive Register Function

Bit	D31 . . . D4	D3	D2	D1	D0
Bit name	Not used	11E	22E	44E	DAE
Initial value	0	0	0	0	0

The status register is used for LRCK signal selection (see table below). DAE is used as ADPCM_SW.

	11E	22E	44E	DAE	Function
Set value	0	0	0	0	LRCK signal is not output. (ADPCM_SW: Off)
	0	0	0	1	LRCK signal is output at 8 [kHz].
	1	0	0	1	LRCK signal is output at 11.025 [kHz].
	—	1	0	1	LRCK signal is output at 22.05 [kHz].
	—	—	1	1	LRCK signal is output at 44.1 [kHz].

Figure 3.47 Status Register Settings and Functions



ADPCM_SW is generated by setting the DAE flag in the status register. LRCK, CLK, and _IRL are generated using CLK_SH.

Figure 3.48 Speech Output Unit Timing Chart

(8) SCSI Interface: The NAV-DS4 reads map data from a an external CD-ROM drive containing a navigation CD-ROM, and performs drawing and display based on this data. A SCSI interface is used for the external CD-ROM drive, and CPU transfer is used for data transfer. An SYM53CF96-2 (manufactured by Symbiosis Logic) is used for the SCSI controller, and an EPM7032LC44-6 (manufactured by Altera) is mounted as the control FPGA. Since the SCSI interface uses little-endian mode, the upper and lower bytes of the device are reversed for connection to the SH7708. Figure 3.49 shows the SCSI controller peripheral block diagram. A half-pitch 50-pin connector (female, shielded) is mounted, and single-end connection is used.

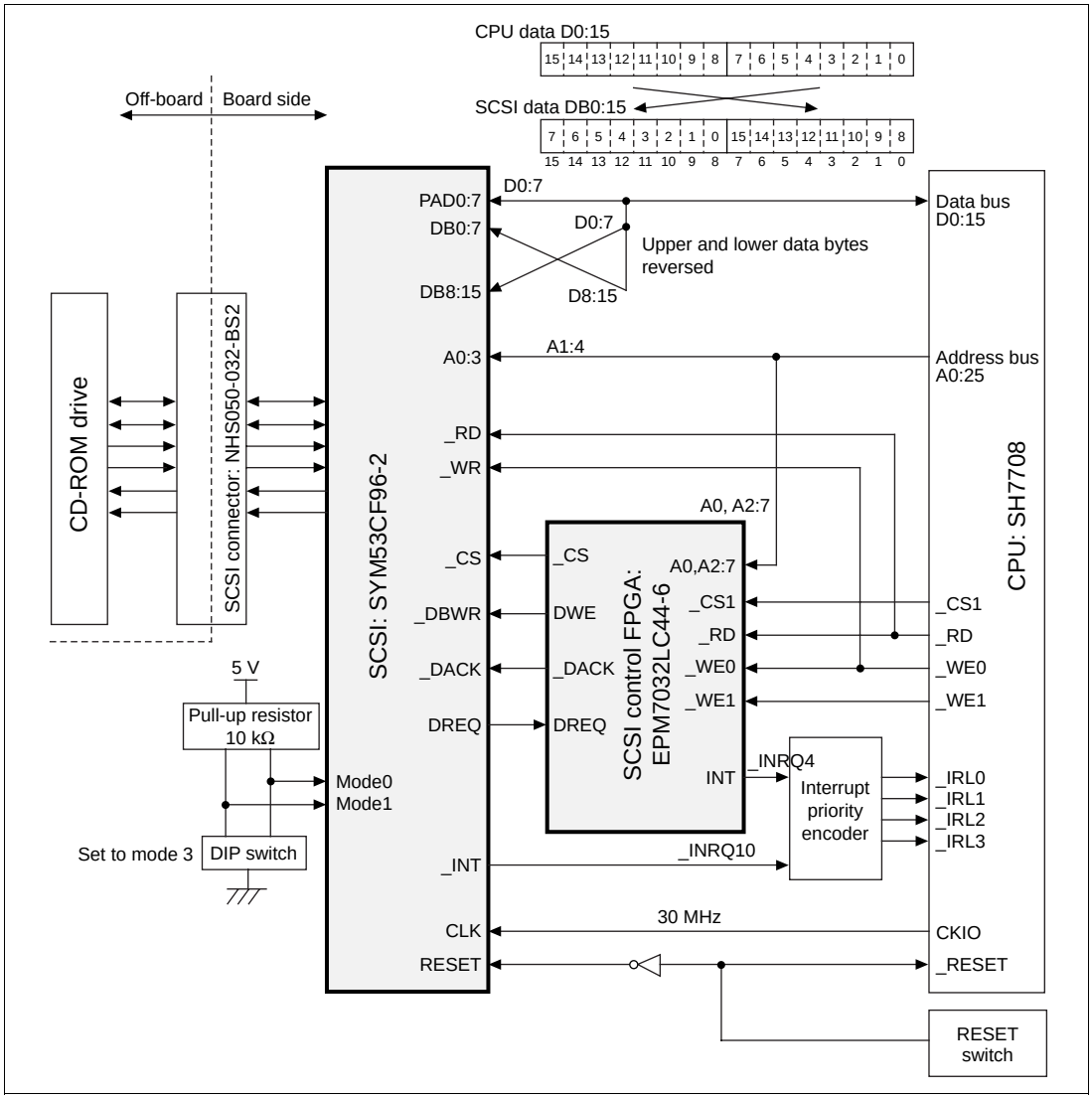


Figure 3.49 SCSI Controller Peripheral Block Diagram

(9) Key Input Interface: The NAV-DS4 is equipped with 16 switches mounted on the mother board, with an EPF8282ATC100-3 (manufactured by Altera) used as the control FPGA. Momentary switching is used, in which the on-state is maintained while the switch is pressed. The FPGA has an interrupt priority encoder function. Figure 3.50 shows the key input FPGA peripheral block diagram.

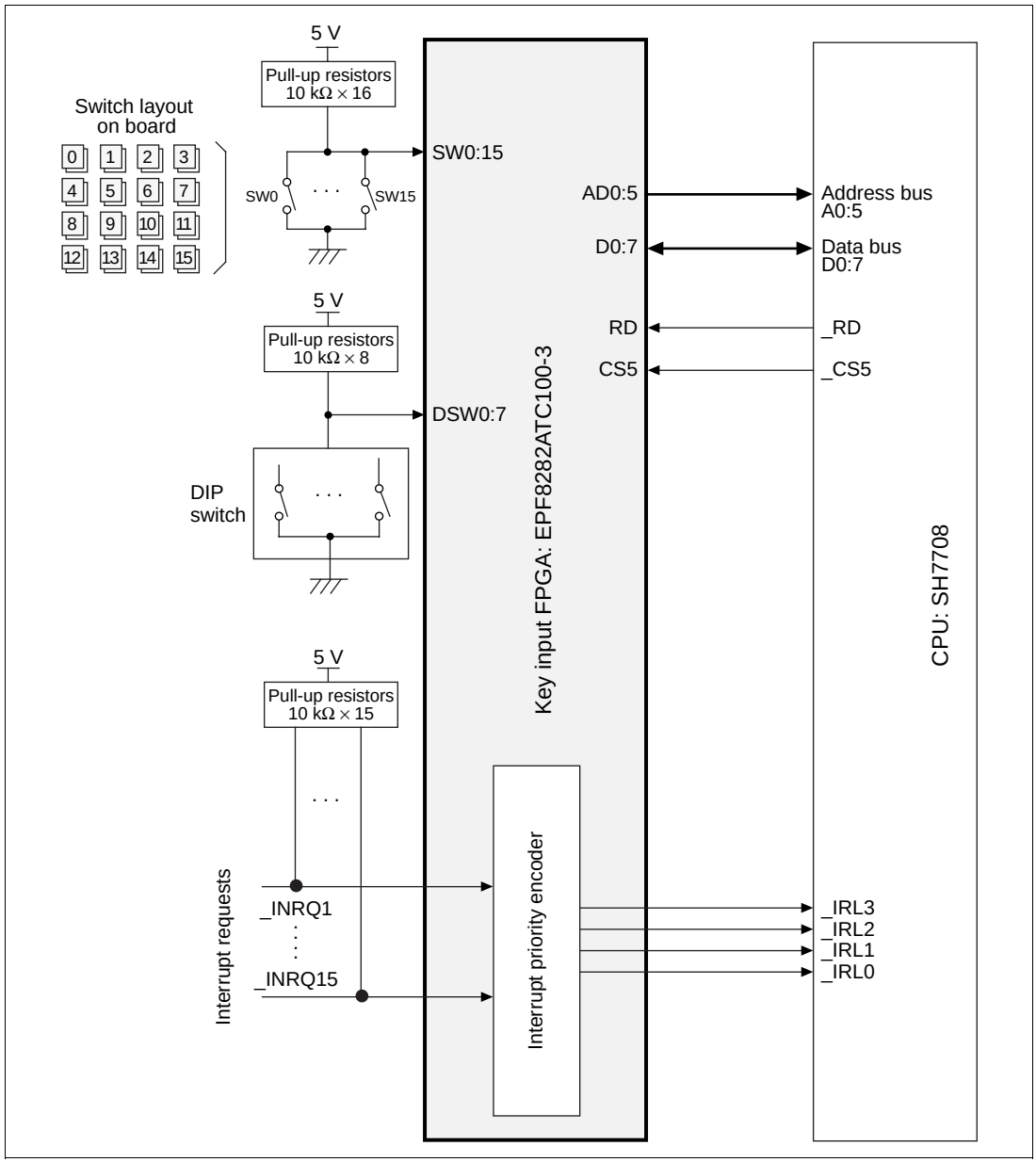


Figure 3.50 Key Input FPGA Peripheral Block Diagram

(10) Serial Communication Interface (SCI): The NAV-DS4 can perform serial data exchange with a PC using the SH7708's on-chip SCI. An MAX233ACWP (manufactured by Maxim) is used as the RS-232C driver. An RS-232C standard D-sub 9-pin (male) connector is used. A DIP switch allows switching between cross and straight connection. Figure 3.51 shows the SCI peripheral block diagram.

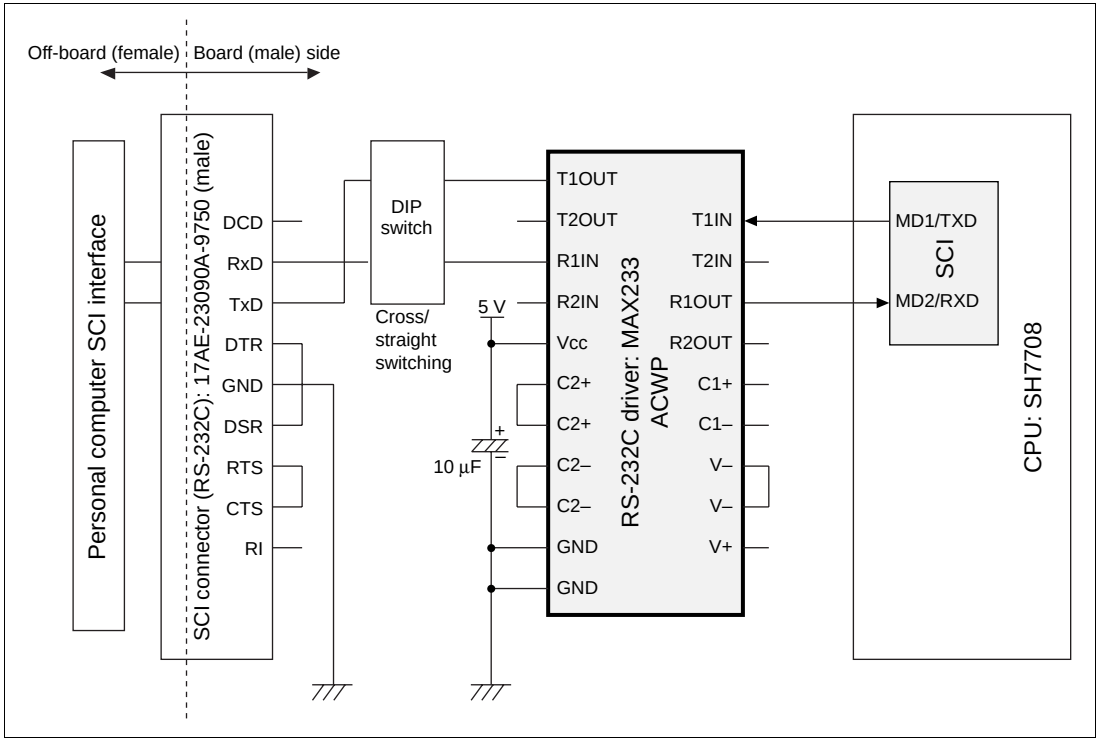


Figure 3.51 SCI Peripheral Block Diagram

(11) Expansion Connectors: The NAV-DS4 is equipped with board-to-board expansion connectors that provide for functional expansion by means of hardware. The expansion connectors are intended for connection to 5 V systems, and a level shifter is used between the connected system and the SH7708. Two HIF7C-80PA-1.27DSAL connectors (80-pin plug type, manufactured by Hirose) are used, and HIF7C-80DA-1.27DSAL units are required on the receptacle side. Figure 3.52 shows the expansion connector peripheral block diagram.

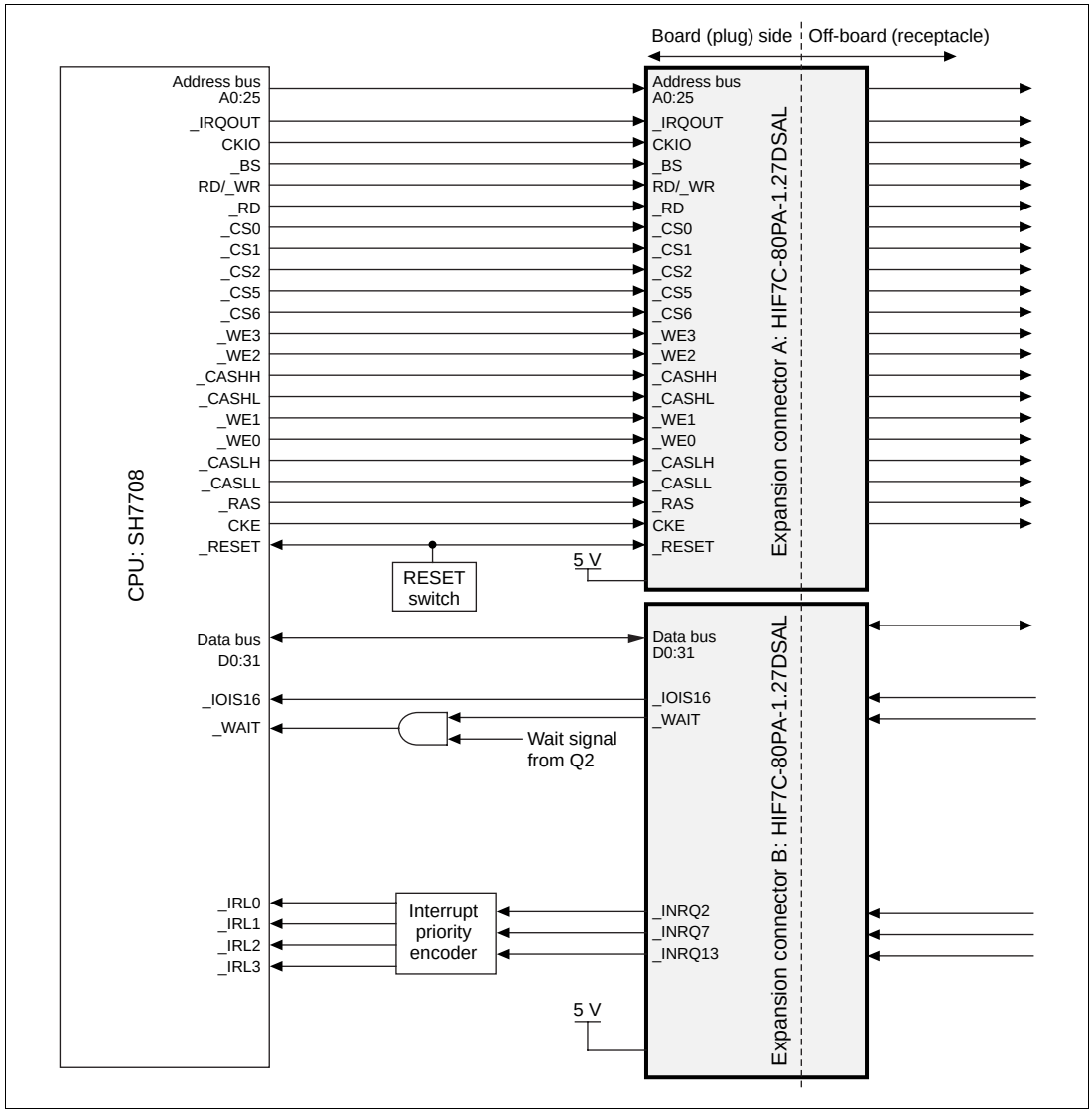
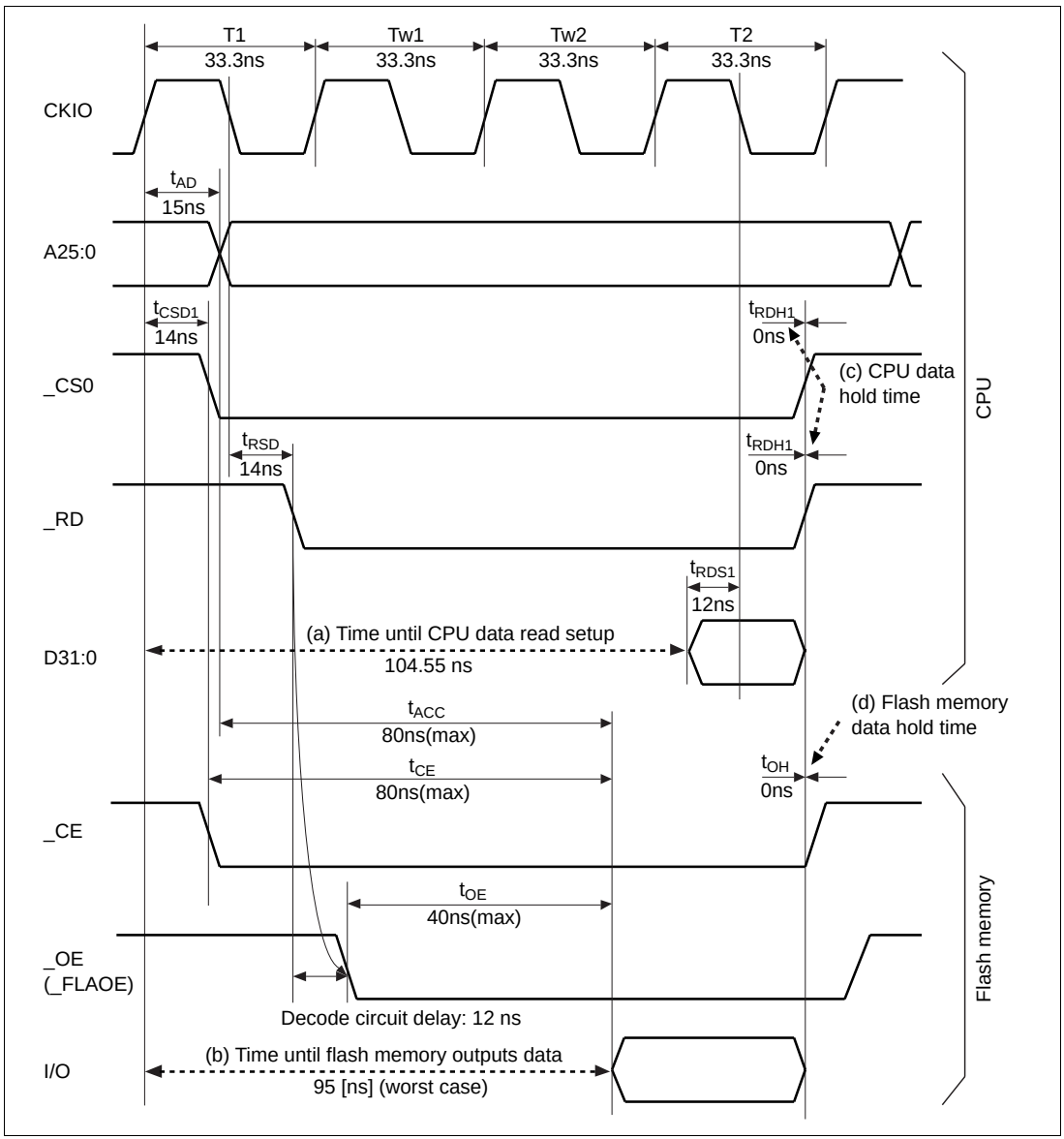


Figure 3.52 Expansion Connector Peripheral Block Diagram

3.6 SH7708 and Peripheral Timing Charts

(1) SH7708 Flash Memory Read Timing



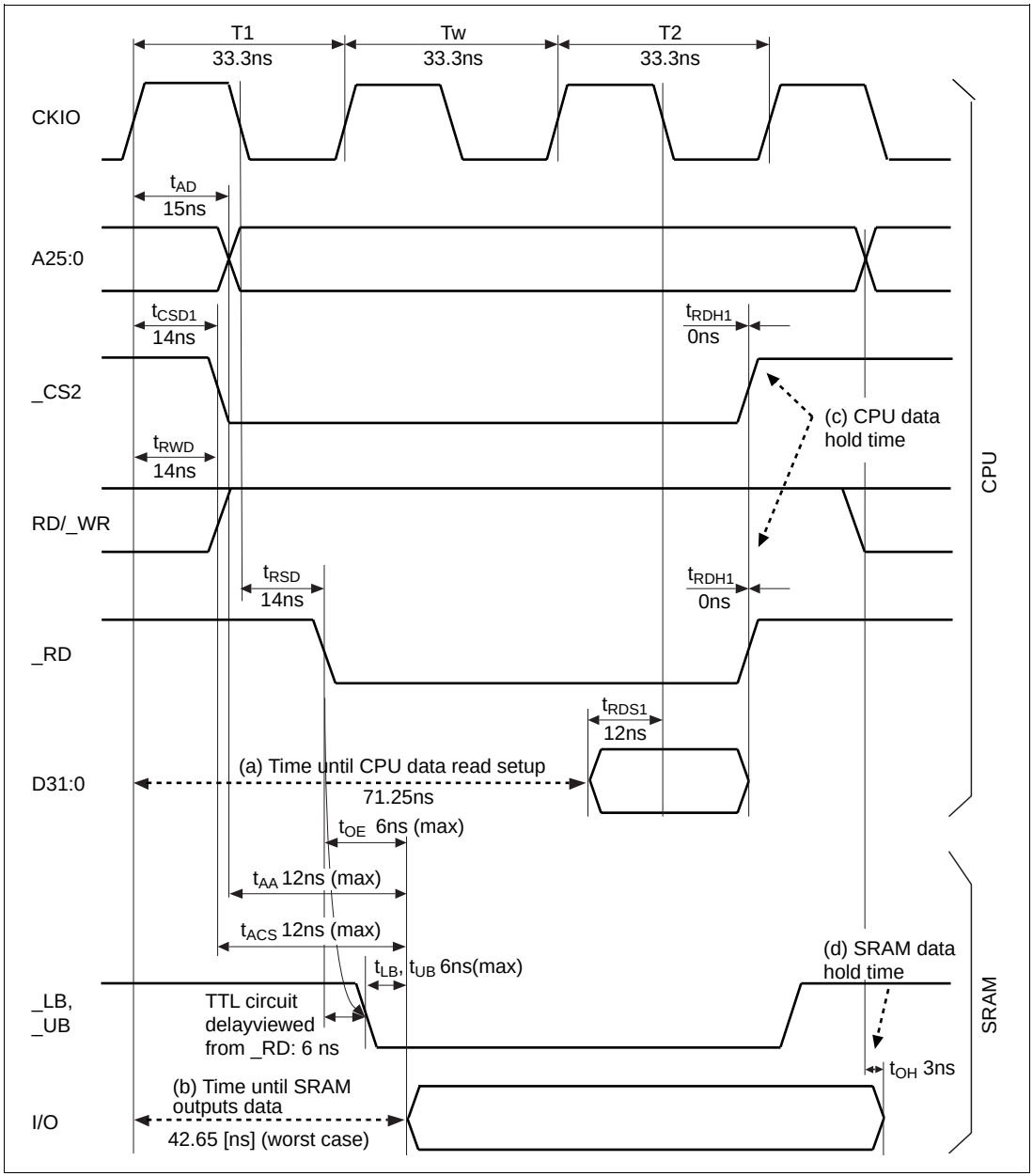
In case of 2-wait/4-cycle access to SH7708 flash memory:

1) Data setup time:
   (a) Time until CPU data read setup
   $T1 + Tw1 + Tw2 + (T2/2) - t_{RDS1} = 33.3 + 33.3 + 33.3 + (33.3/2) - 12 = 104.55$ [ns]
   (b) Time until flash memory outputs data
   Viewed from address: $t_{AD} + t_{ACC} = 15 + 80 = 95$ [ns] ← Worst case
   Viewed from _CE: $t_{CSD1} + t_{CE} = 14 + 80 = 94$ [ns]
   Viewed from _OE: $(T1/2) + t_{RSD}$ + decode circuit delay + $t_{OE} = (33.3/2) + 14 + 12 + 40 = 82.65$ [ns]
   Thus, (b) < (a), and the CPU setup time is satisfied.

2) Data hold time:
   (c) CPU data hold time $t_{RDH1} = 0$ [ns]
   (d) Flash memory data hold time $t_{OH} = 0$ [ns]
   Thus, (d) (c), and the CPU data hold time is satisfied.

From 1) and 2), 2-wait/4-cycle access is possible.

(2) SH7708 SRAM Read Timing



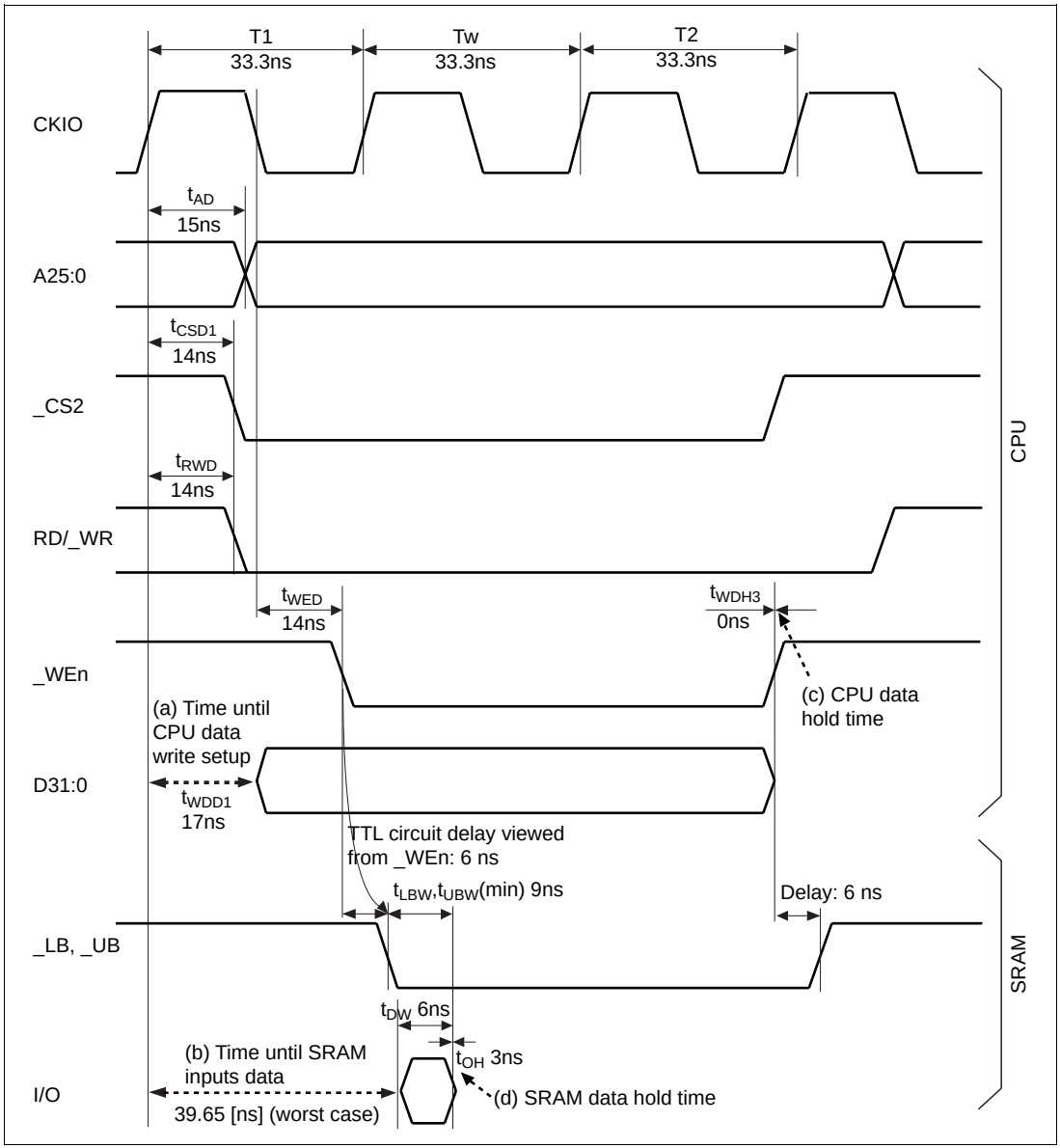
In case of 1-wait/3-cycle read access to SRAM:

1) Data setup time:
   (a) Time until CPU data read setup
   $T1 + Tw + (T2/2) - t_{RDS1} = 33.3 + 33.3 + (33.3/2) - 12 = 71.25$ [ns]
   (b) Time until SRAM outputs data
   Viewed from address: $t_{AD} + t_{AA} = 15 + 12 = 27$ [ns]
   Viewed from _CS2: $t_{CSD1} + t_{ACS} = 14 + 12 = 26$ [ns]
   Viewed from _RD: $(T1/2) + t_{RSD} + t_{OE} = (33.3/2) + 14 + 6 = 36.65$ [ns]
   Viewed from _LB, _UB: $(T1/2) + t_{RSD}$ + TTL circuit delay + t_{LB}, $t_{UB} = (33.3/2) + 14 + 6 + 6 = 42.65$ [ns] ← Worst case
   Thus, (b) < (a), and the CPU setup time is satisfied.

2) Data hold time:
   (c) CPU data hold time $t_{RDH1} = 0$ [ns]
   (d) SRAM data hold time (viewed from address) $t_{OH} = 3$ [ns]
   Thus, (d) (c), and the CPU data hold time is satisfied.

From 1) and 2), 1-wait/3-cycle read access is possible.

(3) SH7708 SRAM Write Timing



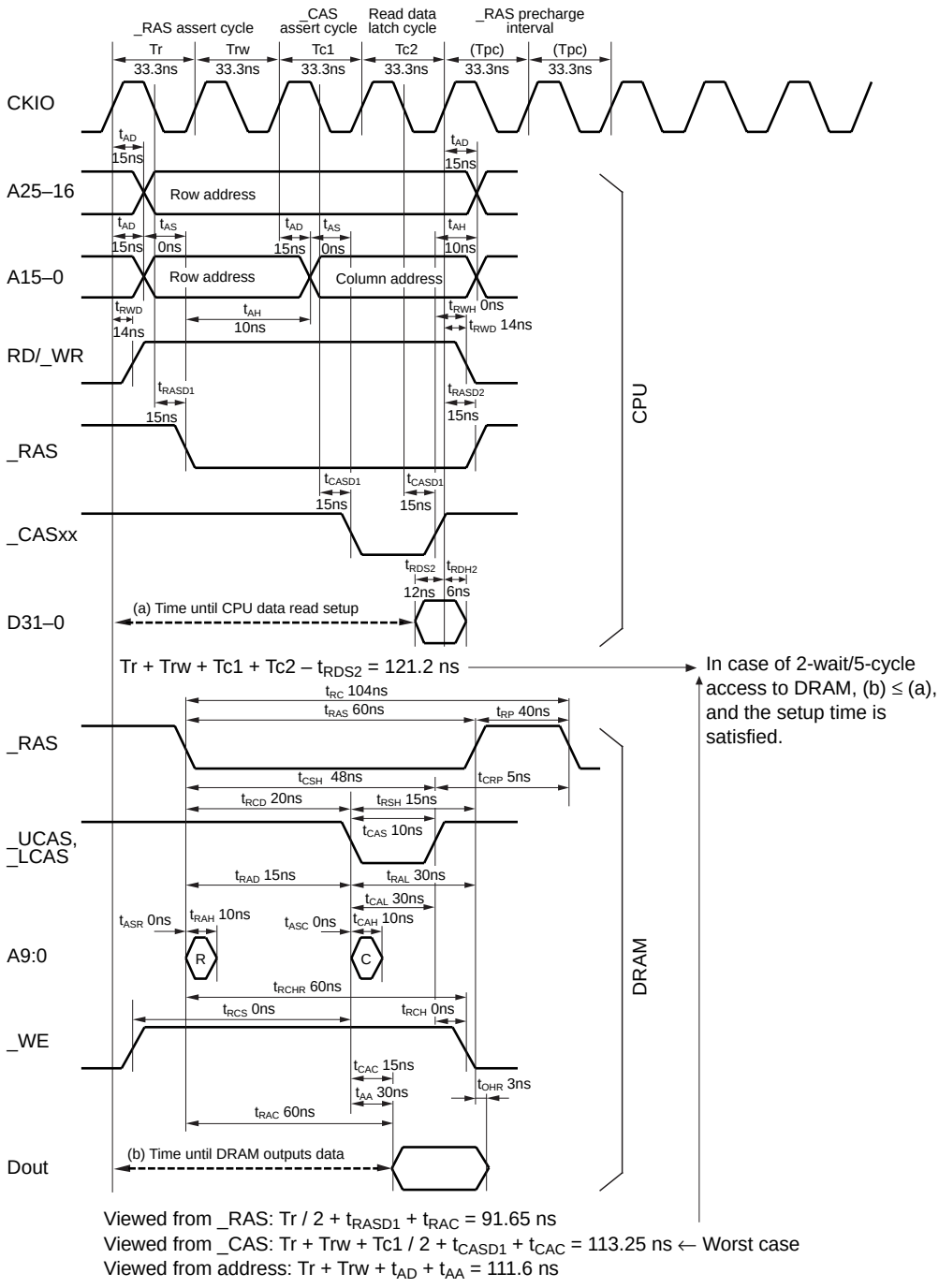
In case of 1-wait/3-cycle write access to SRAM:

1) Data setup time:
   (a) Time until CPU data write setup
   t_{WDD1} = 17 [ns]
   (b) Time until SRAM inputs data
   Viewed from _LB, _UB: (T1/2) + t_{WED} + TTL circuit delay + t_{LBW}, $t_{UBW} - t_{DW}$ = (33.3/2) + 14 + 6 + 9 – 6 = 39.65 [ns] ← Worst case
   Thus, (b) > (a), and the CPU setup time is satisfied.

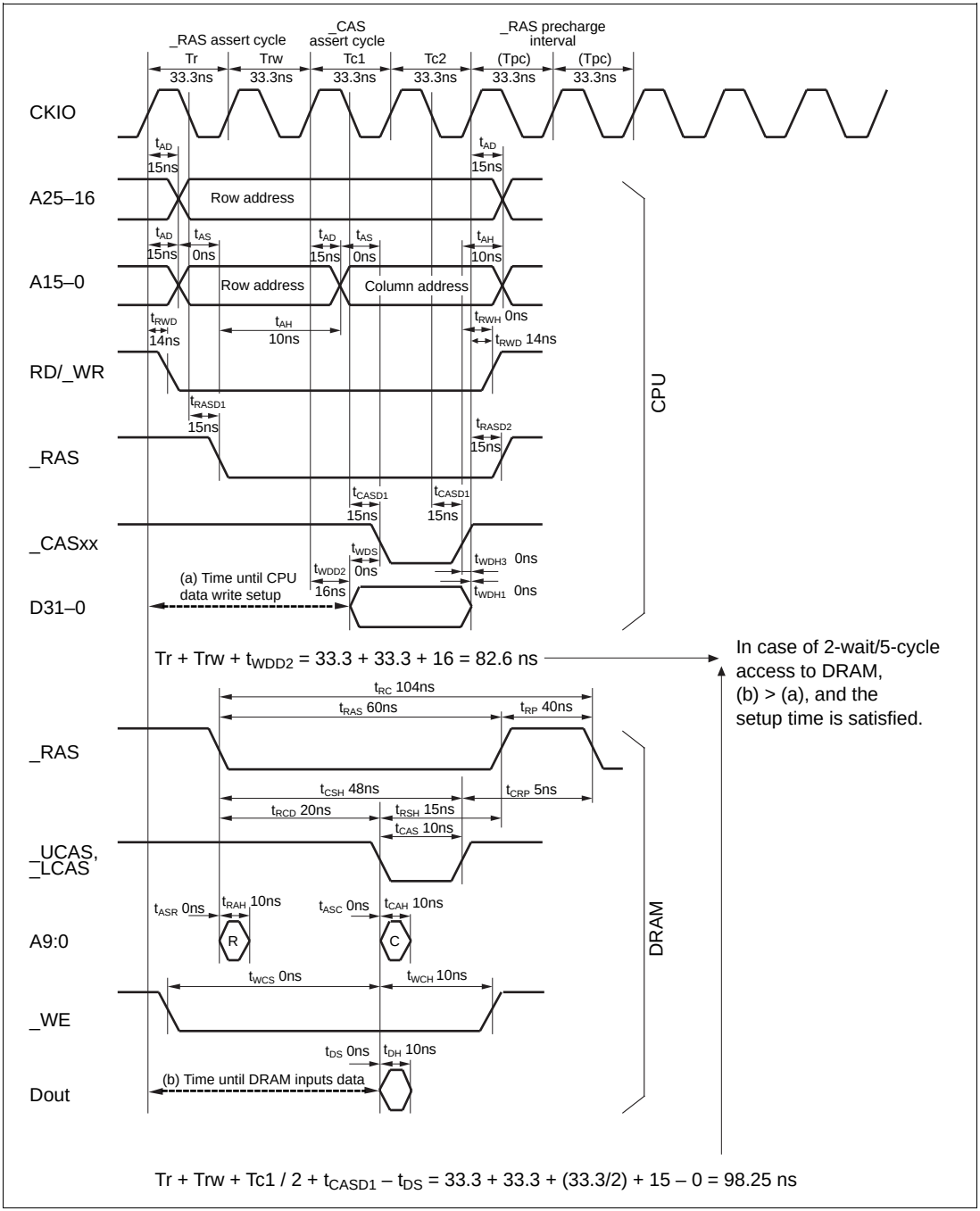
2) Data hold time:
   (c) CPU data hold time (viewed from _WEn) t_{WDH1} = 0 [ns]
   (d) SRAM data hold time t_{DH} = 0 [ns]
   Thus, (d) (c), and the CPU data hold time is satisfied.

From 1) and 2), 1-wait/3-cycle write access is possible.

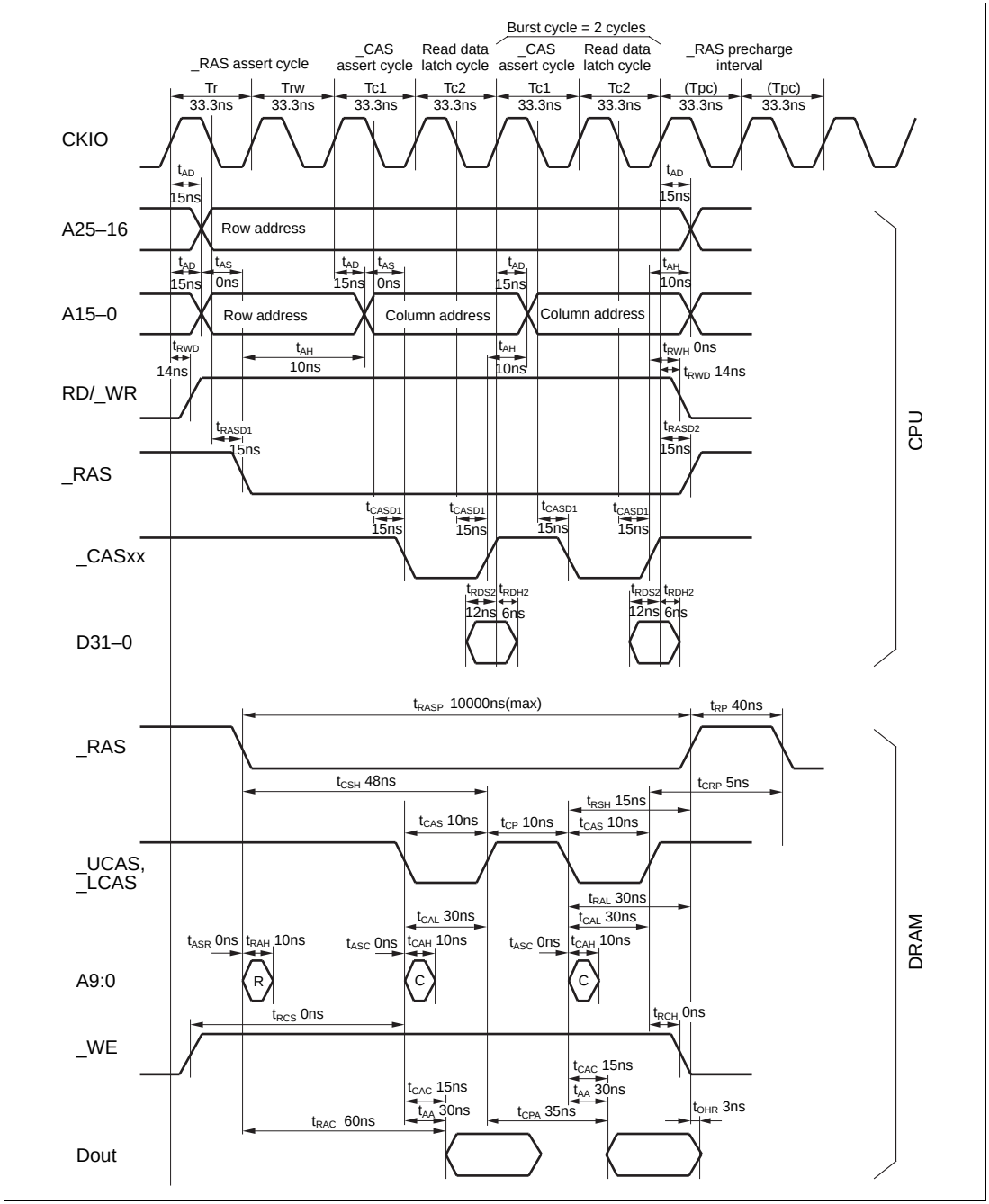
(4) SH7708 DRAM Normal Access Read Timing (EDO Mode)



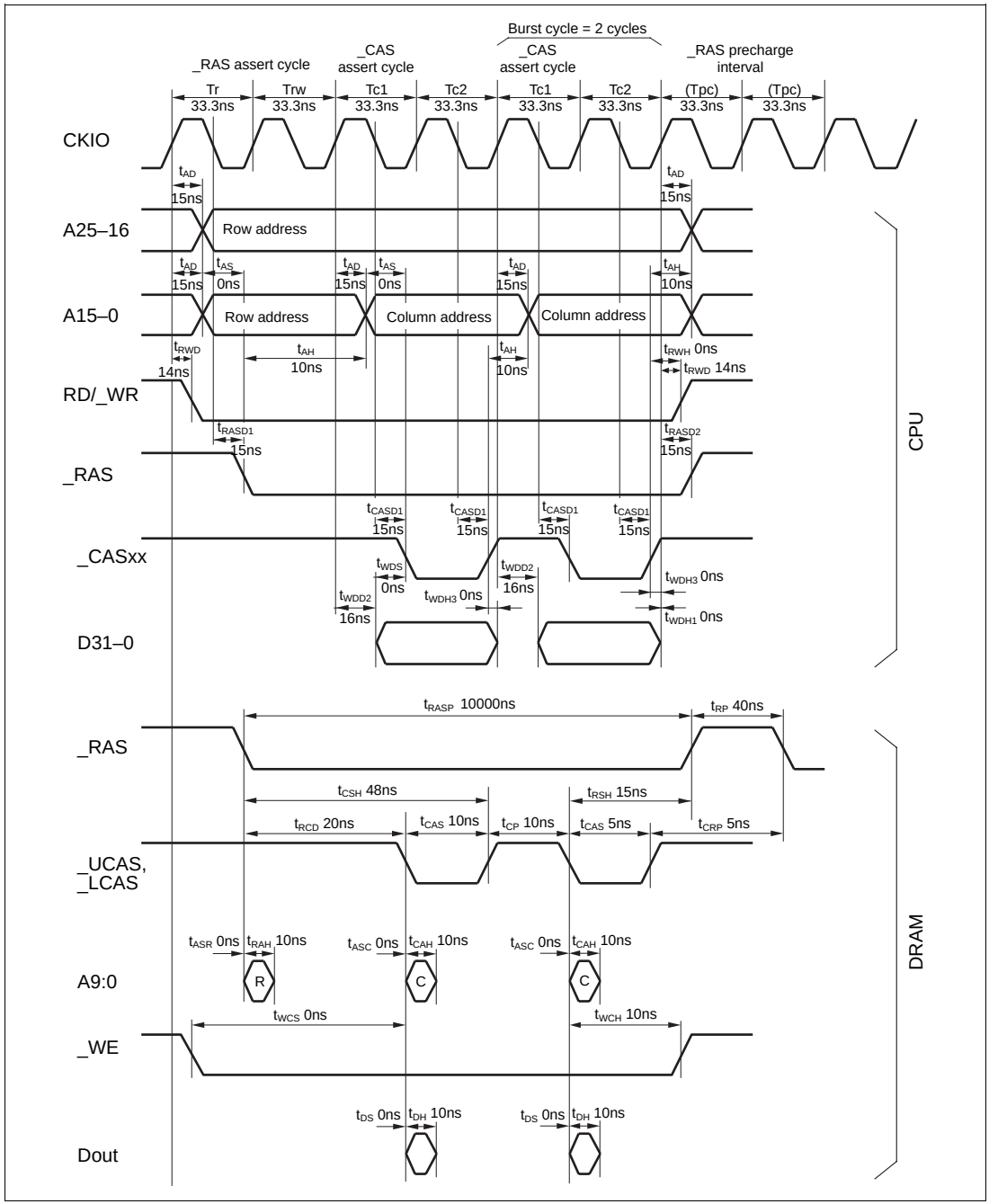
(5) SH7708 DRAM Normal Access Write Timing (EDO Mode)



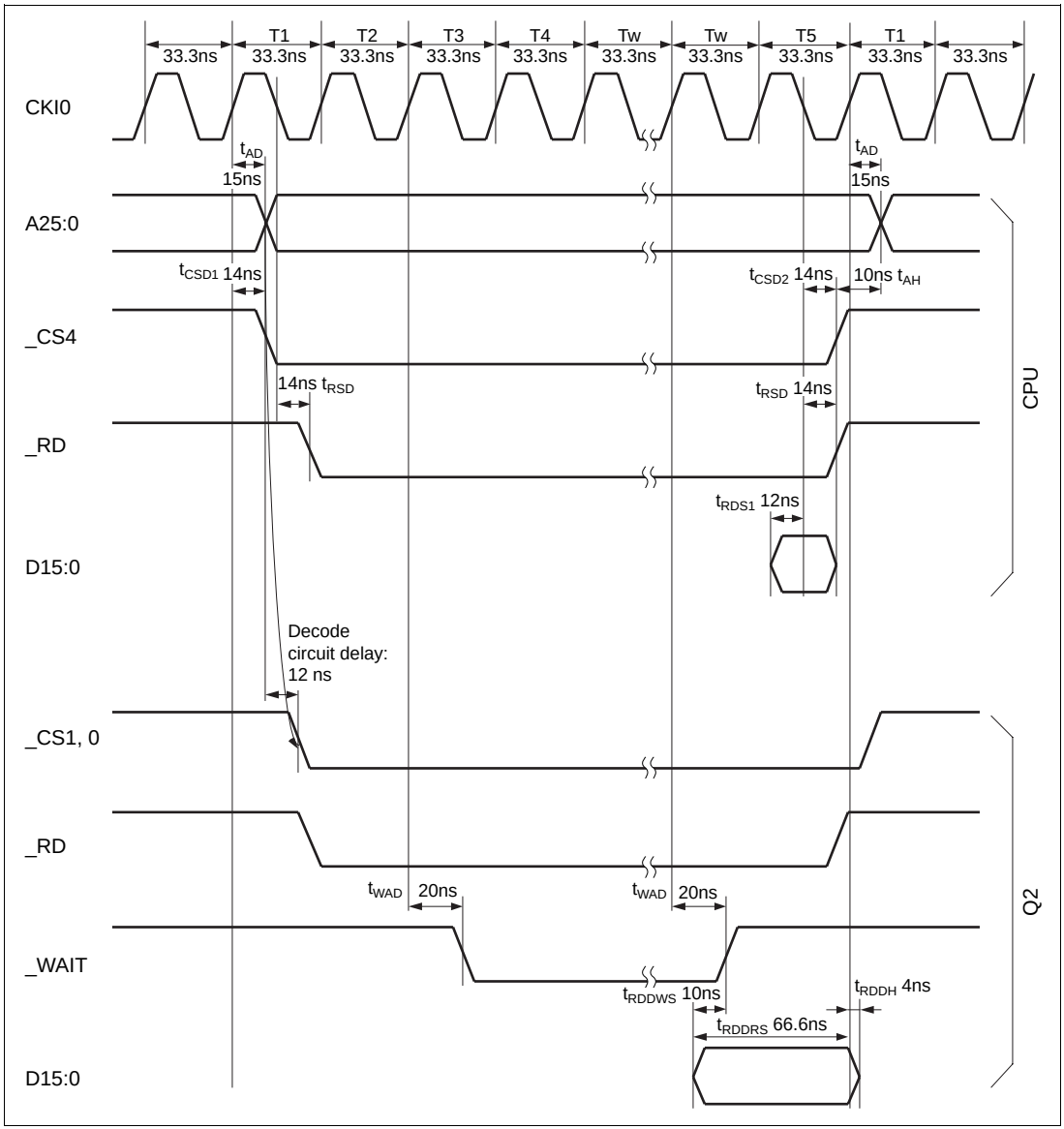
(6) SH7708 DRAM Burst Access Read Timing (EDO Mode)



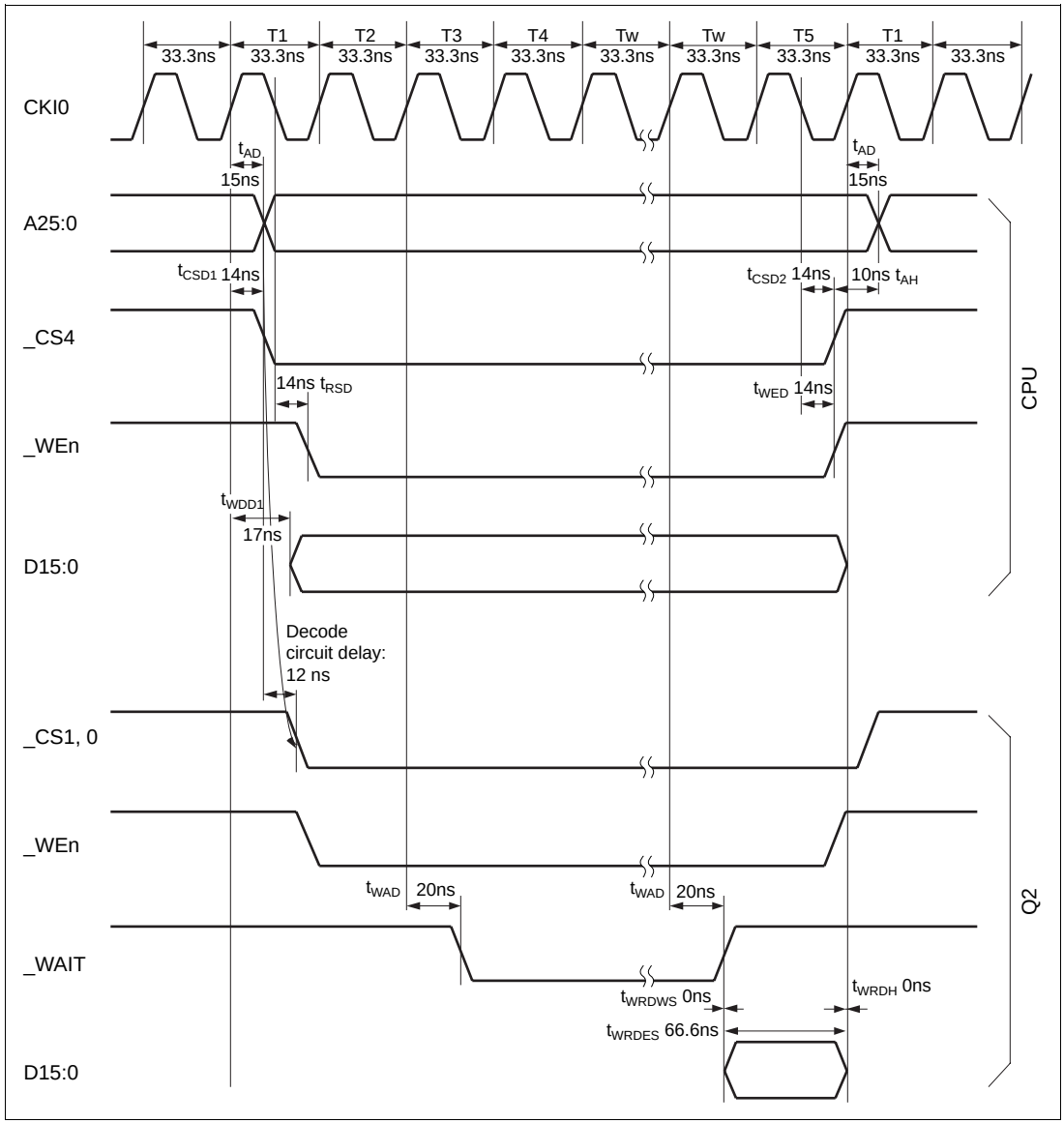
(7) SH7708 DRAM Burst Access Write Timing (EDO Mode)



(8) SH7708 Q2 Read Timing



(9) SH7708 Q2 Write Timing



SH Graphics/Speech Processing Demonstration System NAV-DS4 Application Note

Publication Date: 1st Edition, January 1998
Published by: Semiconductor and IC Div.
Hitachi, Ltd.
Edited by: Technical Documentation Center
Hitachi Microcomputer System Ltd.