PROTEK DEVICES
ANALOG PRODUCTS DIVISION

PA2535/2536
0.35Ω Dual SPDT Analog Switch

Features

- Low Voltage Operation
- Low On-Resistance Ron = 0.35Ω @ 2.7 V
- −69 dB O_{IRR} @ 2.7 V, 100 kHz
- DFN-10 Package
- ESD Protection >2000 V
- Latch-Up Current >300 mA (JESD 78)

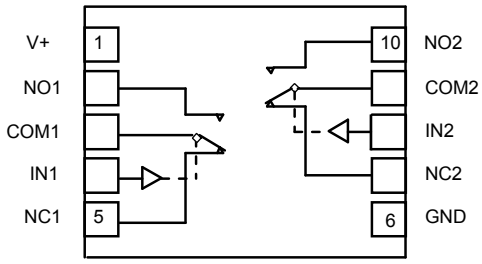
Benefits

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.8-V Logic Compatible
- High Bandwidth

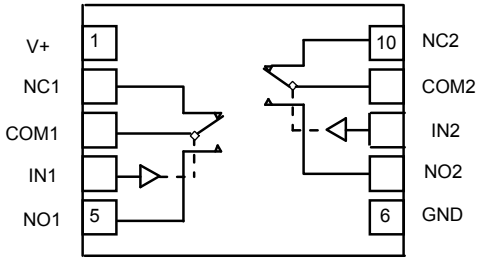
Applications

- Cellular Phones
- Speaker Headset Switching Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement
- USB1.1

PA2535



PA2536



Description

The PA2535/PA2536 are 0.35Ω dual SPDT analog switches designed for low voltage applications.

The PA2535/PA2536 has on-resistance matching (less than 0.05Ω @ 2.7 V) and flatness (less than 0.2Ω @ 2.7 V) that is guaranteed, over the entire voltage range. Additionally, low logic thresholds make the PA2535/PA2536 an ideal interface to low voltage DSP control signals.

The PA2535/PA2536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is −69 dB @ 100 kHz.

The PA2535/PA2536 is built on ProTek Analog's high-density low voltage CMOS process. An epitaxial layer is built in to prevent latchup.

The PA2535/PA2536 contains the additional benefit of 2,000 Volt ESD protections.

In a space saving DFN-10 lead (Pb)-free package, the PA2535/PA2536 are high performance, low R_{on} switches for battery powered applications.

No lead (Pb) is used in the manufacturing process either inside the device/package or on the external terminations.

As a committed partner to the community and the environment, ProTek Analog manufactures this product with the lead (Pb)-free device terminations.

For analog switching products manufactured in DFN packages, the lead (Pb)-free "LF" suffix is being used as a designator. Lead (Pb)-free DFN products purchased at any time will have either a nickel-palladium-gold device termination or a 100% matte tin device termination.

The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

Truth Table

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

Ordering Information

Temp Range	Package	Part Number	
-40 to +80°C	DFN-10	PA2535DN-T7 PA2536DN-T7	PA2535DN-T13 PA2536DN-T13

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Absolute Maximum Ratings
Reference to Ground

V+……-0.3 to +6.0V
IN, COM, NC, NO……....-0.3 to (V+ +0.3V)
Continuous Current (NO, NC, COM)……...300mA
Peak Current……500mA
(Pulsed at 1mS, 10% Duty Cycle)
Storage Temperature (D Suffix)……-65 to 150°C
ESD per Method 3015.7……> 2KV
Power Dissipation……1191mWATT

NOTES
a. Signals on NC, NO, COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered to PC Board.
c. Derate 4.0 mW/°C above 70 °C
d. Derate 14.9 mW/°C above 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability
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Specification V+ = 3.0V *Test Conditions unless otherwise specified: V+ = 3.0V±10%, V_{IN} = 0.4 V or 2.0V*

Parameter	Symbol	Test Conditions	Temp	Min	Typ	Max	Unit
Analog Switch							
Analog Signal Range	V_{NO},V_{NC}, V_{COM}		Full	0.0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 2.7V, V_{COM} = 0.9V- 1.5V I_{NO} , I_{NC} = 50mA,	Room Full		0.35	0.5 0.6	Ω
R_{ON} Matching	ΔR_{ON}					0.05	
R_{ON} Flatness	$R_{ON(FLAT)}$				0.09	0.2	
Switch Off Leakage Current	$I_{OFF(NO)}$ or $I_{OFF(NC)}$	V+ = 3.3 V, V_{NO}, V_{NC}= 1.0 V/3.0 V, V_{COM} = 3.0 V/1.0 V	Room Full	-1 -10		-1 -10	nA
	$I_{COM(OFF)}$		Room Full	-1 -10		-1 -10	
Channel On Leakage Current	$I_{COM(ON)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1.0V/3.0 V	Room Full	-1 -10		-1 -10	
Digital Control							
Input High Voltage	V_{INH}		Full	2.0			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		10		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		52	82 90	nS
Turn Off Time	t_{OFF}		Room Full		43	73 78	
Break Before Make Time	t_{BBM}		Room Full	1	6		
Charge Injection	Q_{INJ}	CL = 1 nF, VGEN = 0 V, RGEN = 0 Ω	Room		21		pC
Off Isolation	OIRR	RL = 50 Ω, CL = 5 pF, f = 1 MHz	Room		-69		dB
Crosstalk	X_{TALK}		Room		-69		
NO, NC OFF Capacitance	$C_{NO(off)}$ $C_{NC(off)}$	VIN = 0 or V+, f = 1 MHz	Room		145		pF
Chanel On Capacitance	C_{ON}		Room		406		
Power Supply							
Supply Range	V+	V_{IN} = 0 or V+		1.8		5.5	V
Supply Current	I+				0.01	1.0	µA

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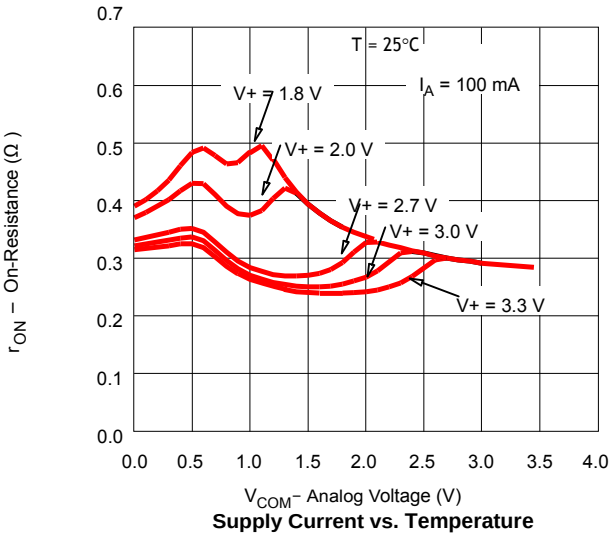
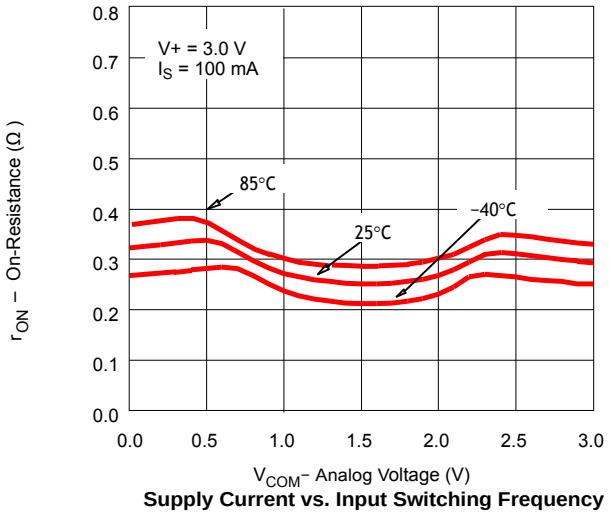
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

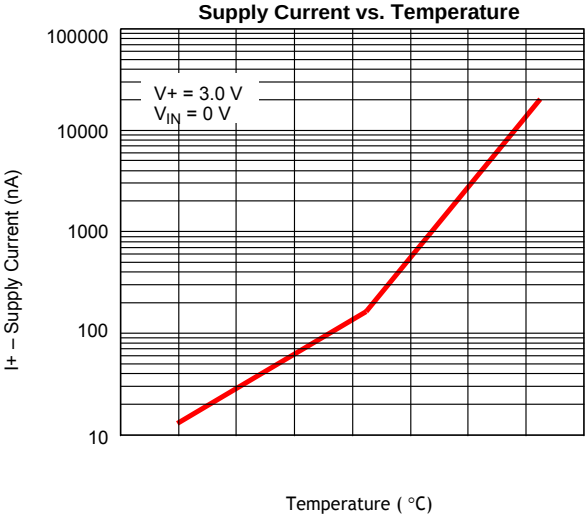
r_{ON} vs. $V_{COM}$and Supply Voltage



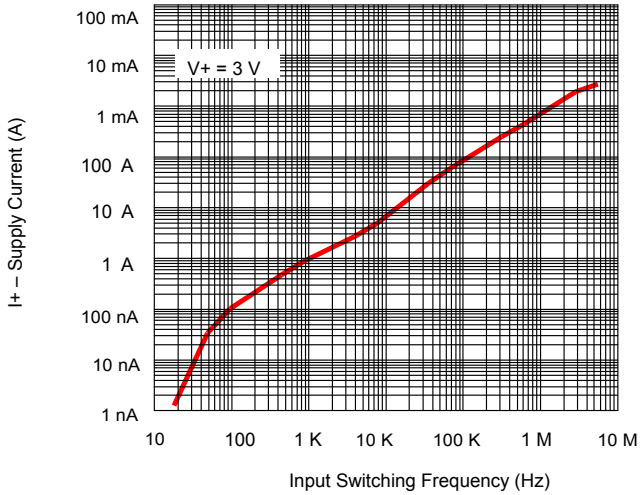
r_{ON} vs. Analog Voltage and Temperature (NC1)



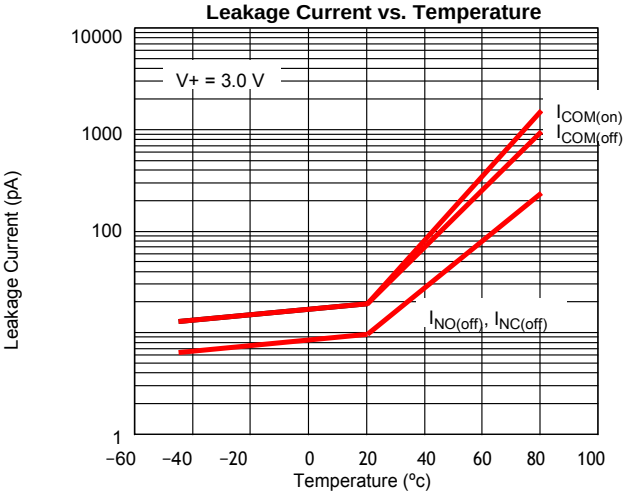
Supply Current vs. Temperature



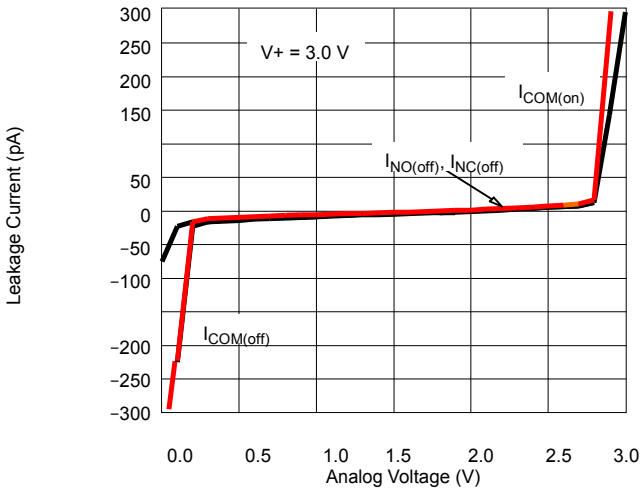
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature



Leakage vs. Analog Voltage



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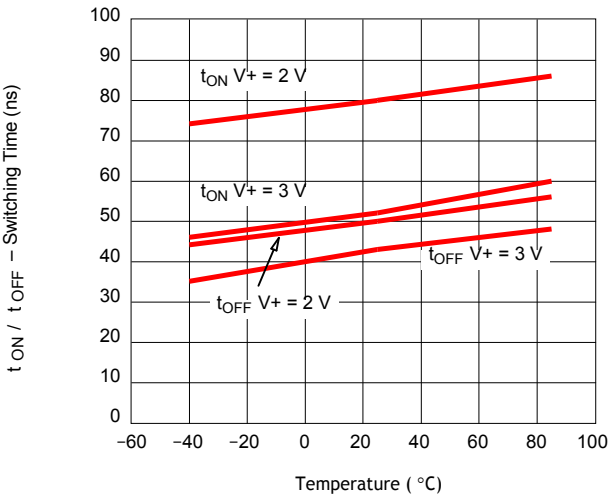
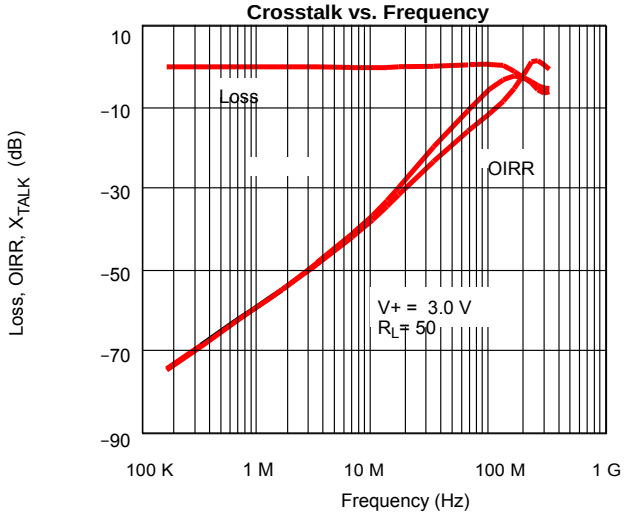
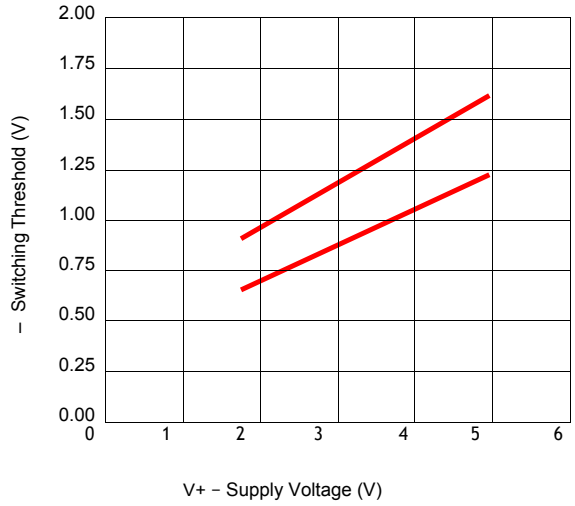
Switching Time vs. Temperature



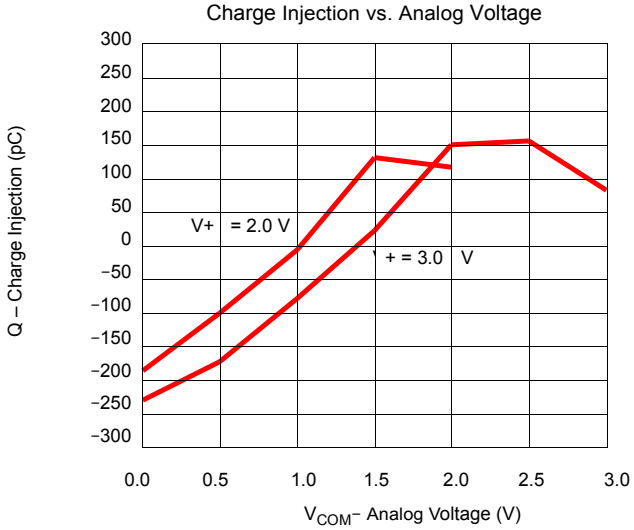
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage



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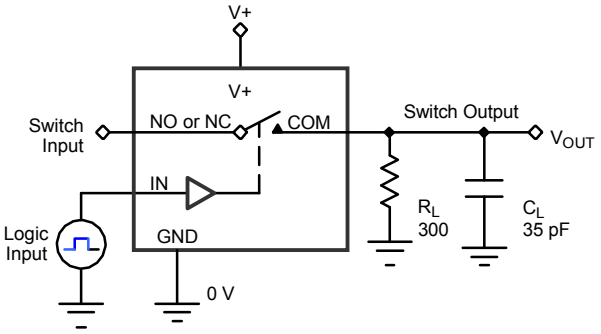
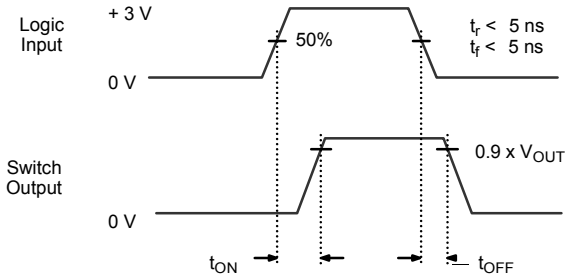
Test Circuits



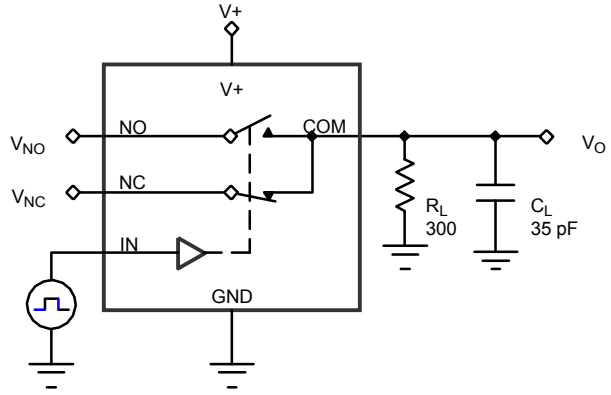
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

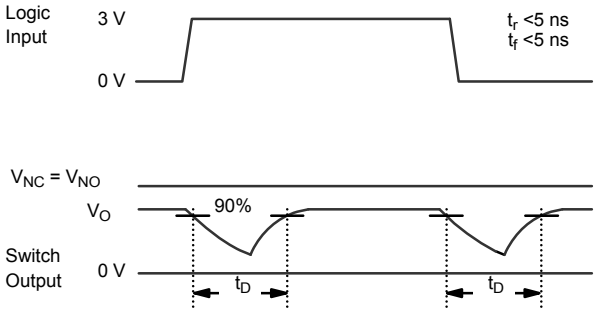
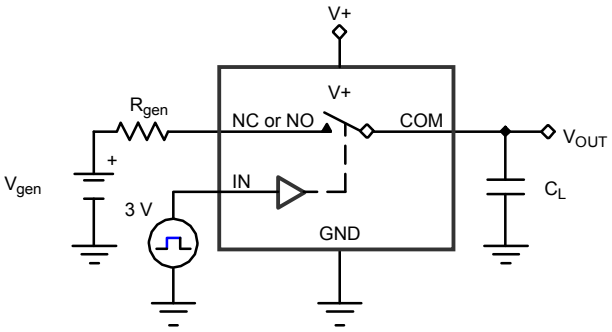
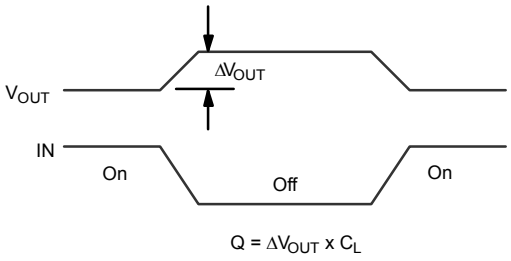


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

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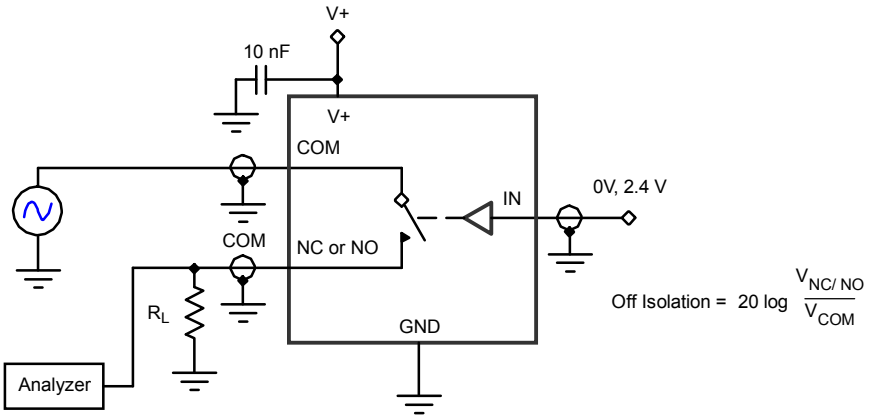

Figure 4. Off-Isolation

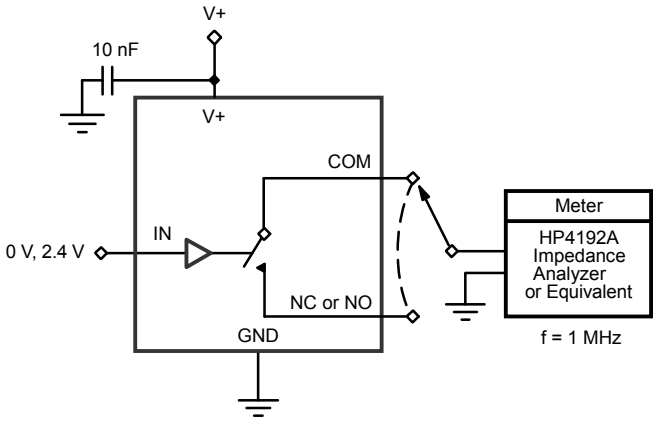

Figure 5. Channel Off/On Capacitance

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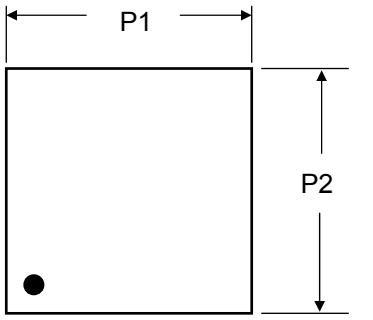
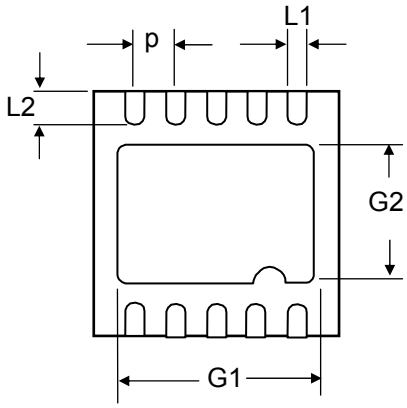
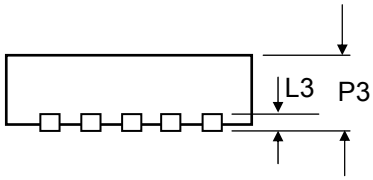
Package Outline and Dimensions DFN-10



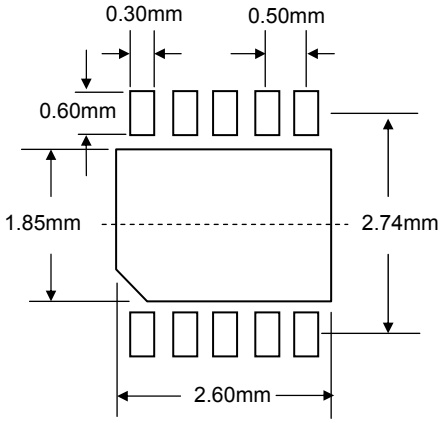
TOP VIEW



BOTTOM VIEW



SIDE VIEW

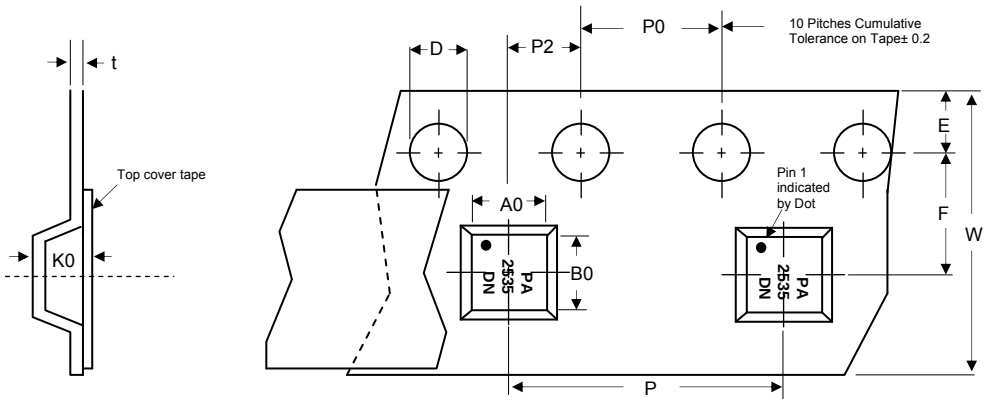


Recommended Land Pattern

Dim	MILLIMETERS		
	MIN	TYP	MAX
P1	2.95	3.00	3.05
P2	2.95	3.00	3.05
P3	0.80	0.85	0.85
L1	0.23	0.25	0.27
L2	0.35	0.40	0.45
L3	0.02	0.02	0.02
p	0.50	0.50	0.50
G1	2.35	2.40	2.45
G2	1.65	1.75	1.75

Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7”)	3.00±0.10	3.00±0.10	1.13±0.10	1.50±0.10	1.75±0.10	5.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	8.00±0.10	0.25
330(13”)	3.00±0.10	3.00±0.10	1.13±0.10	1.50±0.10	1.75±0.10	5.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	8.00±0.10	0.25



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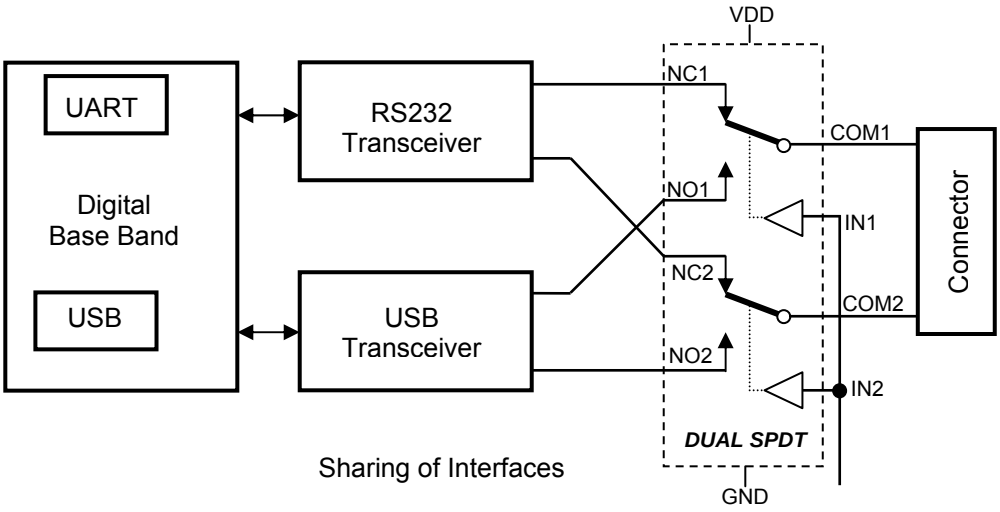
Typical Application



Sharing of Interfaces

Life Support Policy

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