

NCP511

150 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP511 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent current. The NCP511 series features an ultra-low quiescent current of 40 μ A. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

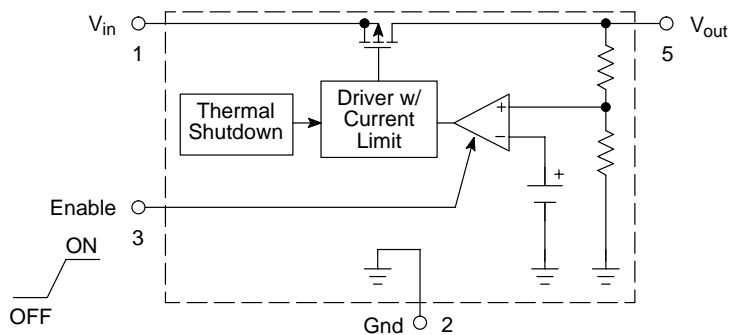
The NCP511 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 1.0 μ F. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are 1.5, 1.8, 2.7, 2.8, 3.0, 3.3, and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Low Quiescent Current of 40 μ A Typical
- Low Dropout Voltage of 100 mV at 100 mA
- Excellent Line and Load Regulation
- Maximum Operating Voltage of 6.0 V
- Low Output Voltage Option
- High Accuracy Output Voltage of 2.0%
- Industrial Temperature Range of -40°C to 85°C

Typical Applications

- Cellular Phones
- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras



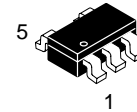
This device contains 82 active transistors

Figure 1. Representative Block Diagram



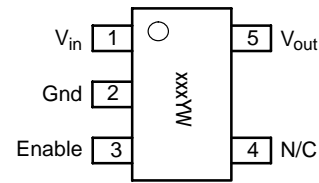
ON Semiconductor®

<http://onsemi.com>



TSOP-5
(SOT23-5, SC59-5)
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM



xxx = Version
Y = Year
W = Work Week

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Vin	Positive power supply input voltage.
2	Gnd	Power supply ground.
3	Enable	This input is used to place the device into low-power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to Vin.
4	N/C	No internal connection.
5	Vout	Regulated output voltage.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	0 to 6.0	V
Enable Voltage	Enable	-0.3 to $V_{in} + 0.3$	V
Output Voltage	V_{out}	-0.3 to $V_{in} + 0.3$	V
Power Dissipation and Thermal Characteristics Power Dissipation Thermal Resistance, Junction to Ambient	P_D $R_{\theta JA}$	Internally Limited 250	W °C/W
Operating Junction Temperature	T_J	+125	°C
Operating Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +150	°C

1. This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability (85°C) ± 100 mA DC with trigger voltage.

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ELECTRICAL CHARACTERISTICS ($V_{in} = V_{out(nom.)} + 1.0\text{ V}$, $V_{enable} = V_{in}$, $C_{in} = 1.0\ \mu\text{F}$, $C_{out} = 1.0\ \mu\text{F}$, $T_J = 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_A = 25^\circ\text{C}$, $I_{out} = 1.0\text{ mA}$) 1.5 V 1.8 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V	V_{out}	1.455 1.746 2.646 2.744 2.94 3.234 4.900	1.5 1.8 2.7 2.8 3.0 3.3 5.0	1.545 1.854 2.754 2.856 3.06 3.366 5.100	V
Output Voltage ($T_A = -40^\circ\text{C}$ to 85°C , $I_{out} = 1.0\text{ mA}$) 1.5 V 1.8 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V	V_{out}	1.455 1.746 2.619 2.716 2.910 3.201 4.900	1.5 1.8 2.7 2.8 3.0 3.3 5.0	1.545 1.854 2.781 2.884 3.09 3.399 5.100	V
Line Regulation ($I_{out} = 10\text{ mA}$) 1.5 V–4.4 V ($V_{in} = V_{out(nom.)} + 1.0\text{ V}$ to 6.0 V) 4.5 V–5.0 V ($V_{in} = 5.5\text{ V}$ to 6.0 V)	Reg_{line}	– –	1.0 1.0	3.5 3.5	mV/V
Load Regulation ($I_{out} = 1.0\text{ mA}$ to 150 mA)	Reg_{load}	–	0.3	0.8	mV/mA
Output Current ($V_{out} = (V_{out}$ at $I_{out} = 150\text{ mA}) - 3\%$) 1.5 V–1.8 V ($V_{in} = 4.0\text{ V}$) 1.9 V–3.0 V ($V_{in} = 5.0\text{ V}$) 3.1 V–5.0 V ($V_{in} = 6.0\text{ V}$)	$I_{out(nom.)}$	150 150 150	– – –	– – –	mA
Dropout Voltage ($I_{out} = 100\text{ mA}$, Measured at $V_{out} - 3.0\%$) 1.5 V 1.8 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V	$V_{in} - V_{out}$	– – – – – – –	245 160 100 100 100 90 75	350 200 200 200 200 200 200	mV
Quiescent Current (Enable Input = 0 V) (Enable Input = V_{in} , $I_{out} = 1.0\text{ mA}$ to $I_{O(nom.)}$)	I_Q	– –	0.1 40	1.0 100	μA
Output Voltage Temperature Coefficient	T_C	–	± 100	–	ppm/ $^\circ\text{C}$
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(en)}$	1.3 –	– –	– 0.3	V
Output Short Circuit Current ($V_{out} = 0\text{ V}$) 1.5 V–1.8 V ($V_{in} = 4.0\text{ V}$) 1.9 V–3.0 V ($V_{in} = 5.0\text{ V}$) 3.1 V–5.0 V ($V_{in} = 6.0\text{ V}$)	$I_{out(max)}$	200 200 200	400 400 400	800 800 800	mA
Ripple Rejection ($f = 1.0\text{ kHz}$, $I_O = 60\text{ mA}$)	RR	–	50	–	dB
Output Noise Voltage ($f = 20\text{ Hz}$ to 100 kHz , $I_{out} = 60\text{ mA}$)	V_n	–	110	–	μVrms

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_J(max) - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

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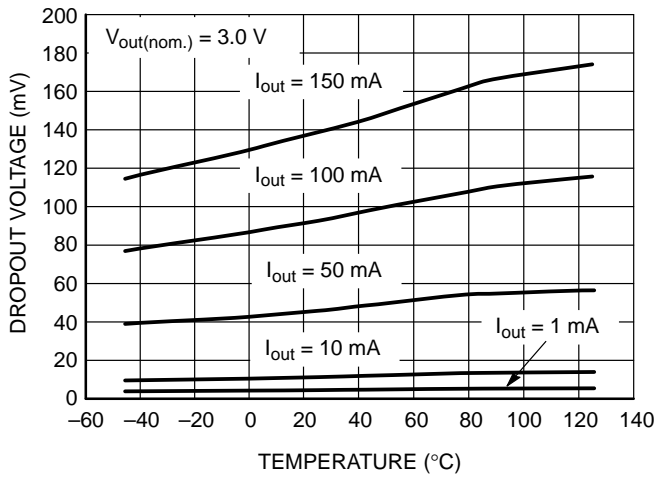


Figure 2. Dropout Voltage vs. Temperature

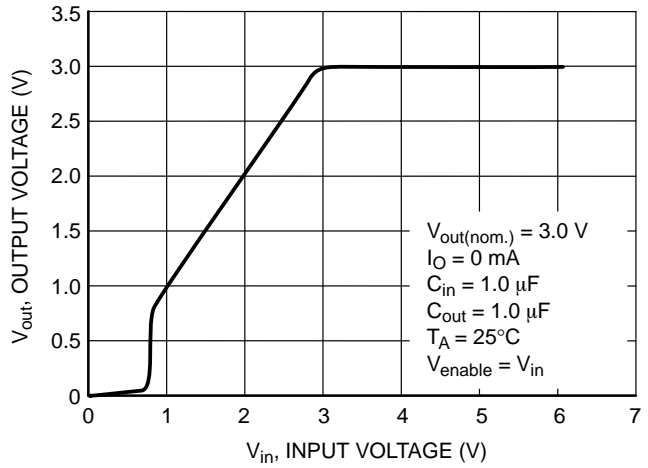


Figure 3. Output Voltage vs. Input Voltage

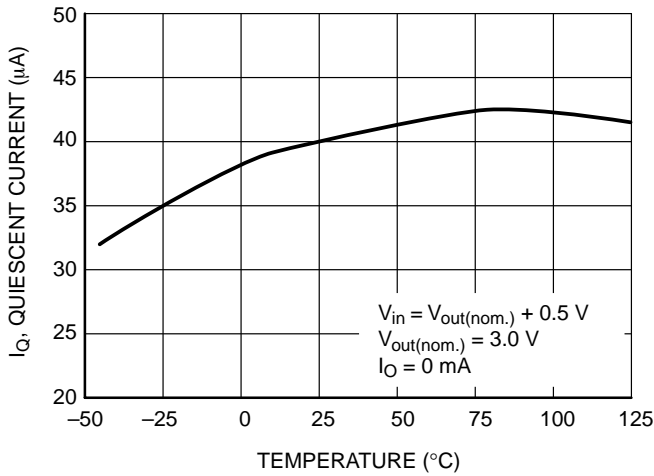


Figure 4. Quiescent Current vs. Temperature

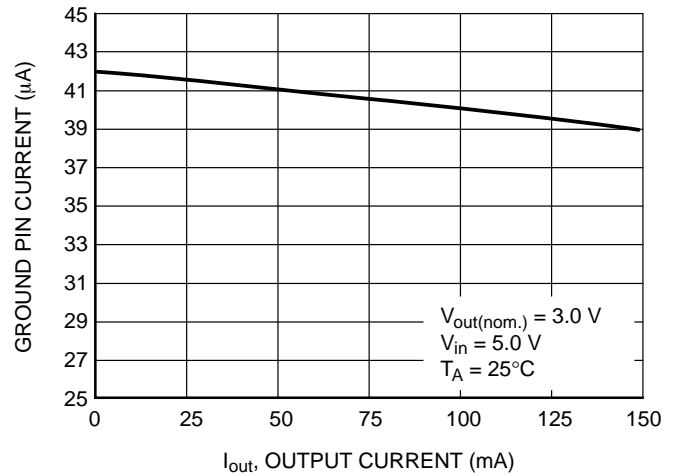


Figure 5. Ground Pin Current vs. Output Current

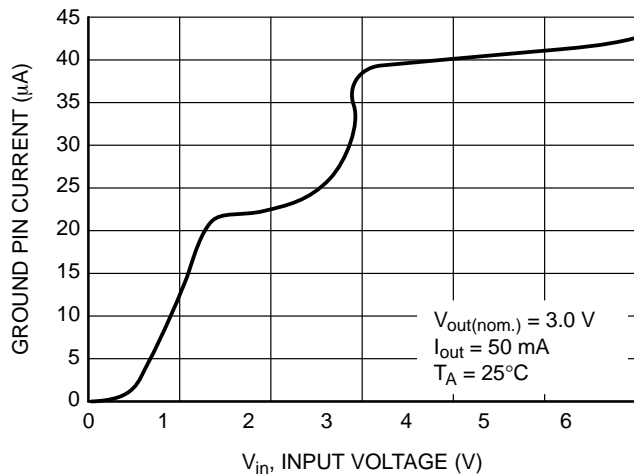


Figure 6. Ground Pin Current vs. Input Voltage

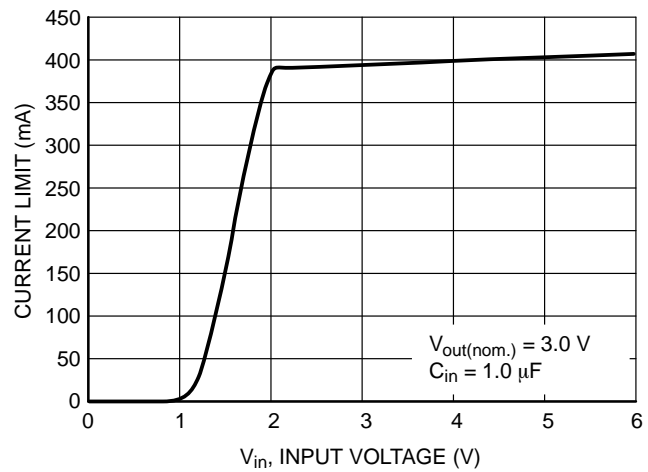


Figure 7. Current Limit vs. Input Voltage

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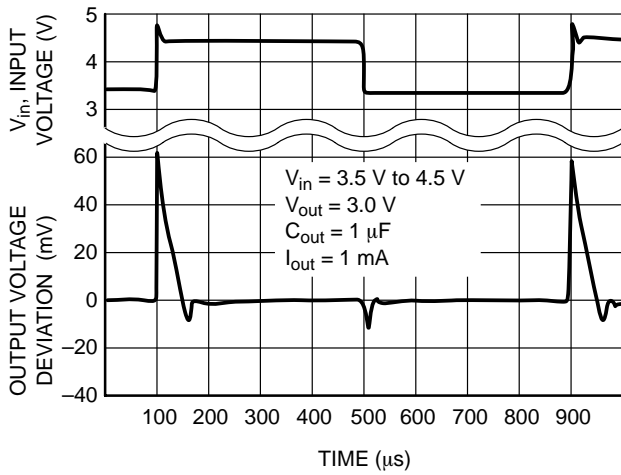


Figure 8. Line Transient Response

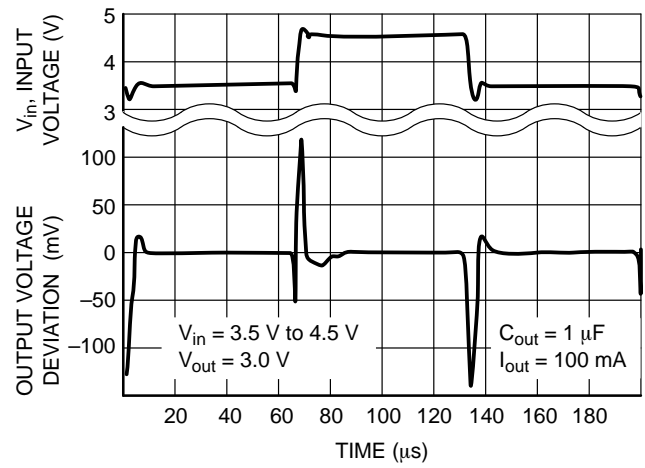


Figure 9. Line Transient Response

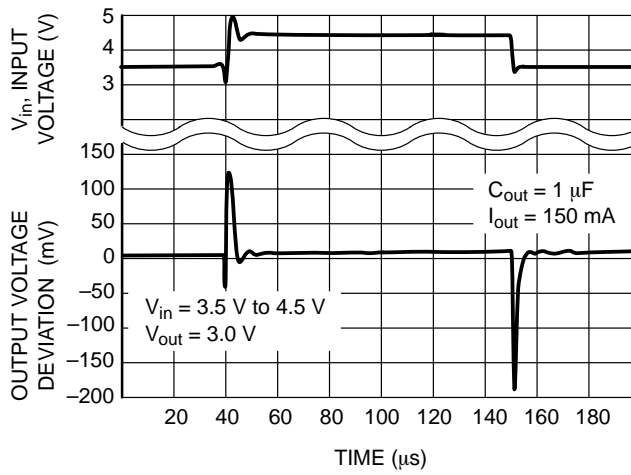


Figure 10. Line Transient Response

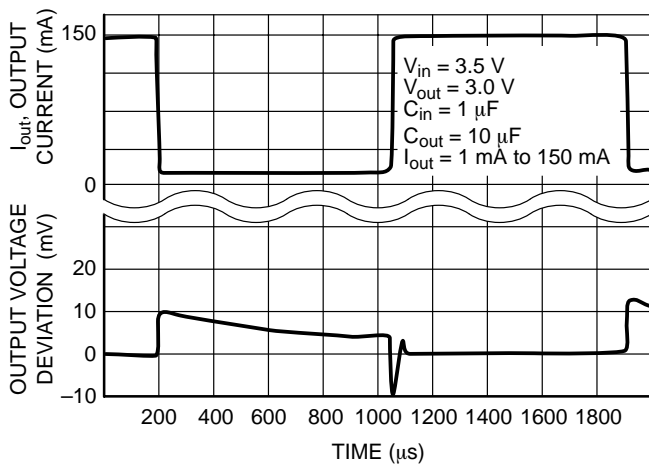


Figure 11. Load Transient Response

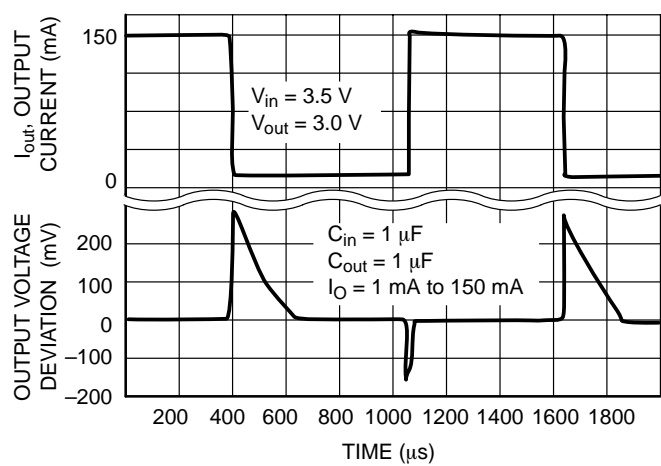


Figure 12. Load Transient Response

NCP511

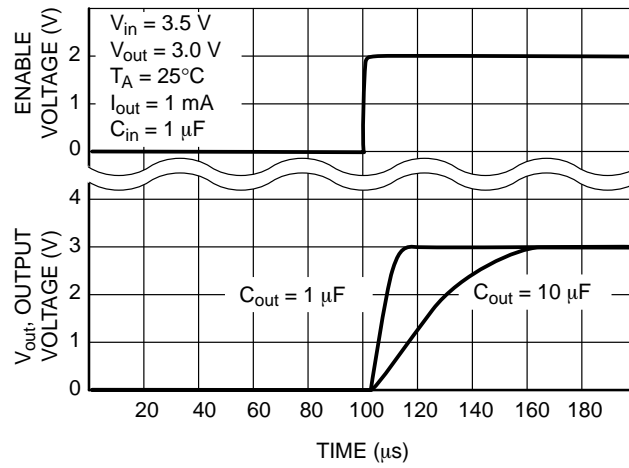


Figure 13. Turn-On Response

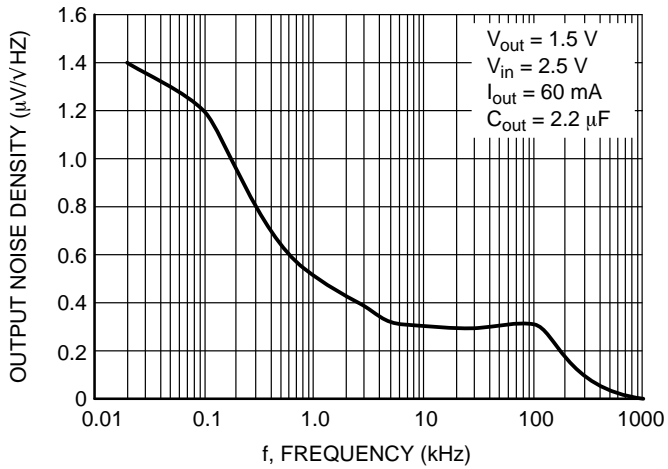


Figure 14. Output Noise Density

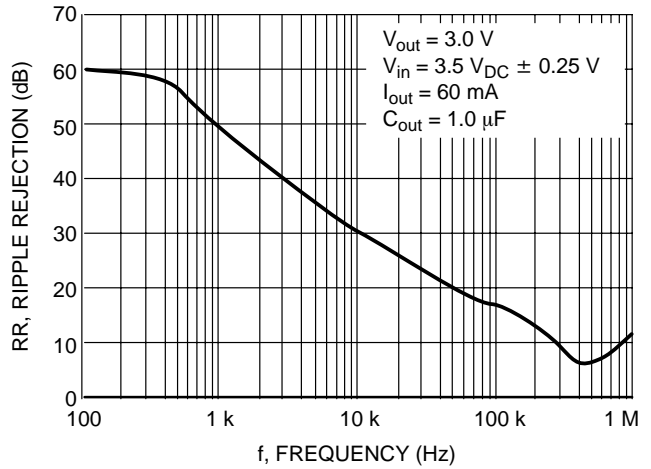


Figure 15. Ripple Rejection vs. Frequency

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

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APPLICATIONS INFORMATION

A typical application circuit for the NCP511 series is shown in Figure 16.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP511 package. Higher values and lower ESR will improve the overall line transient response.

Output Decoupling (C2)

The NCP511 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\text{m}\Omega$ up to 3.0Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in} .

Hints

Please be sure the V_{in} and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

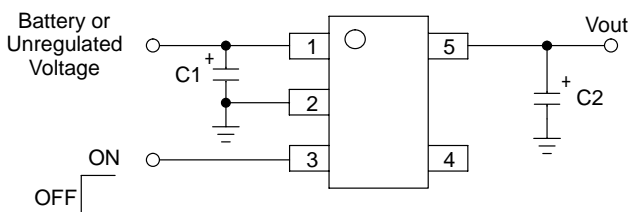


Figure 16. Typical Application Circuit

Thermal

As power across the NCP511 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP511 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C , then the NCP511 can dissipate up to 400 mW @ 25°C .

The power dissipated by the NCP511 can be calculated from the following equation:

$$P_{\text{tot}} = [V_{\text{in}} * I_{\text{gnd}}] + [V_{\text{in}} - V_{\text{out}}] * I_{\text{out}}$$

or

$$V_{\text{inMAX}} = \frac{P_{\text{tot}} + V_{\text{out}} * I_{\text{out}}}{I_{\text{gnd}} + I_{\text{out}}}$$

If a 150 mA output current is needed then the ground current from the data sheet is $40 \mu\text{A}$. For an NCP511SN30T1 (3.0 V), the maximum input voltage will then be 5.6 V.

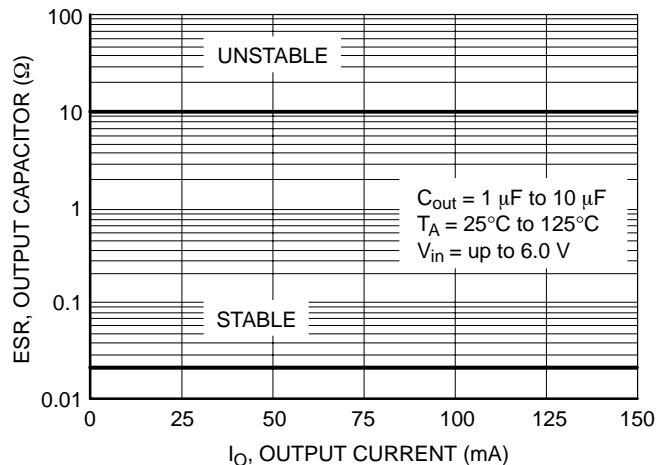


Figure 17. Output Capacitor vs. Output Current

APPLICATION CIRCUITS

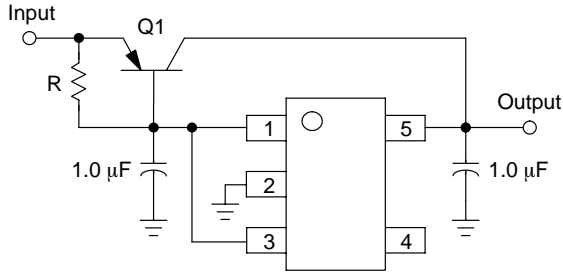


Figure 18. Current Boost Regulator

The NCP511 series can be current boosted with a PNP transistor. Resistor R in conjunction with V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by V_{BE} of the pass resistor.

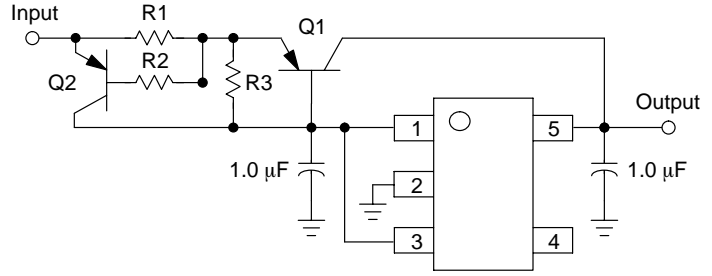


Figure 19. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the V_{BE} of Q2 and R1. $I_{SC} = ((V_{BEQ2} - i_b * R2) / R1) + I_{O(max)} \text{ Regulator}$

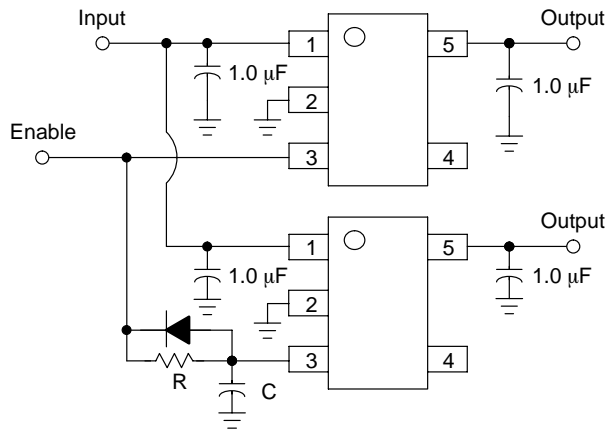


Figure 20. Delayed Turn-on

If a delayed turn-on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C, will delay the turn-on of the bottom regulator. A few values were chosen and the resulting delay can be seen in Figure 21.

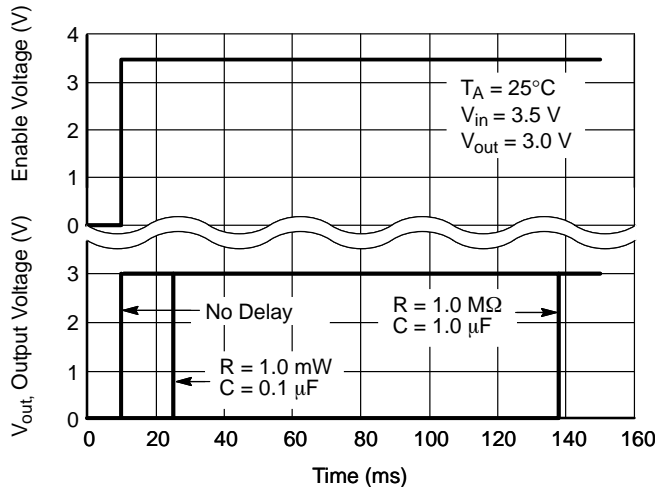


Figure 21. Delayed Turn-on

The graph shows the delay between the enable signal and output turn-on for various resistor and capacitor values.

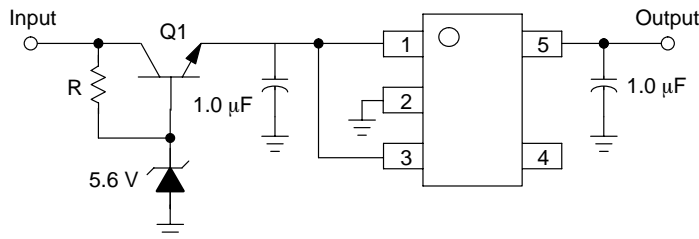


Figure 22. Input Voltages Greater than 6.0 V

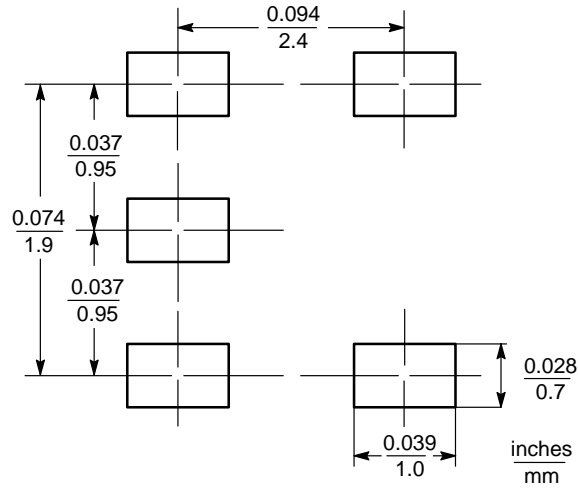
A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP511 series with the addition of a simple pre-regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output (V_{out}) is shorted to G_{nd} .

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MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP-5

(Footprint Compatible with SOT-23-5)

NCP511

ORDERING INFORMATION

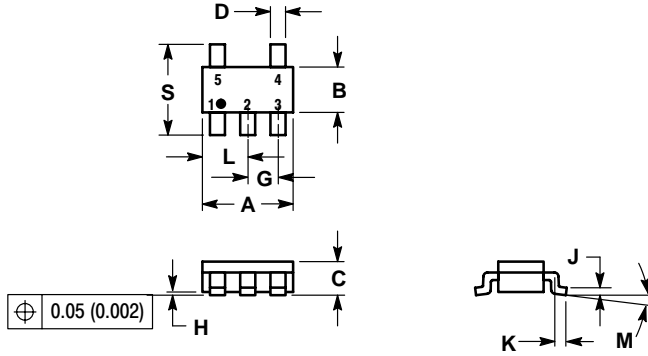
Device	Nominal Output Voltage	Marking	Package	Shipping
NCP511SN15T1	1.5	LBU	TSOP-5	3000 Units/ 7" Tape & Reel
NCP511SN18T1	1.8	LBV		
NCP511SN27T1	2.7	LBX		
NCP511SN28T1	2.8	LBY		
NCP511SN30T1	3.0	LBZ		
NCP511SN31T1	3.1	LFG		
NCP511SN33T1	3.3	LCA		
NCP511SN50T1	5.0	LCB		

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

NCP511

PACKAGE DIMENSIONS


TSOP-5
(SOT23-5, SC59-5)
SN SUFFIX
PLASTIC PACKAGE
CASE 483-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

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