1.8V CMOS 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

IDT74AUC16374

FEATURES:

- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.8V Optimized
- 0.8V to 2.7V Operating Range
- Inputs/outputs tolerant up to 3.6V
- Output drivers: ±9mA @ 2.3V
- Supports hot insertion
- Available in TSSOP, TVSOP, and VFBGA packages

APPLICATIONS:

- high performance, low voltage communications systems
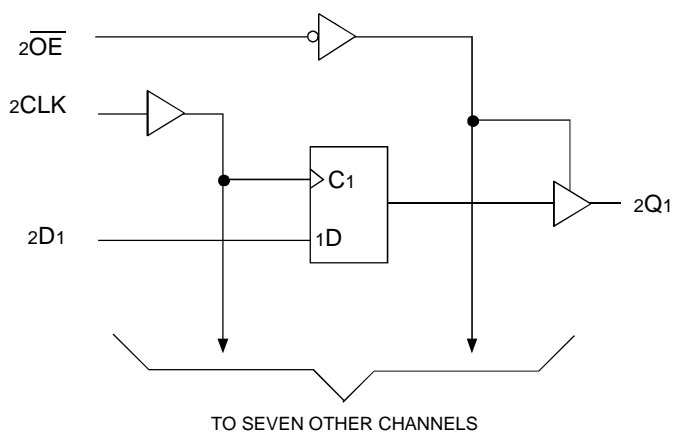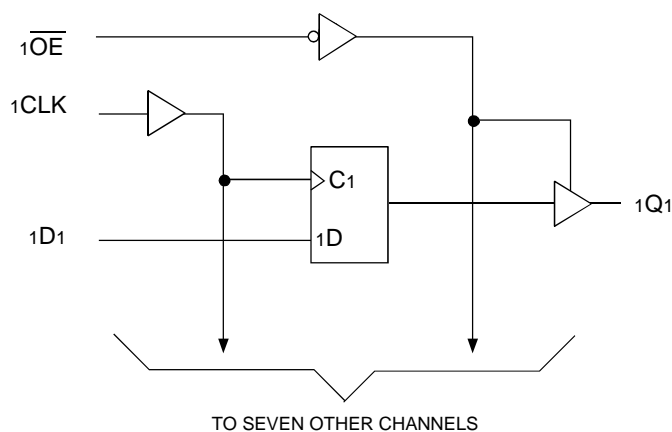- high performance, low voltage computing systems

DESCRIPTION:

This 16-bit edge-triggered D-type flip-flop is built using advanced CMOS technology. The AUC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

$\overline{OE}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{DD} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
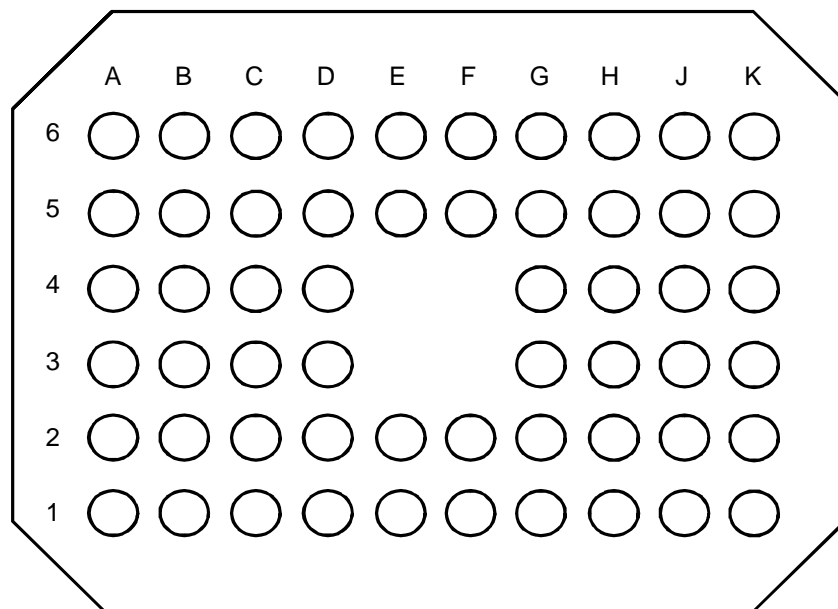
FUNCTIONAL BLOCK DIAGRAM

TO SEVEN OTHER CHANNELS

TO SEVEN OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

JANUARY 2003

DSC-6179/5

PINOUT CONFIGURATION

	A	B	C	D	E	F	G	H	J	K
6	1CLK	1D2	1D4	1D6	1D8	2D1	2D3	2D5	2D7	2CLK
5	NC	1D1	1D3	1D5	1D7	2D2	2D4	2D6	2D8	NC
4	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
3	NC	GND	V_{DD}	GND			GND	V_{DD}	GND	NC
2	NC	1Q1	1Q3	1Q5	1Q7	2Q2	2Q4	2Q6	2Q8	NC
1	1$\overline{OE}$	1Q2	1Q4	1Q6	1Q8	2Q1	2Q3	2Q5	2Q7	2$\overline{OE}$

VFBGA

NOTE:
NC = No Internal Connection

56 BALL VFBGA PACKAGE LAYOUT

TOP VIEW

PIN CONFIGURATION

$1\overline{OE}$	1	48	$1CLK$
$1Q_1$	2	47	$1D_1$
$1Q_2$	3	46	$1D_2$
GND	4	45	GND
$1Q_3$	5	44	$1D_3$
$1Q_4$	6	43	$1D_4$
V_{DD}	7	42	V_{DD}
$1Q_5$	8	41	$1D_5$
$1Q_6$	9	40	$1D_6$
GND	10	39	GND
$1Q_7$	11	38	$1D_7$
$1Q_8$	12	37	$1D_8$
$2Q_1$	13	36	$2D_1$
$2Q_2$	14	35	$2D_2$
GND	15	34	GND
$2Q_3$	16	33	$2D_3$
$2Q_4$	17	32	$2D_4$
V_{DD}	18	31	V_{DD}
$2Q_5$	19	30	$2D_5$
$2Q_6$	20	29	$2D_6$
GND	21	28	GND
$2Q_7$	22	27	$2D_7$
$2Q_8$	23	26	$2D_8$
$2\overline{OE}$	24	25	$2CLK$
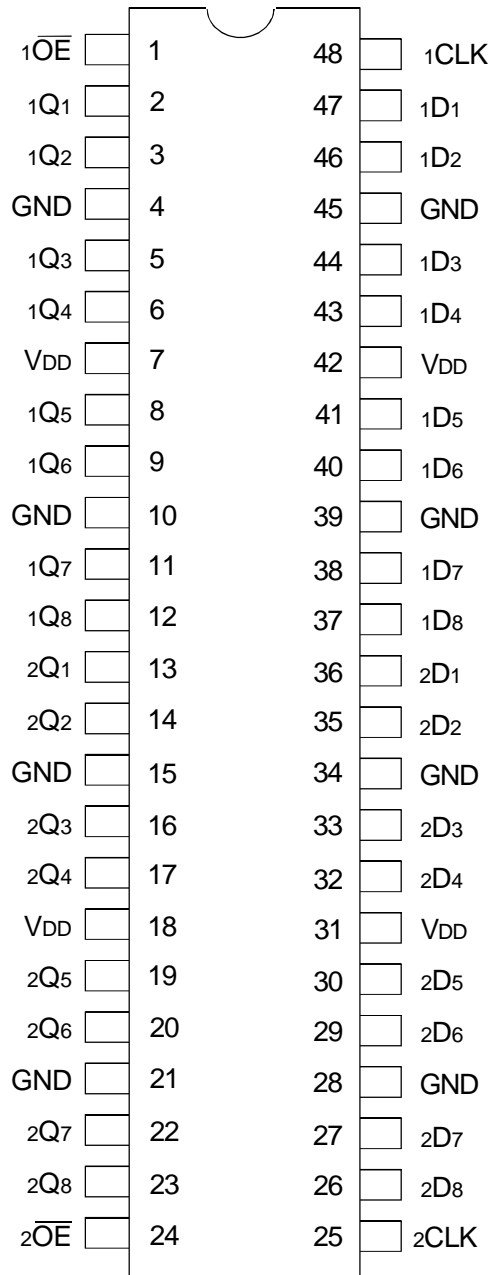
TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
$xCLK$	Clock Inputs
xQx	3-State Outputs
$x\overline{OE}$	3-State Output Enable Inputs (Active LOW)

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}	Terminal Voltage with Respect to GND (all input and V_{DD} terminals)	–0.5 to +3.6	V
V_{TERM}	Terminal Voltage with Respect to GND (any I/O or Output terminals in high-impedance or power-off state)	–0.5 to +3.6	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Continuous DC Output Current	±20	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$, or $V_I > V_{DD}$	±50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	–50	mA
I_{DD} I_{SS}	Continuous Current through each V_{DD} or GND	±100	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE $(T_A = +25°C, F = 1.0 MHz, V_{DD} = 2.5V)$

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}[1]	Input Capacitance	$V_{IN} = 0V$	3		pF
C_{OUT}[2]	Output Capacitance	$V_{OUT} = 0V$	5		pF
C_I[3]	Input Port Capacitance	$V_{IN} = 0V$	3		pF

NOTES:
1. Applies to Control Inputs.
2. Applies to Data Outputs.
3. Applies to Data Inputs.

FUNCTION TABLE (EACH FLIP-FLOP)[1]

Inputs			Output
$x\overline{OE}$	$xCLK$	xDx	xQx
L	↑	H	H
L	↑	L	L
L	H or L	X	Q[2]
H	X	X	Z

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Level of Q before the indicated steady-state conditions were established.

RECOMMENDED OPERATING CHARACTERISTICS[1]

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		0.8	2.7	V
V_{IH}	Input HIGH Voltage Level	V_{DD} = 0.8V	V_{DD}	—	V
		V_{DD} = 1.1V to 1.3V	0.65 x V_{DD}	—	
		V_{DD} = 1.4V to 1.6V	0.65 x V_{DD}	—	
		V_{DD} = 1.65V to 1.95V	0.65 x V_{DD}	—	
		V_{DD} = 2.3V to 2.7V	1.7	—	
V_{IL}	Input LOW Voltage Level	V_{DD} = 0.8V	—	0	V
		V_{DD} = 1.1V to 1.3V	—	0.35 x V_{DD}	
		V_{DD} = 1.4V to 1.6V	—	0.35 x V_{DD}	
		V_{DD} = 1.65V to 1.95V	—	0.35 x V_{DD}	
		V_{DD} = 2.3V to 2.7V	—	0.7	
V_I	Input Voltage		0	2.7	V
V_O	Output Voltage	Active State	0	V_{DD}	V
		3-State	0	2.7	
I_{OH}	HIGH Level Output Current	V_{DD} = 0.8V	—	–0.7	mA
		V_{DD} = 1.1V	—	–3	
		V_{DD} = 1.4V	—	–5	
		V_{DD} = 1.65V	—	–8	
		V_{DD} = 2.3V	—	–9	
I_{OL}	LOW Level Output Current	V_{DD} = 0.8V	—	0.7	mA
		V_{DD} = 1.1V	—	3	
		V_{DD} = 1.4V	—	5	
		V_{DD} = 1.65V	—	8	
		V_{DD} = 2.3V	—	9	
$\Delta t/\Delta v$	Input Transition Rise or Fall Time		—	20	ns/V
T_A	Operating Free-Air Temperature		–40	+85	°C

NOTE:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE[1]

Following Conditions Apply Unless Otherwise Specified:
Operating Conditions: T_A = –40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{IH} I_{IL}	Input HIGH or LOW Current All Inputs	V_{DD} = 2.7V, V_I = V_{DD} or GND		—	—	±5	µA
I_{OFF}	Input/Output Power Off Leakage	V_{DD} = 0V, V_{IN} or V_O ≤ 2.7V		—	—	±10	µA
I_{OZH}	High Impedance Output Current	V_{DD} = 2.7V	V_O = V_{DD}	—	—	±10	µA
I_{OZL}	(3-State Output Pins)		V_O = GND	—	—	±10	
I_{DDL} I_{DDH} I_{DDZ}	Quiescent Power Supply Current	V_{DD} = 0.8V to 2.7V V_{IN} = GND or V_{DD}		—	—	20	µA

NOTE:
1. All unused inputs of the device must be held at V_{DD} or GND to ensure proper operation.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = –100µA	V_{DD} - 0.1	—	—	V
		V_{DD} = 0.8V	I_{OH} = –0.7mA	—	0.55	—	
		V_{DD} = 1.1V[2]	I_{OH} = –3mA	0.8	—	—	
		V_{DD} = 1.4V[3]	I_{OH} = –5mA	1	—	—	
		V_{DD} = 1.65V[4]	I_{OH} = –8mA	1.2	—	—	
		V_{DD} = 2.3V[5]	I_{OH} = –9mA	1.8	—	—	
V_{OL}	Output LOW Voltage	V_{DD} = 0.8V - 2.7V	I_{OH} = 100µA	—	—	0.2	V
		V_{DD} = 0.8V	I_{OL} = 0.7mA	—	0.25	—	
		V_{DD} = 1.1V[2]	I_{OL} = 3mA	—	—	0.3	
		V_{DD} = 1.4V[3]	I_{OL} = 5mA	—	—	0.4	
		V_{DD} = 1.65V[4]	I_{OL} = 8mA	—	—	0.45	
		V_{DD} = 2.3V[5]	I_{OH} = 9mA	—	—	0.6	

NOTES:

1. V_{IL} and V_{IH} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS table for the appropriate V_{DD} range. T_A = -40°C to +85°C.
2. Demonstrates operation for nominal V_{DD} = 1.2V.
3. Demonstrates operation for nominal V_{DD} = 1.5V.
4. Demonstrates operation for nominal V_{DD} = 1.8V.
5. Demonstrates operation for nominal V_{DD} = 2.5V.

OPERATING CHARACTERISTICS, T_A = 25°C[1]

Symbol	Parameter	Test Conditions	V_{DD} = 0.8V	V_{DD} = 1.2V	V_{DD} = 1.5V	V_{DD} = 1.8V	V_{DD} = 2.5V	Unit
C_{PD} (each output)	Power Dissipation Capacitance[2] Outputs Enabled, 1 Output Switching	1 f_{DATA} = 5MHz 1 f_{CLK} = 10MHz 1 f_{OUT} = 5MHz $\overline{OE}$ = GND, C_L = 0pF	24	24	24.1	26.2	31.2	pF
$C_{PD(Z)}$	Power Dissipation Capacitance Outputs Disabled, 1 Clock and 1 Data Switching	1 f_{DATA} = 5MHz 1 f_{CLK} = 10MHz f_{OUT} = not switching $\overline{OE}$ = V_{DD}, C_L = 0pF	7.5	7.5	8	9.4	13.2	pF
C_{PD} (each clock)	Power Dissipation Capacitance[3] Outputs Disabled, Clock Only Switching	1 f_{DATA} = 0MHz 1 f_{CLK} = 10MHz f_{OUT} = not switching $\overline{OE}$ = V_{DD}, C_L = 0pF	13.8	13.8	14	14.7	17.5	pF

NOTES:

1. Total device C_{PD} for multiple (x) outputs switching and (n) clocks inputs switching = {x * C_{PD} (each output)} + {n C_{PD} (each clock)}.
2. C_{PD} (each output). This is the C_{PD} for each data bit where each input and output circuit is operating at 5MHz. The clock frequency is 10MHz and the numbers shown are minus the I_{DD} component.
3. C_{PD} (each clock); this is the C_{PD} for each clock circuit, operating at 10MHz.

SWITCHING CHARACTERISTICS[1]

| Symbol	Parameter	V_{DD} = 0.8V	V_{DD} = 1.2V±0.1V		V_{DD} = 1.5V±0.1V		V_{DD} = 1.8V±0.15V			V_{DD} = 2.5V±0.2V		Unit
		Typ.	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
f_{MAX}		85	—	250	—	250	—	—	250	—	250	MHz
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.7	2.2	ns
f_{CLOCK}	Clock Frequency	85	250	—	250	—	250	—	—	250	—	MHz
t_{SU}	Set-up Time, Data before CLK↑	1.4	1	—	1	—	1	—	—	1	—	ns
t_H	Hold Time, Data after CLK↑	0.1	0.9	—	0.9	—	0.9	—	—	0.9	—	ns
t_W	Pulse Duration, CLK HIGH or LOW	5.9	1.9	—	1.9	—	1.9	—	—	1.9	—	ns

NOTE:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = -40°C to +85°C.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS[1]

Symbol	V_{DD} = 0.8V	V_{DD} = 1.2V±0.1V	V_{DD} = 1.5V±0.1V	V_{DD} = 1.8V±0.15V	V_{DD} = 2.5V±0.2V	Unit
V_{LOAD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	2xV_{DD}	V
V_T	V_{DD}/2	V_{DD}/2	V_{DD}/2	V_{DD}/2	V_{DD}/2	V
V_{LZ}	100	100	100	150	150	mV
V_{HZ}	100	100	100	150	150	mV
R_L	2	2	2	1	0.5	KΩ
C_L	15	15	15	30	30	pF
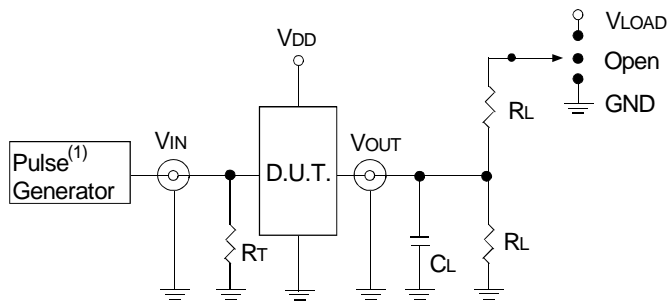
Test Circuits for All Outputs

DEFINITIONS:
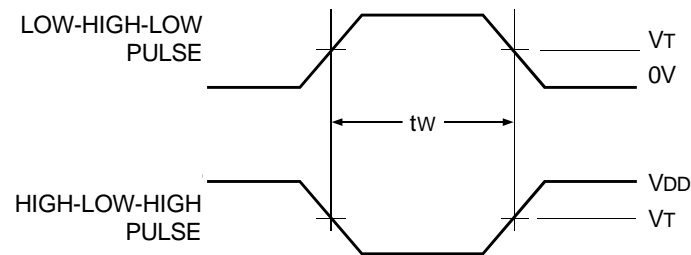C_L = Load capacitance: includes jig and probe capacitance.
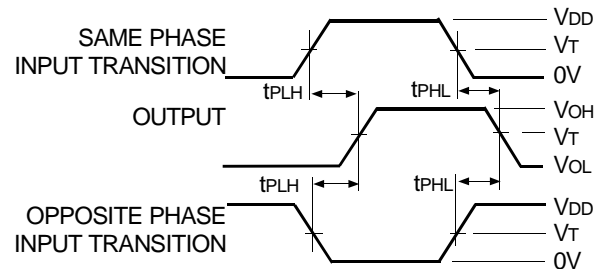R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
NOTE:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; slew rate ≥ 1V/ns.
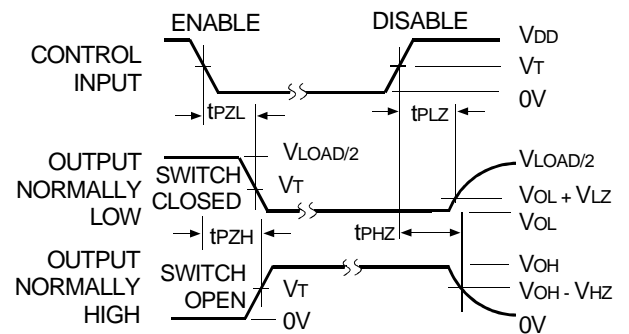
SWITCH POSITION

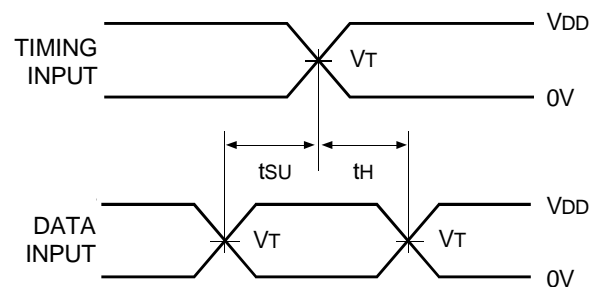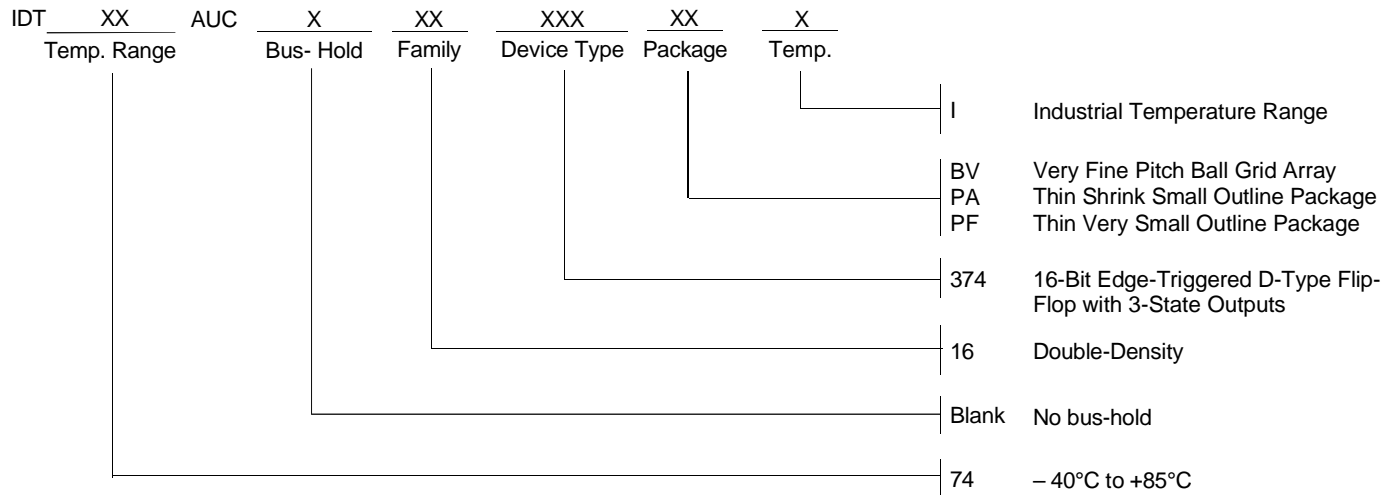| Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other Tests	Open

Pulse Width

Propagation Delay

NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

Setup and Hold Times

ORDERING INFORMATION

IDT   XX   AUC   X   XX   XXX   XX   X

Temp. Range   Bus- Hold   Family   Device Type   Package   Temp.

I	Industrial Temperature Range
BV	Very Fine Pitch Ball Grid Array
PA	Thin Shrink Small Outline Package
PF	Thin Very Small Outline Package
374	16-Bit Edge-Triggered D-Type Flip-Flop with 3-State Outputs
16	Double-Density
Blank	No bus-hold
74	– 40°C to +85°C