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TDA9106

LOW COST DEFLECTION PROCESSOR FOR MULTISYNC MONITORS

HORIZONTAL
- SELF-ADAPTATIVE
- DUAL PLL CONCEPT
- 150kHz MAXIMUM FREQUENCY
- X-RAY PROTECTION INPUT
- I^2C CONTROLS : HORIZONTAL DUTY-CYCLE, H-POSITION, FREE RUNNING FREQUENCY, FREQUENCY GENERATOR FOR BURN-IN MODE

VERTICAL
- VERTICAL RAMP GENERATOR
- 50 TO 165Hz AGC LOOP
- GEOMETRY TRACKING WITH V-POS & AMP
- I^2C CONTROLS :
  V-AMP, V-POS, S-CORR, C-CORR

I^2C GEOMETRY CORRECTIONS
- VERTICAL PARABOLA GENERATOR (Pincushion, Keystone, Corner Correction, Top/bottom Corner Correction Balance)
- HORIZONTAL DYNAMIC PHASE (Side Pin Balance & Parallelogram)
- HORIZONTAL AND VERTICAL DYNAMIC FOCUS (Horizontal Focus Amplitude, Horizontal Focus Symmetry)

GENERAL
- SYNC PROCESSOR
- HOR. & VERT. SYNC OUTPUT FOR MCU
- HOR. & VERT. BLANKING OUTPUTS
- 12V SUPPLY VOLTAGE
- 8V REFERENCE VOLTAGE
- HOR. & VERT. LOCK UNLOCK OUTPUTS
- READ/WRITE I^2C INTERFACE
- HORIZONTAL MOIRE OR DAC OUTPUT

DESCRIPTION

The TDA9106 is a monolithic integrated circuit assembled in 42 pins shrunk dual in line plastic package. This IC controls all the functions related to the horizontal and vertical deflection in multimodes or multi-frequency computer display monitors.

The internal sync processor, combined with the very powerful geometry correction block are making the TDA9106 suitable for very high performance monitors with very few external components.

It is particularly well suited for high-end 15" and 17" monitors.

Combined with ST7275 Microcontroller family, TDA9206 (Video preamplifier) and STV942x (On-Screen Display controller) the TDA9106 allows to built fully I^2C bus controlled computer display monitors, thus reducing the number of external components to a minimum value.

SHRINK42
(Plastic Package)
ORDER CODE : TDA9106
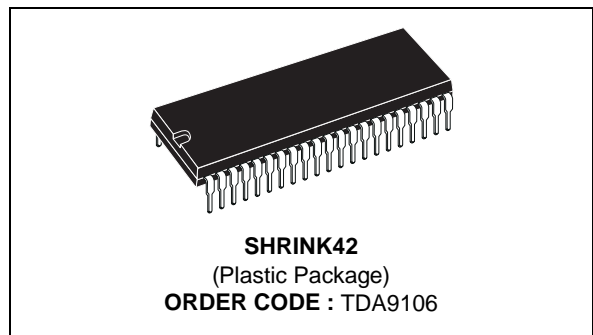
PIN CONNECTIONS

S/G	1	42	GND
MOIRE	2	41	SDA
PLL1INHIB	3	40	SCL
PLL2C	4	39	5V
HREF	5	38	H/HVIN
HFLY	6	37	HLOCKOUT
HGND	7	36	HOUT
FC2	8	35	VSYNCOUT
FC1	9	34	TEST
C0	10	33	VSYNCIN
R0	11	32	VFOCUS
PLL1F	12	31	EWOUT
HLOCKCAP	13	30	VFLY
HPOS	14	29	VOUT
XRAY	15	28	VDCOUT
HFOCUSCAP	16	27	VCAP
HFOCUS	17	26	V_{REF}
V_{CC}	18	25	VAGCCAP
GND	19	24	VGND
HOUTEM	20	23	VBLKOUT
HOUTCOL	21	22	HBLKOUT

PIN CONNECTIONS

Pin	Name	Function
1	S/G	Sync on green input
2	MOIRE	Moire output
3	PLL1 INHIB	TTL-Compatible input for PLL1 inhibition
4	PLL2C	Second PLL Loop Filter
5	HREF	Horizontal Section Reference Voltage (to filter)
6	HFLY	Horizontal Flyback Input (positive polarity)
7	HGND	Horizontal Section Ground
8	FC2	VCO Low Threshold filtering Capacitor
9	FC1	VCO High Threshold filtering Capacitor
10	C0	Horizontal Oscillator Capacitor
11	R0	Horizontal Oscillator Resistor
12	PLL1F	First PLL Loop Filter
13	HLOCKCAP	First PLL Lock/Unlock Time Constant Capacitor
14	HPOS	Horizontal Centering Output (to filter)
15	XRAY	X-RAY protection input (with internal latch function)
16	HFOCUSCAP	Horizontal Dynamic Focus Oscillator Capacitor
17	HFOCUS	Horizontal Dynamic Focus Output
18	V_{CC}	Supply Voltage (12V Typ)
19	GND	General Ground (related to V_{CC})
20	HOUTEM	Horizontal Drive Output (internal transistor emitter)
21	HOUTCOL	Horizontal Drive Output (int. trans. open collector)
22	HBLKOUT	Horizontal Blanking Output (see activation table)
23	VBLKOUT	Vertical Blanking Output (see activation table)
24	VGND	Vertical Section Ground
25	VAGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
26	V_{REF}	Vertical Section Reference Voltage (to filter)
27	VCAP	Vertical Sawtooth Generator Capacitor
28	V_{DCOUT}	Vertical Position Reference Voltage Output
29	VOUT	Vertical Ramp Output (with frequency independant amplitude and S or C Corrections if any)
30	VFLY	Vertical Flyback Input (positive polarity)
31	EWOUT	East/West Pincushion Correction Parabola Output (with Corner corrections if any)
32	VFOCUS	Vertical Dynamic Focus Output
33	VSYNCIN	TTL-compatible Vertical Sync Input (for separated H&V)
34	TEST	Not to be used - Test pin
35	VSYNCOUT	TTL Vertical Sync Output (Extracted VSYNC in case of S/G or TTL Composite HV Inputs)
36	HOUT	TTL Horizontal Sync Output (To be used for frequency measurement)
37	HLOCKOUT	First PLL Lock/Unlock Output (5V unlocked - 0V locked)
38	H/HVIN	TTL-compatible Horizontal Sync Input
39	5V	Supply Voltage (5V Typ.)
40	SCL	I^2C-Clock input
41	SDA	I^2C-Data input
42	GND	Ground (Related to 5V)

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QUICK REFERENCE DATA

Parameter	Value	Unit
Horizontal Frequency	15 to 150	kHz
Autosynch Frequency (for given R0 and C0)	1 to 4.5	FH
± Horizontal Sync Polarity Input	YES	
Polarity Detection (on both Horizontal and Vertical Sections)	YES	
TTL Composite Synch or Sync on Green	YES	
Lock/Unlock Identification (on both Horizontal 1st PLL and Vertical Section)	YES	
I^2C Control for H-Position	± 10	%
XRay Protection	YES	
I^2C Horizontal Duty Adjust	30 to 60	%
I^2C Free Running Adjustment	0.8 to 1.3	F0
Stand-by Function	YES	
Two Polarities H-Drive Outputs	YES	
Supply Voltage Monitoring	YES	
PLL1 Inhibition Possibility	YES	
Blanking Outputs (both Horizontal and Vertical)	YES	
Vertical Frequency	35 to 200	Hz
Vertical Autosync (for 150nF)	50 to 165	Hz
Vertical S-Correction	YES	
Vertical C-Correction	YES	
Vertical Amplitude Adjustment	YES	
Vertical Position Adjustment	YES	
East/West Parabola Output	YES	
Pin Cushion Correction Amplitude Adjustment	YES	
Keystone Adjustment	YES	
Corner and Corner Balance Adjustments	YES	
Internal Dynamic Horizontal Phase Control	YES	
Side Pin Balance Amplitude Adjustment	YES	
Parallelogram Adjustment	YES	
Tracking of Geometric Corrections	YES	
Reference Voltage (both on Horizontal and Vertical)	YES	
Dynamic Focus (both Horizontal and Vertical)	YES	
I^2C Horizontal Dynamic Focus Amplitude Adjustment	YES	
I^2C Horizontal Dynamic Focus Keystone Adjustment	YES	
Type of Input Sync Detection (supplied by 5V Digital Supply)	YES	
Horizontal Moiré Output	YES	
I^2C Controlled H-Moiré Amplitude	YES	
Frequency Generator for Burn-in	YES	
Fast I^2C Read/Write	400	kHz

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BLOCK DIAGRAM

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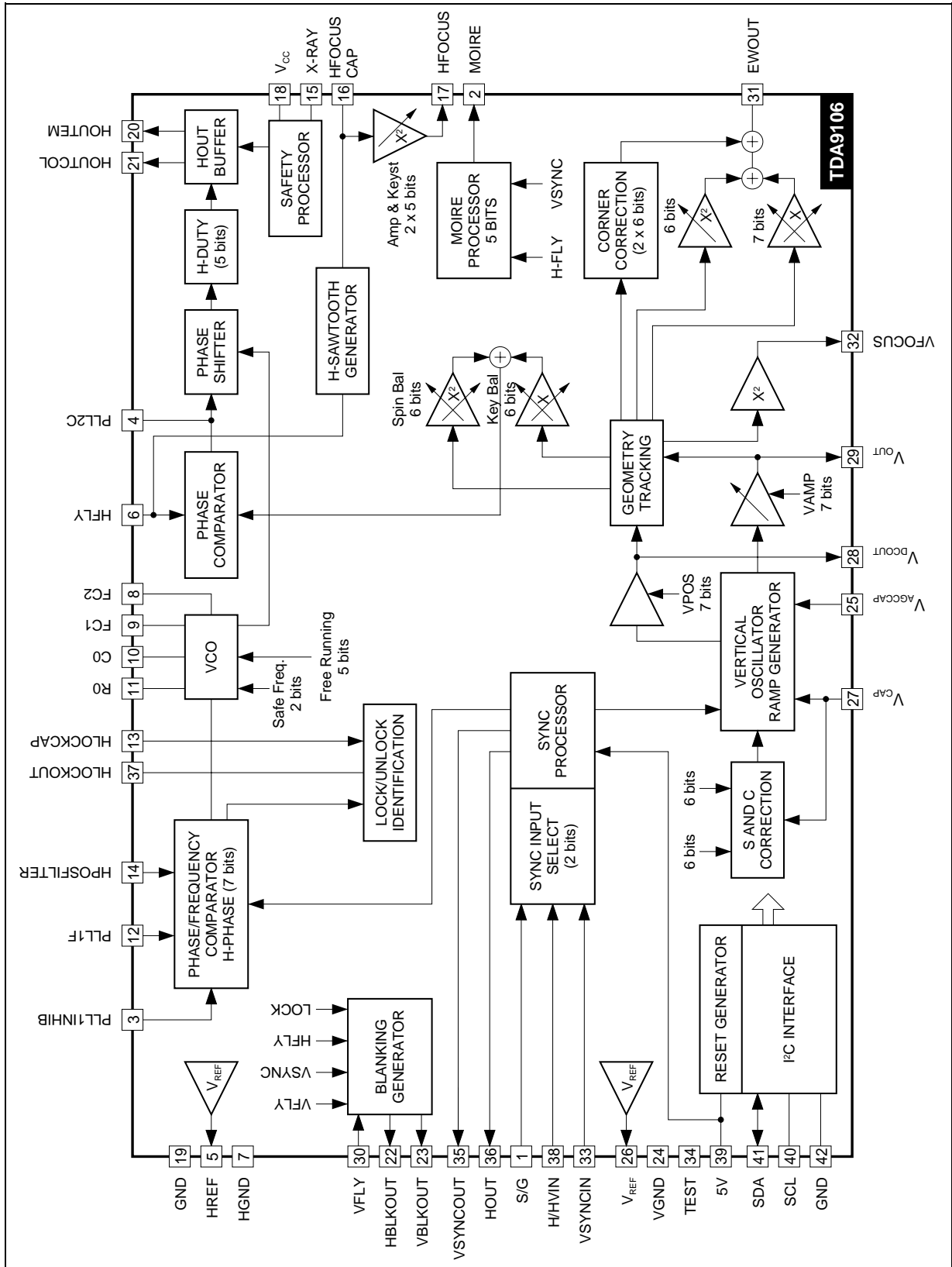
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 18)	13.5	V
V_{DD}	Supply Voltage (Pin 39)	5.7	V
V_{IN}	Max Voltage on Pin 6 Pins 15, 21, 22, 23 Pin 1 Pin 4 Pins 3, 33,34,37,38,40,41 Pin 16 Pins 8, 9, 10, 11, 12, 13, 14, 25, 27, 30	1.8 12 3.6 4 5 6 8	V V V V V V V
VESD	ESD susceptibility Human Body Model,100pF Discharge through 1.5kΩ EIAJ Norm,200pF Discharge through 0Ω	2 300	kV V
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	65	°C/W

SYNCHRO PROCESSOR
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HsVR	Horizontal Sync Input Voltage	Pin 38	0		5	V
MinD	Minimum Horizontal Input Pulses Duration	Pin 38	0.7			µs
Mduty	Maximum Horizontal Input Signal Duty Cycle	Pin 38			25	%
VsVR	Vertical Sync Input Voltage	Pin 33	0		5	V
VSW	Minimum Vertical Sync Pulse Width	Pin 33	5			µs
VSmD	Maximum Vertical Sync Input Duty Cycle	Pin 33			15	%
VextM	Maximum Vertical Sync Width on TTL H/Vcomposite or S/G	Pins 1, 38			750	µs

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VSGDC	S/G Clamped DC Level	Pin 1, I_1 = -1µA		1		V
ISGbias	Internal Diode Bias Current	Pin 1, V_1 = 1.6V		10		µA
VSGTh	Slicing Level (see application design choice)	Pin 1		0.2		V
VINTH	Horizontal and Vertical Input Voltage (Pins 33,38)	Low Level High Level	 2.2		0.8 	V V
RIN	Horizontal and Vertical Pull-Up Resistor	Pins 33,38		200		kΩ
VOut	Output Voltage (Pins 35,36,37)	Low level High Level		0 5		V V
TfrOut	Falling and Rising Output CMOS Buffer	Pins 35,36,37 Cout = 20pF		100		ns
VHlock	Horizontal 1st PLL Lock Output Status (Pin 37)	Locked Unlocked		0 5		V V
VoutT	Extracted Vsync Integration Time (% of TH) on H/V Composite or S/G	Pin 35, C0 = 820pF	26	35		%

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I^{2}C READ/WRITE
Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I^{2}C PROCESSOR						
Fscl	Maximum Clock Frequency	Pin 40	400			kHz
Tlow	Low period of the SCL Clock	Pin 40	1.3			µs
Thigh	High period of the SCL Clock	Pin 40	0.6			µs
Vinth	SDA and SCL Input Threshold	Pins 40,41		2.2		V
VACK	Acknowledge Output Voltage on SDA input with 3mA	Pin 41			0.4	V

See also I^{2}C Table Control and I2C Sub Address Control

HORIZONTAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VCO						
$R_{0(Min.)}$	Minimum Oscillator Resistor	Pin 11	6			kΩ
$C_{0(Min.)}$	Minimum Oscillator Capacitor	Pin 10	390			pF
$F_{(Max.)}$	Maximum Oscillator Frequency				150	kHz
OUTPUT SECTION						
I6m	Maximum Input Peak Current	Pin 6			2	mA
HOI1 HOI2	Horizontal Drive Output Maximum Current Pin 20 Pin 21	Sourced current Sunk current			20 20	mA mA

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage	Pin 18	10.8	12	13.2	V
V_{DD}	Supply Voltage	Pin 39	4.5	5	5.5	V
I_{CC}	Supply Current	Pin 18		50		mA
I_{DD}	Supply Current	Pin 39		5		mA
V_{REF-H}	Horizontal Reference Voltage	Pin 5, I = 5mA	7.4	8	8.6	V
V_{REF-V}	Vertical Reference Voltage	Pin 5, I = 5mA	7.4	8	8.6	V
I_{REF-H}	Max. Sourced Current on V_{REF-H}	Pin 5			5	mA
I_{REF-V}	Max. Sourced Current on V_{REF-V}	Pin 26			5	mA

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HORIZONTAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
1st PLL SECTION						
HpolT	Polarity Integration Delay		0.75			ms
V_{VCO}	VCO Control Voltage (Pin12)	V_{REF-H} = 8V f_0 f_H(Max.)		V_{REF-H} / 6 6.2		V V
Vcog	VCO Gain (Pin 12)	R_0 = 6.49kΩ, C_0 = 820pF, dF/dV = 1/11R_0C_0		17		kHz/V
Hph	Horizontal Phase Adjustment	% of Horizontal Period		±10		%
Hphmin Hphtyp Hphmax	Horizontal Phase Decoupling Output Minimum Value Typical Value Maximum Value	Sub-Address 01, Pin 14 Byte x1111111 Byte x1000000 Byte x0000000		2.8 3.4 4.0		V V V
f_0	Free Running Frequency	R_0 = 6.49kΩ, C_0 = 820pF, f_0 = 0.97/8R_0C_0		22.3		kHz
dF0/dT	Free Running Frequency Thermal Drift (No drift on external components)			-150		ppm/C
f_0(Min.) f_0(Max.)	Free Running Frequency Adjustment Minimum Value Maximum Value	Sub-Address 02 Byte xxx11111 Byte xxx00000		0.8 1.3		F0 F0
CR	PLL1 Capture Range	R_0 = 6.49kΩ, C_0 = 820pF, from f_0+0.5kHz to 4.5F_0 f_H(Min.) f_H(Max.)	100		23.5	kHz kHz
PLLinh	PLL1 Inhibition (Pin3)	Typ Threshold = 1.6V PLL ON PLL OFF	2		0.8	V V
SFF	Safe Forced Frequency SF1 Byte 11xxxxxx SF2 Byte 10xxxxxx	Sub-Address 02		2F0 3F0		
FC1 FC2	VCO Sawtooth Level High FC1=(4.V_{REF-H})/5 Low FC2=(V_{REF-H})/5	Pin 9 To filter Pin 8 To filter		6.4 1.6		V V
2nd PLL SECTION AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage (Pin 6)		0.65	0.75		V
Hjit	Horizontal Jitter (see Pins 8-9 filtering)			TBD		ppm
HDmin HDmax	Horizontal Drive Output Duty-Cycle (Pin 20 or 21) (see Note 1) Low Level High Level (see Note 2)	Sub-Address 00 Byte xxx11111 Byte xxx00000		30 60		% %
XRAYth	X-RAY Protection Input Threshold Voltage	Pin 15		8		V
Vphi2	Internal Clamping Levels on 2nd PLL Loop Filter (Pin 4)	Low Level High Level		1.6 4.0		V V
VSCinh	Threshold Voltage To Stop H-Out,V-Out when V_{CC} < VSCinh	Pin 18		7.5		V
IHblk	Maximum Horizontal Blanking Output Current	I_{22}			10	mA
VHblk	Horizontal Blanking Output Low Level (Blanking ON)	V_{22} with I_{22} = 10mA		0.25	0.5	V
HDvd HDem	Horizontal Drive Output Low Level (Pin 20 to GND) High Level (Pin 21 to V_{CC}=12V)	V_{21}-V_{20}, I_{OUT} = 20mA V_{20}, I_{OUT} = 20mA	9.5	1.1 10	1.7	V V

Notes : 1. Duty Cycle is the ratio of power transistor OFF time to period. Power transistor is OFF when output transistor is OFF.
2. Initial Condition for Safe Operation Start Up (Max. duty cycle).

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HORIZONTAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
\multicolumn{7}{l}{HORIZONTAL DYNAMIC FOCUS SECTION}
HDFst	Horizontal Dynamic Focus Sawtooth Minimum Level Maximum Level	HfocusCap = C_0 = 820pF, f_H = 90kHz, Pin 16		 2 4.7		 V V
HDFdis	Horizontal Dynamic Focus Sawtooth Discharge Width	Driven by Hfly		500		ns
HDFDC	Bottom DC Output Level	R_{LOAD} = 10kΩ, Pin 17		2		V
TDHDF	DC Output Voltage Thermal Drift			200		ppm/C
HDFamp	Horizontal Dynamic Focus Amplitude Min Byte xxx11111 Typ Byte xxx10000 Max Byte xxx00000	Sub-Address 03, Pin 17, f_H = 90kHz, Keystone Typ		 1 1.5 3		 V_{PP} V_{PP} V_{PP}
HDFKeyst	Horizontal Dynamic Focus Keystone Min A/B Byte xxx11111 Typ Byte xxx10000 Max A/B Byte xxx00000	Sub-Address 04, f_H = 90kHz, Typ Amp B/A A/B A/B		 3.5 1.0 3.5		

MOIRE OUTPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{MOIRE}	Minimum Output Resistor	Pin 2	2			kΩ
V_{MOIRE}	Output Voltage (moire off), Subaddress 0F Byte 0xx00000 Byte 0xx10000 Byte 0xx11111	Pin 2, R_{MOIRE} = 2kΩ		 0.2 1.1 2.0		 V V V

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VERTICAL SECTION
Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUTS SECTION						
VEWM	Maximum EW Output Voltage	Pin 31			6.5	V
VEWm	Minimum EW Output Voltage	Pin 31	1.8			V
VDFm	Minimum Vertical Dynamic Focus Output Voltage	Pin 32	1.8			V
R_{LOAD}	Minimum Load for less than 1% Vertical Amplitude Drift	Pin 25	65			MΩ

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL RAMP SECTION						
VRB	Voltage at Ramp Bottom Point	V_{REF-V}=8V, Pin 27		2		V
VRT	Voltage at Ramp Top Point (with Sync) V_{REF-V}	Pin 27		5		V
VRTF	Voltage at Ramp Top Point (without Sync)	Pin 27		VRT-0.1		V
VSTD	Vertical Sawtooth Discharge Time Duration (Pin 27)	With 150nF Cap		80		μs
VFRF	Vertical Free Running Frequency (see Notes 3 & 4)	$C_{OSC (Pin 27)}$ = 150nF Measured on Pin27,		100		Hz
ASFR	AUTO-SYNC Frequency	C_{27} = 150nF ±5% See Note 5	50		165	Hz
RAFD	Ramp Amplitude Drift Versus Frequency at Maximum Vertical Amplitude	C_{27} = 150nF 50Hz < f and f < 165Hz		200	TBD	ppm/Hz
Rlin	Ramp Linearity on Pin 27 (see Notes 3 & 4)	2.5 < V_{27} and V_{27} < 4.5V		0.5		%
Vpos	Vertical Position Adjustment Voltage (Pin28)	Sub Address 06 Byte x0000000 Byte x1000000 Byte x1111111	3.65	3.2 3.5 3.8	3.3	V V V
I_{VPOS}	Max Current on Vertical Position Output	Pin 28		±2		mA
VOR	Vertical Output Voltage (peak-to-peak on Pin 29)	Sub Address 05 Byte x0000000 Byte x1000000 Byte x1111111	3.5	2.25 3 3.75	2.5	V V V
VoutDC	DC Voltage on Vertical Output	See Note 6, Pin 29		3.5		V
VOI	Vertical Output Maximum Current (Pin29)			±5		mA
dVS	Max Vertical S-Correction Amplitude x0xxxxxx inhibits S-CORR x1111111 gives max S-CORR	Subaddress 07 $\Delta V/V_{PP}$ at T/4 $\Delta V/V_{PP}$ at 3T/4		-4 +4		% %
Ccorr	Vertical C-Corr Amplitude x0xxxxxx inhibits C-CORR	SubAddress 08 Byte x1000000 Byte x1100000 Byte x1111111		-3 0 3		% % %
VflyTh	Vertical Flyback Threshold	Pin 30		1		V
VflyInh	Inhibition of Vertical Flyback Input	See Note 7, Pin 30	7.5			V

Notes : 3. With Register 07 at Byte x0xxxxxx (Vertical S-Correction Control) then the S correction is inhibited, consequently the sawtooth has a linear shape.
4. With Register 08 at Byte x0xxxxxx (Vertical C - Correction Control) then the C correction is inhibited, consequently the sawtooth has a linear shape.
5. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchronize, using a single capacitor value on Pin 27 and with a constant ramp amplitude.
6. V_{OUTDC} = (7/16).V_{REF-V}. Typically 3.5V for Vertical reference voltage typical value (8V).
7. When Pin 30 (V_{REF-V}) - 0.5V, Vfly input is inhibited and vertical blanking on vertical blanking output is replaced by vertical sawtooth discharge time.

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VERTICAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
EAST/WEST FUNCTION						
EW$_{DC}$	DC Output Voltage with Typ Vpos,Keystone, Corner and Corner Balance Inhibited	Pin 31, see Figure 1		2.5		V
TDEW$_{DC}$	DC Output Voltage Thermal Drift	See Note 8		100		ppm/C
EWpara	Parabola Amplitude with Vamp Max, V-Pos Typ, Keystone, Corner and Corner Balance Inhibited	Subaddress 09 Byte 1x111111 Byte 1x100000 Byte 1x000000		 2.6 1.4 0		 V V V
EWtrack	Parabola Amplitude Function of V-AMP Control (tracking between V-AMP and E/W) with Typ Vpos, Keystone, Corner and Corner Balance Inhibited, EW Typ Amplitude (see Note 9)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 0.45 0.8 1.4		 V V V
KeyAdj	Keystone Adjustment Capability with Typ Vpos, Corner and Corner Balance Inhibited, EW Inhibited and Vertical Amplitude Max (see Note 9 and Figure 4)	Subaddress 0A Byte 10000000 Byte 11111111		 1 1		 V$_{PP}$ V$_{PP}$
KeyTrack	Intrinsic Keystone Function of V-POS Control (tracking between V-POS and EW) with Corner and Corner Balance Inhibited, EW Max Amplitude and Vertical Amplitude Max (see Note 9) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.5 0.5		
Corner Max	Max Corner Correction Amplitude with Vamp Max, V-POS Typ, EWamp, Keystone and Corner Balance Inhibited (see Note 9)	Subaddress 0B ΔEWout at T/6, 5T/6 Byte x1111111 Byte x1000000		 +0.2 -0.2		 V V
Corner BalMax	Max Corner Balance Correction Amplitude with Vamp Max, V-POS Typ, EWamp, Keystone and Corner Inhibited Subaddress 0C (see Note 9)	Byte 01111111 ΔEWout at T/4 ΔEWout at 3T/4		 +0.2 -0.2		 V V
		Byte 01000000 ΔEWout at T/4 ΔEWout at 3T/4		 -0.2 +0.2		 V V
INTERNAL HORIZONTAL DYNAMIC PHASE CONTROL FUNCTION						
SPBpara	Side Pin Balance Parabola Amplitude (Figure 2) with Vamp Max, V-POS Typ and Parallelogram Inhibited (see Notes 9 & 10)	Subaddress 0D Byte x1111111 Byte x1000000		 +2.8 -2.8		 %TH %TH
SPBtrack	Side Pin Balance Parabola Amplitude function of Vamp Control (tracking between Vamp and SPB) with SPB Max, V-POS Typ and Parallelogram Inhibited (see Notes 9 & 10)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		 1.0 1.8 2.8		 %TH %TH %TH
ParAdj	Parallelogram Adjustment Capability with Vamp Max, V-POS Typ and SPB Inhibited (see Notes 9, 10 & 11)	Subaddress 0E Byte x1111111 Byte x1000000		 +2.8 -2.8		 %TH %TH
Partrack	Intrinsic Parallelogram Function of Vpos Control (tracking between V-Pos and DHPC) with Vamp Max, SPB Max and Parallelogram Inhibited (see Notes 9 & 10) A/B Ratio B/A Ratio	Subaddress 06 Byte x0000000 Byte x1111111		 0.5 0.5		

Notes : 8. These parameters are not tested on each unit. They are measured during our internal qualification
     9. Refers to Notes 3 & 4 from last section.
   10. TH is the Horizontal PLL Period Duration.
   11. Figure 2 is representing effect of dynamic horizontal phase control.

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VERTICAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL DYNAMIC FOCUS FUNCTION						
VDF_{DC}	DC Output Voltage with V-Pos Typ	See Figure 3		6		V
$TDVDF_{DC}$	DC Output Voltage Thermal Drift	See Note 12		100		ppm/C
VDFAMP	Parabola Amplitude Function of Vamp (tracking between Vamp and VDF) with V-Pos Typ (see Figure 3) (see Note 13)	Subaddress 05 Byte 10000000 Byte 11000000 Byte 11111111		0.9 1.6 2.5		V V V
VDFKEY	Parabola Assymetry Function of VPos Control (tracking between V-Pos and VDF) with Vamp Max. (see Note 13)	Subaddress 06 Byte x0000000 Byte x1111111		0.5 0.5		

Notes : 12. Parameter not tested on each unit but measured during our internal qualification procedure including batches coming from corners of our process and also temperature characterization
13. S and C corrections are inhibited so the output sawtooth has a linear shape.

Figure 1 : E/W Output
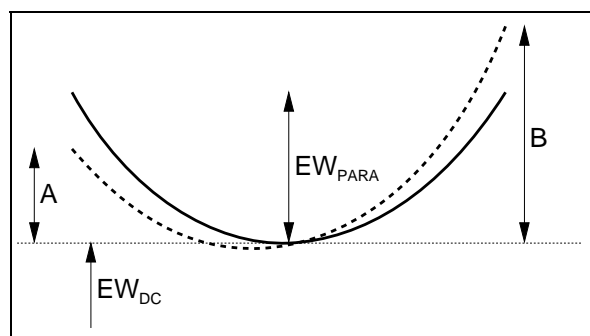
Figure 2 : Dynamic Horizontal Phase Control Output
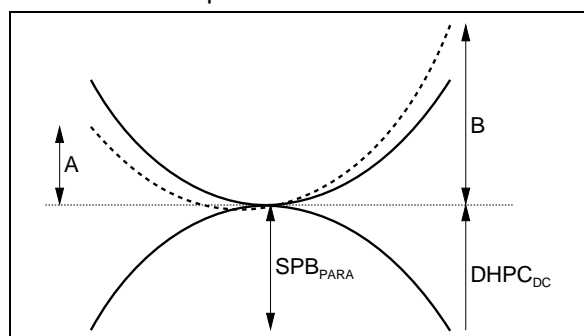
Figure 3 : Vertical Dynamic Focus Function
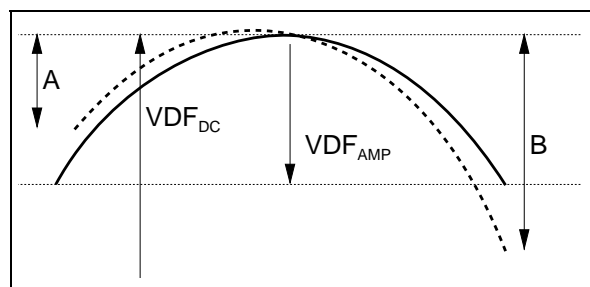
Figure 4 : Keystone Effect on E/W Output (PCC Inhibited)
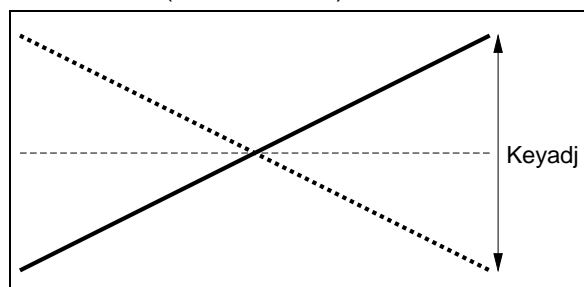
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TYPICAL VERTICAL OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Picture Image
Vertical Size	05	29	10000000 11111111	2.25V 3.75V	
Vertical Position DC Control	06	28	x0000000 x1000000 x1111111	3.2V 3.5V 3.8V	
Vertical S Linearity	07	29	x0xxxxxx Inhibited x1111111	V_{PP} $\frac{V}{V_{PP}} = 4\%$	
Vertical C Linearity	08	29	x1000000 x1111111	V_{PP} $\frac{V}{V_{PP}} = 3\%$ V_{PP} $\frac{V}{V_{PP}} = 3\%$	

9106-06.TBL / 9106-07.EPS TO 9106-13.EPS

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GEOMETRY OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Picture Image
Trapezoid Control	0A	31	EWamp Typ. 10000000 / 11111111	3.75V, 2.75V, 2.5V, 3.75V, 2.75V, 2.5V	
Pin Cushion Control	09	31	Keystone Inhibited 1x000000 / 1x111111	2.5V, 0V, 2.5V	
Parrallelogram Control	0E	Internal	SPB Inhibited x1000000 / x1111111	3.7V, 2.8% TH, 3.7V, 2.8% TH	
Side Pin Balance Control	0D	Internal	Parallelogram Inhibited X10000000 / x1111111	3.7V, 2.8% TH, 2.8% TH, 3.7V	
Vertical Dynamic Focus		32		6V, 2.5V	

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GEOMETRY OUTPUT WAVEFORMS (continued)

Function	Sub Address	Pin	Byte	Specification	Picture Image
Corner Control	0B	31	EWamp Typ. x1111111 / 01000000		
Corner Balance Control	0C	31	EWamp Typ. 10000000 / 11111111		

9106-07.TBL / 9106-23.EPS TO 9106-30.EPS

Note : The specification of output voltage is indicated on 3.75V_{PP} vertical sawtooth output condition.The output voltage depends on vertical sawtooth output voltage.

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I²C BUS ADDRESS TABLE

Sub Address Definition

Slave Address (8C) : *Write Mode*

	D8	D7	D6	D5	D4	D3	D2	D1	
0	x	x	x	x	0	0	0	0	Horizontal Drive Selection / Horizontal Duty Cycle
1	x	x	x	x	0	0	0	1	Horizontal Position
2	x	x	x	x	0	0	1	0	Safety Frequency / Free Running Frequency
3	x	x	x	x	0	0	1	1	Synchro Priority / Horizontal Focus Amplitude
4	x	x	x	x	0	1	0	0	Refresh / Horizontal Focus Keystone
5	x	x	x	x	0	1	0	1	Vertical Ramp Amplitude
6	x	x	x	x	0	1	1	0	Vertical Position Adjustment
7	x	x	x	x	0	1	1	1	S Correction
8	x	x	x	x	1	0	0	0	C Correction
9	x	x	x	x	1	0	0	1	E/W Amplitude
A	x	x	x	x	1	0	1	0	E/W Keystone
B	x	x	x	x	1	0	1	1	Cbow Corner
C	x	x	x	x	1	1	0	0	Spin Corner
D	x	x	x	x	1	1	0	1	Side Pin Balance
E	x	x	x	x	1	1	1	0	Parallelogram
F	x	x	x	x	1	1	1	1	Moire Control Amplitude

Slave Address (8D) : *Read Mode*

	D8	D7	D6	D5	D4	D3	D2	D1	
0	x	x	x	x	0	0	0	0	Synchro and Polarity Detection

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I²C BUS ADDRESS TABLE (continued)

Table : Register Map

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE								
00	Blk Sel 1, Blk [0]	HDrive 0, off [1], on		Horizontal Duty Cycle				
				[0]	[0]	[0]	[0]	[0]
01	Xray 1, reset [0]	Horizontal Phase Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
02	Safety Frequency			Free Running Frequency				
	1, on [0], off	1, F0 x 2 [0], F0 x 3		[0]	[0]	[0]	[0]	[0]
03	Sync Priority			Horizontal Focus Amplitude				
	0, Vextr [1], Vin	0, S/G [1], H/V		[1]	[0]	[0]	[0]	[0]
04	Detect Refresh [0], off			Horizontal Focus Keystone				
				[1]	[0]	[0]	[0]	[0]
05	Vramp 0, off [1], on	Vertical Ramp Amplitude Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06		Vertical Position Adjustment						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07		S Select 1, on [0]	S Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
08		C Select 1, on [0]	C Correction					
			[1]	[0]	[0]	[0]	[0]	[0]
09	EW Sel 0, off [1]		East/West Amplitude					
			[1]	[0]	[0]	[0]	[0]	[0]
0A	EW Key 0, off [1]	East/West Keystone						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	Test H 1, on [0], off	Cbow Sel 1, on [0]	Cbow Corner					
			[1]	[0]	[0]	[0]	[0]	[0]
0C	Test V 1, on [0], off	Spin Sel 1, on [0]	Spin Corner					
			[1]	[0]	[0]	[0]	[0]	[0]
0D		SPB Sel 0, off [1]	Side Pin Balance					
			[1]	[0]	[0]	[0]	[0]	[0]
0E		Parallelo 0, off [1]	Parallelogram					
			[1]	[0]	[0]	[0]	[0]	[0]
0F	Moire 1, on [0], off			Moire Control				
				[0]	[0]	[0]	[0]	[0]
READ MODE								
00	Hlock 0, on [1], no	Vlock 0, on [1], no	Xray 1, on [0], off	Polarity Detection		Synchro Detection		
				H/V pol [1], negative	V pol [1], negative	Vext det [0], no det	H det [0], no det	V det [0], no det

[ ] initial value

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OPERATING DESCRIPTION

I - GENERAL CONSIDERATIONS
I.1 - Power Supply

The typical values of the power supply voltages V_CC and V_DD are respectively 12V and 5V. Perfect operation is obtained if V_CC and V_DD are maintened in the limits : 10.8 to 13.2V and 4.5 to 5.5V.

In order to avoid erratic operation of the circuit during transient phase of V_CC switching on, or switching off, the value of V_CC is monitored and the outputs of the circuit are inhibited if V_CC is less than 7.5V typically.

In the same manner, V_DD is monitored and internal set-up is made until V_DD reaches 4V (see I^{2}C Control Table for power on reset).

In order to have a very good power supply rejection, the circuit is internally powered by several internal voltage references (the unique typical value of which is 8V). Two of these voltage references are externally accessible, one for the vertical part and one for the horizontal one. If needed, these voltage references can be used (until load is less than 5mA). Furthermore it is necessary to filter the a.m. voltage references by the use of external capacitor connected to ground, in order to minimize the noise and consequently the "jitter" on vertical and horizontal output signals.

I.2 - I^{2}C Control

TDA9106 belongs to the I^{2}C controlled device family, instead of being controlled by DC voltages on dedicated control pins, each adjustment can be realized through the I^{2}C Interface.

The I^{2}C bus is a serial bus with a clock and a data input. The general function and the bus protocol are specified in the Philips-bus data sheets.

The interface (Data and Clock) is TTL-level compatible. The internal threshold level of the input comparator is 2.2V (when V_DD is 5V). Spikes of up to 50ns are filtered by an integrator and maximum clock speed is limited to 400kHz.

The data line (SDA) can be used in a bidirectional way that means in read-mode the IC clocks out a reply information (1 byte) to the micro-processor.

The bus protocol prescribes always a full-byte transmission. The first byte after the start condition is used to transmit the IC-address(7 bits-8C) and the read/write bit (0 write - 1 read).

I.3 - Write Mode

In write mode the second byte sent contains the subaddress of the selected function to adjust (or controls to affect) and the third byte the corresponding data byte. It is possible to send more than one data byte to the IC. If after the third byte no stop or start condition is detected, the circuit increments automatically the momentary subaddress in the subaddress counter by one (auto-increment mode). So it is possible to transmit immediately the next data bytes without sending the IC address or subaddress. It can be useful so as to reinitialize the whole controls very quickly (flash manner). This procedure can be finished by a stop condition.

The circuit has 16 adjustment capabilities: 3 for Horizontal part, 4 for Vertical one, 2 for E/W correction, 2 for original Corner correction, 2 for the Dynamic Horizontal phase control, 1 for Moire option and 2 for Horizontal Dynamic Focus.

20 bits are also dedicated to several controls (ON/OFF, Horizontal Safety Frequency, Synchro Priority, Detection Refresh and Xray reset).

I.4 - Read Mode

During read mode the second byte transmits the reply information.

The reply byte contains Horizontal and Vertical Lock/Unlock status, Xray activated or not, the Horizontal and Vertical polarity detection. It also contains Synchro detection status that is useful for μP to assign Sync priority.

A stop condition always stops all activities of the bus decoder and switches the data and the clock line (SDA and SCL) to high impedance.

See I^{2}C Subaddress and control tables.

I.5 - Synchro Processor

The internal Sync Processor allows the TDA9106 to accept any kind of input synchro signals :
- separated Horizontal & Vertical TTL-compatible sync signals,
- composite Horizontal &Vertical TTL-compatible sync signals,
- sync on green or composite video signal.

OPERATING DESCRIPTION (continued)

I.6 - Sync Identification Status

TDA9106 is able to feed back to the MCU (thanks to I^2C) the Sync input status (sync identification) so that the MCU can choose Sync priority through I^2C.

As extracted Vertical sync pulse is performed when choice already occured and when 12V is supplied, we recommend to use the device as following :(that means that even in Power management mode the IC is able to inform MCU on detected synchro signals due to its 5V supply).

First, refresh Synchro detection by I^2C. Then check the status of H/V det and Vdet by I^2C read.

Sync priority choice should be :

Table 1 : Sync Priority Choice

H/V det	V det	Sync priority Subaddress 03		Comment
		D8	D7	Synchro type
Yes	Yes	1	1	Separated H & V
Yes	No	0	1	Composite TTL H&V
No	No	0	0	Sync on Green

Of course, when choice is done, one can refresh the synchro detections and verify that extracted Vsync is present and that no synchro type change occured.

Synchro processor is also giving synchro polarity information.

I.7 - IC status

The IC can inform the MCU either the 1st Horizontal PLL or Vertical section are locked or not, and if Xray has been activated.

This last status permits to the MCU :
- reset the Xray internal latch decreasing the V_{CC} supply
- directly reset throw the I^2C interface.

I.8 - Synchro Inputs

Both H/HVin and Vsyncin inputs are TTL compatible trigger with Hysterisis to avoid erratic detection. It includes pull up resistor to V_{DD}.

Vertical sync extractor is included for composite sync or composite video.Application engineer must adapt resistor R and capacitor C dedicated to its application.

Figure 5

TDA9106
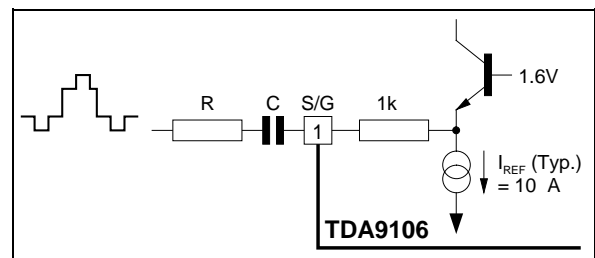
Resistor R is fixed by detection threshold wanted :
$$R < (V_{THRESHOLD} / I_{REF})$$
Then C is determined by maximum pulse width to detect (in general, vertical sync width) :
$$RC > (max \ pulse \ width)$$

I.9 - Synchro Processor Outputs

Synchro processor delivers on 3 TTL-compatible CMOS outputs the following signals :
- Hout as follow :

Sync Mode	Hout Mode	Hout Polarity
Separated	Horizontal	Same as Input
TTL Composite	TTL Composite	Same as Input
S/G	Composite	Negative

- Vsyncout is either vertical extracted pulse output or Vsyncin input. It keeps the input polarity.
- Hlockout is the Horizontal 1st PLL status : 0V when locked. It permits MCU to adjust free running frequency and optimizes the IC performance.

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OPERATING DESCRIPTION (continued)

II - HORIZONTAL PART
II.1 - Internal Input Conditions

Horizontal part is internally fed by synchro processor with a digital signal. corresponding to horizontal synchro pulses or to TTL composite input.

Concerning the duty cycle of the input signal, the following signals (positive or negative) may be applied to the circuit.

Using internal integration, both signals are recognized on condition that $Z/T < 25\%$. Synchronization occurs on the leading edge of the internal sync signal. The minimum value of Z is 0.7µs.
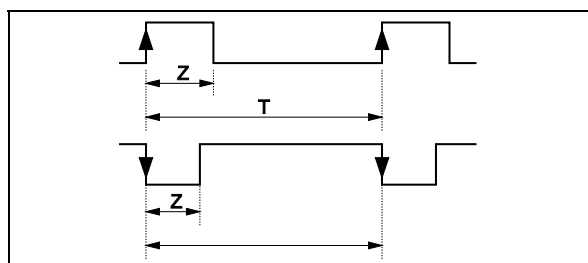
Figure 6

An other integration is able to extract vertical pulse of composite synchro if duty cycle is more than 25% (typically d = 35%).

Figure 7
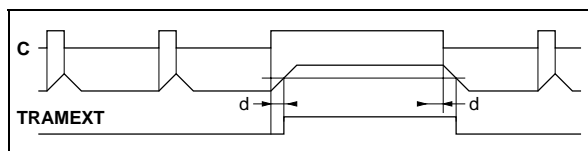
The last feature performed is the equalizing pulses removing to avoid parasitic pulses on phase comparator input which is intolerent to wrong or missing pulse.

II.2 - PLL1

The PLL1 is composed of a phase comparator, an external filter and a voltage controlled oscillator (VCO).

The phase comparator is a "phase frequency" type designed in CMOS technology. This kind of phase detector avoids locking on false frequencies. It is followed by a "charge pump", composed of two current sources sunk and sourced (I = 1mA Typ. when locked, I = 140µA when unlocked). This difference between lock/unlock permits a smooth catching of horizontal frequency by PLL1. This effect is reinforced by an internal original slow down

system when PLL1 is locked avoiding Horizontal too fast frequency change.

The dynamic behaviour of the PLL is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used (see Figure 8).

Figure 8
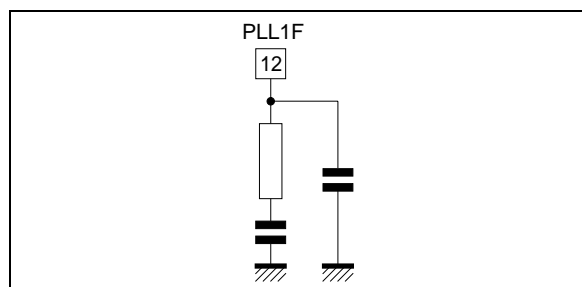
PLL1 is internally inhibited during extracted vertical sync (if any) to avoid taking in account missing pulses or wrong pulses on phase comparator. The inhibition results from the opening of a switch located between the charge pump and the filter (see Figure 9). For particular synchro type, MCU can drive Pin 3 to high level (TTL compatible input) to inhibit PLL1. It can also be used to avoid PLL1 locking on synchro inputs if a "dangerous" mode is detected by the MCU.

The VCO uses an external RC network. It delivers a linear sawtooth obtained by charge and discharge of the capacitor, by a current proportionnal to the current in the resistor. Typical thresholds of sawtooth are 1.6V and 6.4V. These two levels are accessible to be filtered as on Figure 10 to improve jitter.

The control voltage of the VCO is typically comprised between 1.33V and 6V (see Figure 10). The theorical frequency range of this VCO is in the ratio 1 to 4.5, the effective frequency range has to be smaller 1 to 4.2 due to clamp intervention on filter lowest value. To avoid spread of external components and the circuit itself, it is possible to adjust free running frequency through I^2C. This adjustment can be made automatically on the manufacturing line without manual operation by using Hlock/unlock information. The adjustment range is 0.8 to 1.3 F0 (where 1.3 F0 is the free running frequency at power on reset).

The synchro frequency has to be always higher than the free running frequency. As an example for a synchro range from 24kHz to 100kHz, the suggested free running frequency is 23kHz.

OPERATING DESCRIPTION (continued)

Figure 9 : PLL1 Block Diagram

* SMFE : Safety Frequency Mode Enable
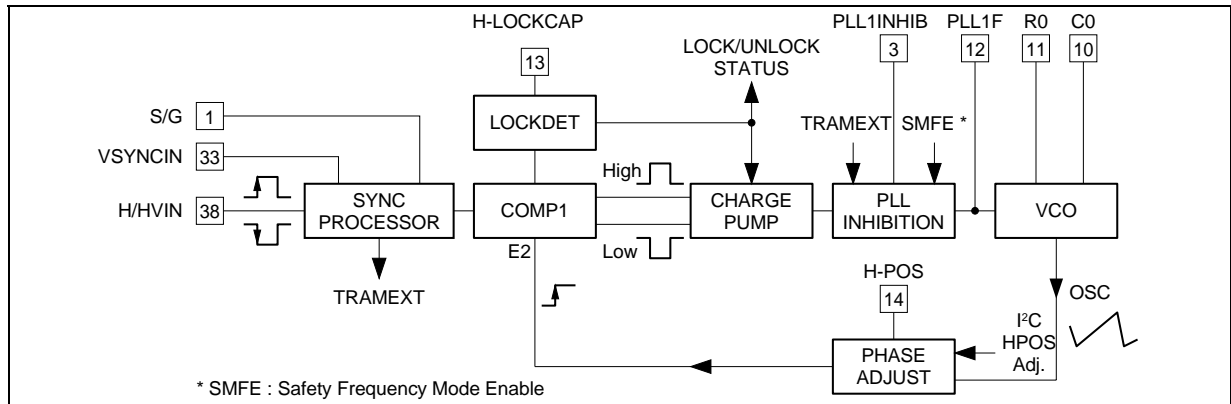
Figure 10 : Details of VCO
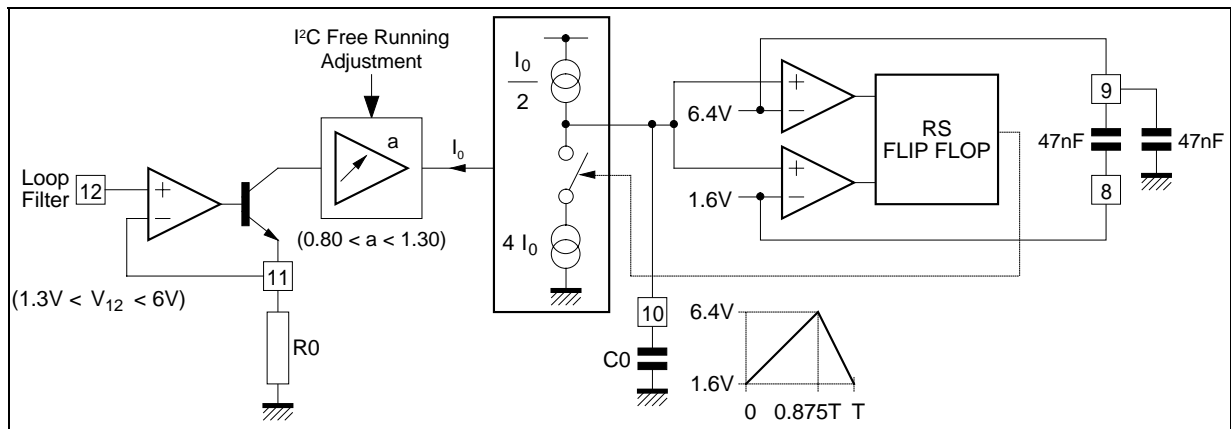
An other feature is the capability for MCU to force horizontal frequency through I^2C to 2xF0 or 3xF0 (for burn in mode or safety requirement).In this case, inhibition switch is opened leaving PLL1 free but voltage on PLL1 filter is forced to 2.66V for 2xF0 or 4.0V for 3xF0.

The PLL1 ensures the coincidence between the leading edge of the synchro signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage I^2C adjustable between 2.8V and 4.0V (corresponding to $\pm$ 10%) (see Figure 11). This voltage has to be filtered on Pin 14 so as to optimize jitter.

The TDA9106 also includes a Lock/Unlock identification block which senses in real time wheither PLL1 is locked on the incoming horizontal sync signal or not. The resulting information is available on Hlockout (see Synchro Processor). The block function is described in Figure 12.

The NOR1 gate is receiving the phase comparator output pulses (which also drive the charge pump). When PLL1 is locked, on point A there is a very small negative pulse (about 100ns) at each hori-

zontal cycle, so after RC filter, there is a high level on Pin 13 which forces Hlockout to low level. Hysterisis comparator detects locking when Pin 13 is reaching 6.5V and unlocking when Pin 13 is decreasing to 6.0V.

Figure 11 : PLL1 Timing Diagram
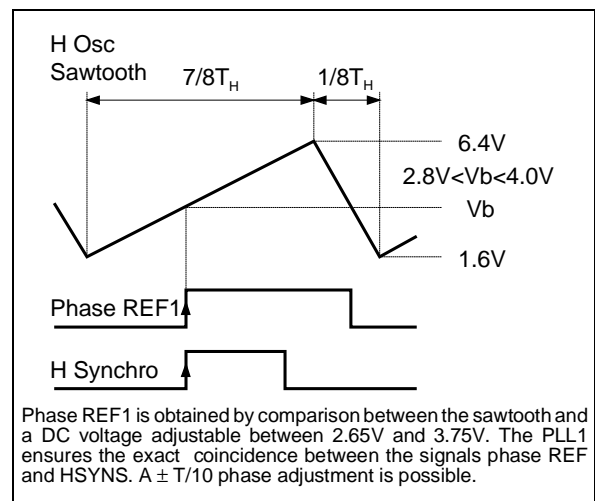
Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.65V and 3.75V. The PLL1 ensures the exact coincidence between the signals phase REF and HSYNS. A $\pm$ T/10 phase adjustment is possible.

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OPERATING DESCRIPTION (continued)

Figure 12 : LOCK/UNLOCK Block Diagram
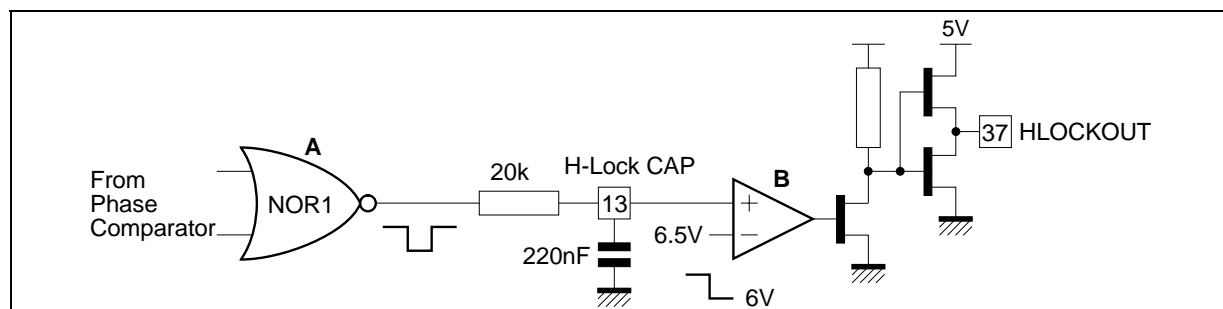
When PLL1 is unlocked, the 100ns negative pulse on A becomes much larger and consequently the average level on Pin 13 decreases. It forces Hlockout to go high.

The Pin 13 status is approximately the following :
- near 0V when there is no H-Sync
- between 0 and 4V with H-Sync frequency different from VCO
- between 4 to 8 V when VCO frequency reaches H-Sync one (but not already in phase)
- near 8V when PLL1 is locked.

It is important to notice that Pin 13 is not an output pin but is only used for filtering purpose (see Figure 12).

The lock/unlock information is also available throw I^2C read.

II.3 - PLL2

The PLL2 ensures a constant position of the shaped flyback signal in comparion with the saw-tooth of the VCO (Figure 13).

Figure 13 : PLL2 Timing Diagram

The duty cycle of H-drive is adjustable between 30% and 60%.

The phase comparator of PLL2 (phase type comparator) is followed by a charge pump with $\pm$ 0.5mA (typ.) output current.

The flyback input is composed of an NPN transistor. This input must be current driven. The maximum recommended input current is 2mA (see Figure 14).

Figure 14 : Flyback Input Electrical Diagram
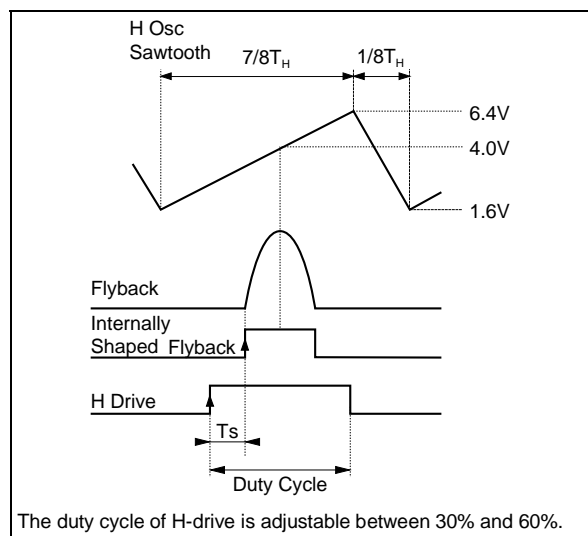
The duty cycle is adjustable through I^2C from 30% to 60%. For Start Up safe operation, initial duty cycle (after Power on reset) is 60% so as to avoid too long conduction of BU transistor.

Maximum storage time is about 43.75% - (Tfly/2.TH). Typically, Tfly/TH is around 20% that means Ts max is around 33.75%.

II.4 - Output Section

The H-drive signal is transmitted to the output through a shaping block ensuring Ts and I^2C adjustable duty cycle. In order to secure scanning power part operation, the output is inhibited in the following circumstances :
- V_{CC} too low
- Xray protection activated
- During horizontal flyback
- I^2C bit control (voluntary inhibition by MCU).

The output stage is composed of a NPN Darlington bipolar transistor. Both the collector and the emittor are accessible (see Figure 16).

The output Darlington is in off-state when the power scanning transistor is also in off-state.

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OPERATING DESCRIPTION (continued)

Figure 16 : Output stage simplified diagram, showing the two possibilities of connection
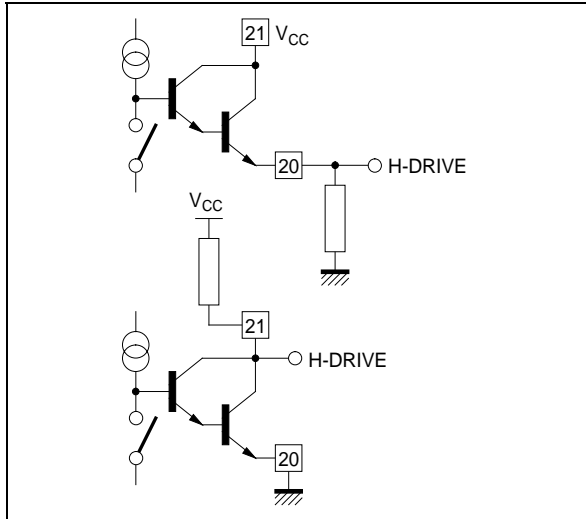
The maximum output current is 20mA, and the corresponding voltage drop of the output darlington is 1.1V typically.

It is evident that the power scanning transistor cannot be directly driven by the integrated circuit.

An interface has to be designed between the circuit and the power transistor which can be of bipolar or MOS type.

II.5 - X-RAY Protection

The activation of the X-Ray protection is obtained by application of a high level on the X-Ray input (Pin 15 > 8V). The consequencies of X-Ray protection are :
- inhibition of H-Drive output
- activation of horizontal blanking output.
- activation of vertical blanking output.

The reset of this protection is obtained either by V_{CC} switch off or I^2C reset by MCU (see Figure 17).

II.6 - Horizontal Dynamic Focus

TDA9106 delivers an horizontal parabola wave form on Pin 17. This parabola is performed from a sawtooth in phase with flyback pulse. This sawtooth is present on Pin 16 where the horizontal focus capacitor is the same as C0 to obtain a controlled amplitude (from 2 to 4.7V typically).

Symmetry (keystone) and amplitude are I^2C adjustable (see Figure 18). This signal has to be connected to the CRT focusing grids and mixed with vertical dynamic focus.

Figure 17 : Safety Functions Block Diagram

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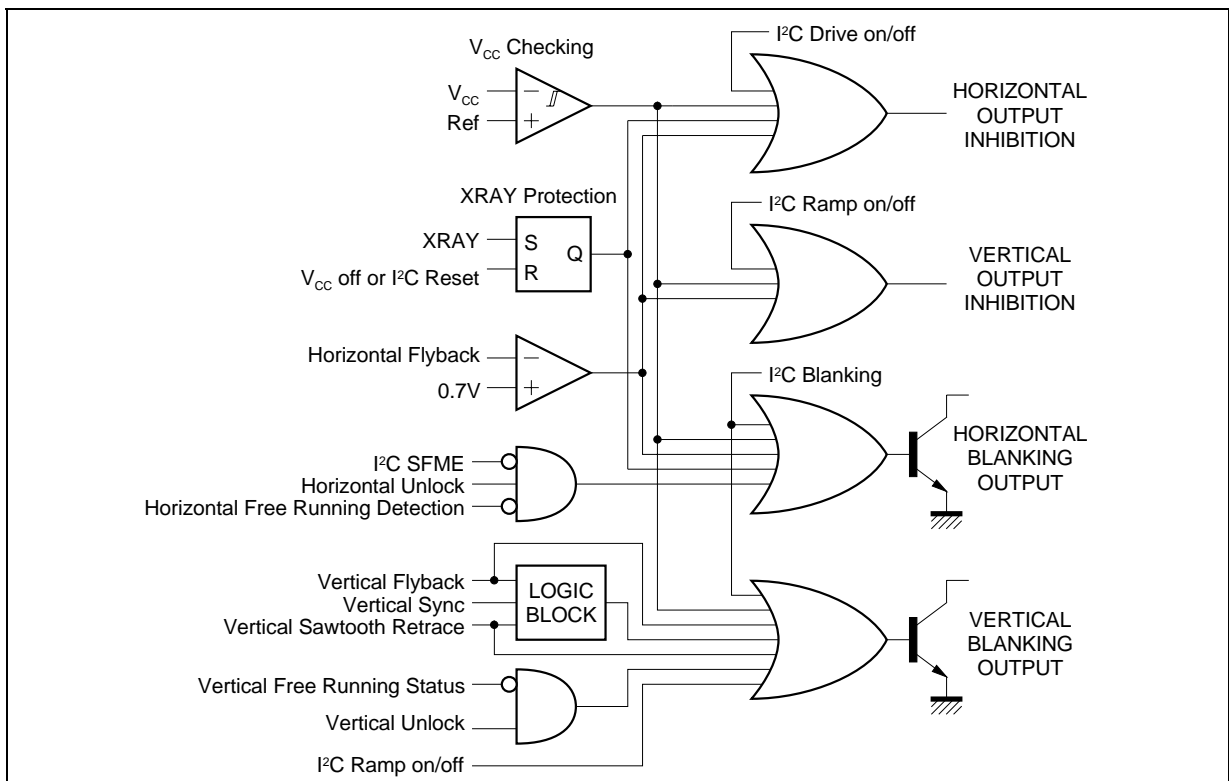
OPERATING DESCRIPTION (continued)

Figure 18
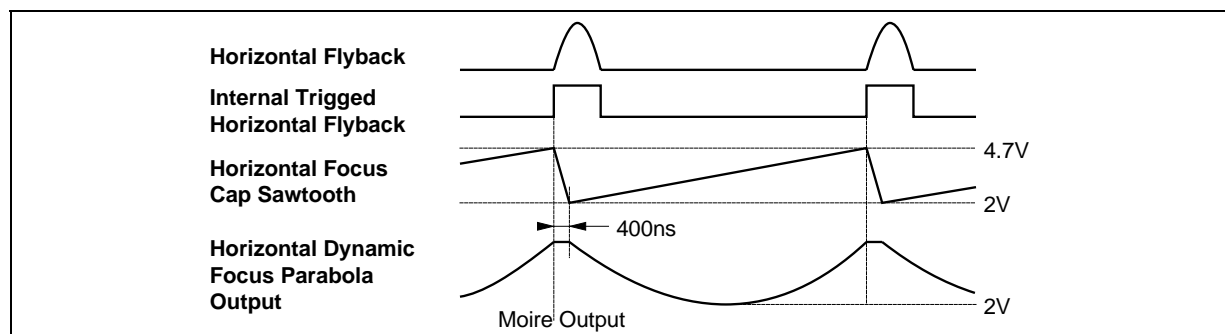
II.7 - Moire Output

The moire output is intented to correct a beat between horizontal video pixel period and actual CRT pixel width.

The moire signal is a combination of Horizontal and Vertical frequency signals.

To achieve a moire cancellation, it has to be connected to any point on the chassis controlling the horizontal position. We recommend to introduce this "Horizontal Controlled Jitter" on the relative ground

of PLL2 capacitor where this "controlled jitter" frequency type will directly affect the horizontal position.The amplitude of the signal is I^2C adjustable.

One point to notice is :

- in case H-Moire is not necessary in the application, H-Moire output (Pin 2) can be turned to as a 5 bits digital to analog converter output (0.3V to 2.2V V output voltage),
- in case of no use in application, this pin must be left high impedance(or resistor to ground).

Figure 19 : Moire Function Block Diagram
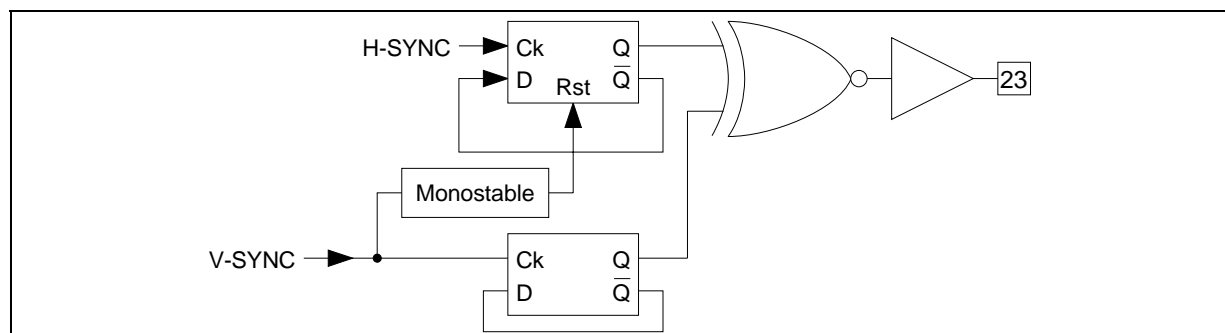
Figure 20 : Moire Output Waveform

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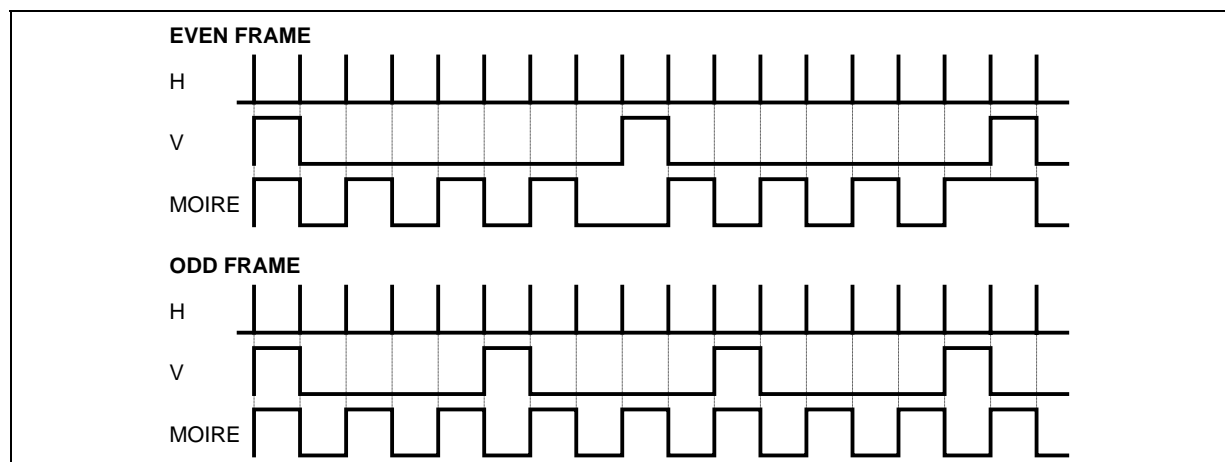
OPERATING DESCRIPTION (continued)

III - VERTICAL PART

III.1 - Geometric Corrections

The principle is represented in Figure 21.

Starting from the vertical ramp, a parabola shaped current is generated for E/W correction, dynamic horizontal phase control correction, and vertical dynamic Focus correction.

The base of the parabola generator is an analog multiplier the output current of which is equal to :

$$\Delta I = k \cdot (V_{OUT} - V_{DCOUT})^2$$

Where Vout is the vertical output ramp, typically comprised between 2 and 5V, Vdcout is the vertical DC output adjustable in the range $3.2V \geq 3.8V$ in order to generate a dissymetric parabola if required (keystone adjustment).

Corner and Corner Balance corrections may be added to the E/W one. These are respectively 3rd and 2nd order waveforms.

In order to keep a good screen geometry for any end user preferences adjustment we implemented the "geometry tracking".

Due to large output stages voltage range (E/W, FOCUS), the combination of tracking function with maximum vertical amplitude max or min vertical position and maximum gain on the DAC control

may lead to the output stages saturation. This must be avoided by limiting the output voltage by apropriate I^{2}C registers values.

For E/Wpart and Dynamic Horizontal phase control part, a sawtooth shaped differential current in the following form is generated :

$$\Delta I' = k' \cdot (V_{OUT} - V_{DCOUT})^2$$

Then ΔI and $\Delta I'$ are added together and converted into voltage for the E/W part.

Each of the four E/W components or the two Dynamic Horizontal phase control ones may be inhibited by their own I^{2}C select bit.

The E/W parabola is available on Pin 31 by the way of an emitter follower which has to be biased by an external resistor (10kΩ). It can be DC coupled with external circuitry.

The output connection of the vertical Dynamic Focus is the same as the E/W one.

This reverse parabola is available on Pin 32.

Dynamic Horizontal phase control current drives internally the H-position, moving the Hfly position on the Horizontal sawtooth in the range $\pm$ 2.8% Th both on SidePin Balance and Parallelogram.

Figure 21 : Geometric Corrections Principle

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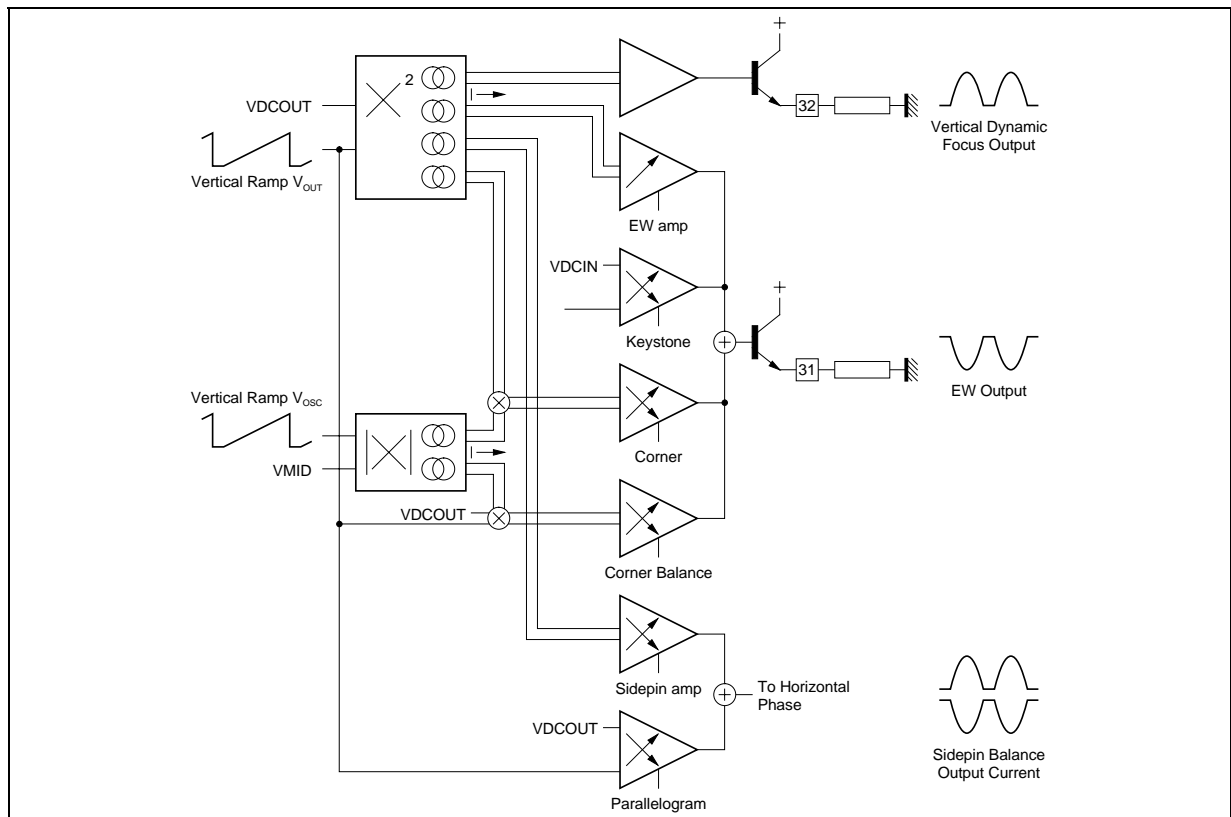
OPERATING DESCRIPTION (continued)

III.2 - EW

$$EW_{OUT} = 2.5V + K1\,(V_{OUT} - V_{DCOUT})^2$$
$$+ K2\,(V_{OUT} - V_{DCOUT})$$
$$+ K3\,(V_{OUT} - V_{DCOUT})^2\,|V_{OSC} - V_{MID}|$$
$$+ K4\,(V_{OUT} - V_{DCOUT})\,|V_{OSC} - V_{MID}|$$

V_{OSC} is the ramp Pin 27 and V_{MID} the middle of it, typically 3.5V

K1 is adjustable by EW amplitude I^2C register
K2 is adjustable by Keystone I^2C register
K3 is adjustable by Cbow Corner I^2C register
K4 is adjustable by Spin Corner I^2C register

III.3 - Dynamic Horizontal Phase Control

$$I_{OUT} = K5\,(V_{OUT} - V_{DCOUT})^2 + K6\,(V_{OUT} - V_{DCOUT})$$

K5 is adjustable by SidePin Balance I^2C register
K6 is adjustable by Parallelogram I^2C register

III.4 - Vertical Dynamic Focus

$$VFOC_{OUT} = 6V - 0.7\,(V_{OUT} - V_{DCOUT})^2$$

No adjustment is available for this part except by means of tracking.

III.5 - Vertical Sawtooth Generator

The vertical part generates a fixed amplitude ramp which can be affected by S and C correction shape. Then, the amplitude of this ramp is adjusted to drive an external power stage (see Figure 22).
The internal reference voltage used for the vertical part is available between Pin 26 and Pin 24. Its typical value is :

$$V_{26} = V_{REF} = 8V$$

The charge of the external capacitor on Pin 27 (VCAP) generates a fixed amplitude ramp between the internal voltages, V_I ($V_I = V_{REF}/4$) and V_H ($V_H = 5/8 \times V_{REF}$).

Figure 22 : Vertical Part Block Diagram

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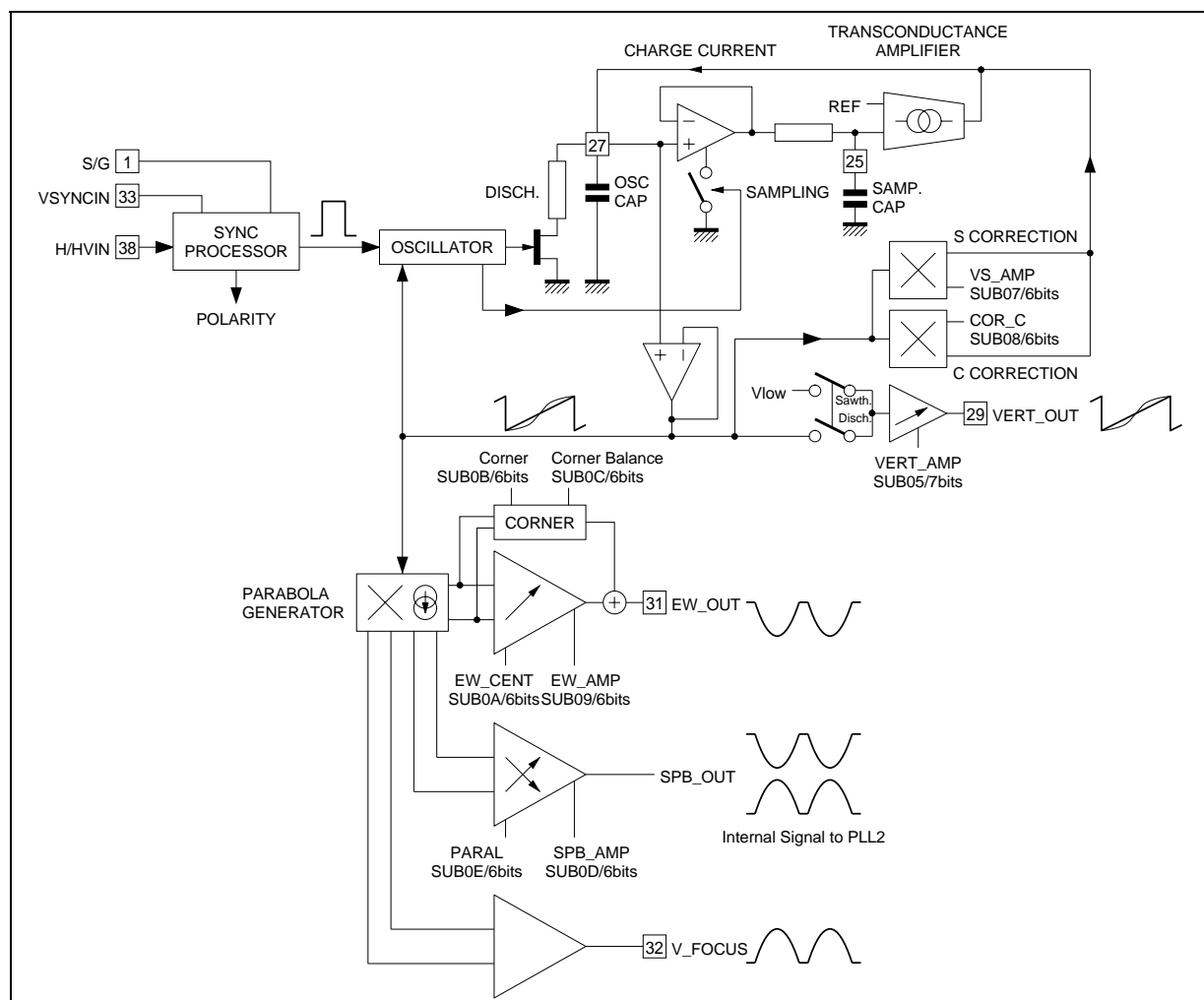
OPERATING DESCRIPTION (continued)

When the synchronization pulse is not present, an internal current source sets the free running frequency. For an external capacitor, $C_{OSC} = 150nF$, the typical free running frequency is 106Hz.

Typical free running frequency can be calculated by :

$$f_0 \text{ (Hz)} = 1.6 \, e^{-5} \cdot \frac{1}{C_{OSC}}$$

A negative or positive TTL level pulse applied on Pin 33 (VSYNC) as well as a TTL composite sync on Pin 38 or a Sync on Green signal on Pin 1 can synchronise the ramp in the range [fmin , fmax]. This frequency range depends on the external capacitor connected on Pin 27. A capacitor in the range [150nF, 220nF] $\pm$ 5% is recommended for application in the following range : 50Hz to 120Hz.

Typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by :

$$f_{(Max.)} = 2.5 \text{ x } f_0 \text{ and } f_{(Min.)} = 0.33 \text{ x } f_0$$

If S or C corrections are applied, these values are slighty affected.

If a synchronization pulse is applied, the internal oscillator is automaticaly synchronized but the amplitude is no more constant. An internal correction is activated to adjust it in less than a half a second : the highest point of the ramp (Pin 27) is sampled on the sampling capacitor connected on Pin 25 at each clock pulse and a transconductance amplifier generates the charge current of the capacitor. The ramp amplitude becomes again constant and frequency independant.

The read status register enables to have the vertical Lock-Unlock and the vertical Sync Polarity informations.

It is recommended to use a AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

Good stability of the internal closed loop is reached by a 470nF $\pm$ 5% capacitor value on Pin 25 (VAGC).

Pin 30, VFLY is the vertical flyback input used to generate the vertical blanking signal on Pin 23. If Vfly is not used, (V_{REF} - 0.5), at minimum, must be connected to this input.

In such case, the vertical blanking output will be activated by the vertical sync input signal and re-

setted by the end of vertical sawtooth discharging pulse.

III.6 - I²C Control Adjustments

Then, S and C correction shapes can be added to this ramp. This frequency independent S and C corrections are generated internally. Their amplitude are adjustable by their respective I²C register. They can also be inhibited by their Select bit.

At the end, the amplitude of this S and C corrected ramp can be adjusted by the vertical ramp amplitude control register.

The adjusted ramp is available on Pin 29 (V_{OUT}) to drive an external power stage.

The gain of this stage is typically 25% depending on its register value.

The DC value of this ramp is kept constant in the frequency range, for any correction applied on it. its typical value is $V_{MID} = 7/16 \cdot V_{REF}$.

A DC voltage is available on Pin 28 (VDCOUT). It is driven by its own I²C register (vertical Position). Its value is $V_{DCOUT} = 7/16 \cdot V_{REF} \pm 300mV$.

So the V_{DCOUT} voltage is correlated with DC value of V_{OUT}. It increases the accuracy when temperature varies.

III.7 - Basic Equations

In first approximation, the amplitude of the ramp on Pin 29 (Vout) is :

$$V_{OUT} - V_{MID} = (V_{OSC} - V_{MID}) \cdot (1 + 0.25 \, (V_{AMP}))$$

with $V_{MID} = 7/16 \cdot V_{REF}$; typically 3.5V, the middle value of the ramp on Pin 27
$V_{OSC} = V_{27}$, ramp with fixed amplitude
V_{AMP} is -1 for minimum vertical amplitude register value and +1 for maximum

On Pin 28 (V_{DCOUT}), the voltage (in volts) is calculated by :

$$V_{DCOUT} = V_{MID} + 0.3 \, (VPOS)$$

with VPOS equals -1 for minimum vertical position register value and +1 for maximum
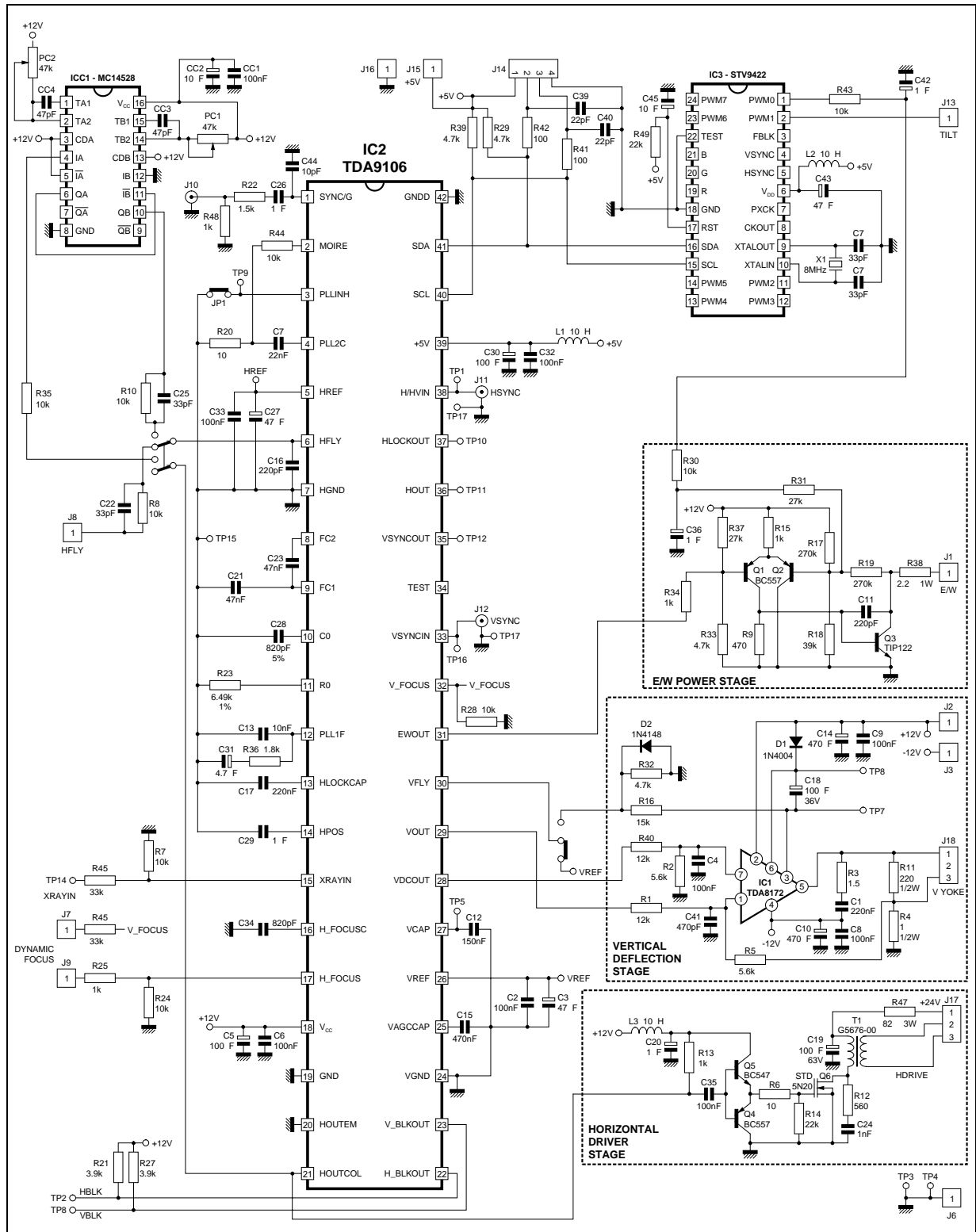
The current available on Pin 27 is :

$$I_{OSC} = \frac{3}{8} \cdot V_{REF} \cdot C_{OSC} \cdot f$$

with C_{OSC} : capacitor connected on Pin 27
f : synchronization frequency

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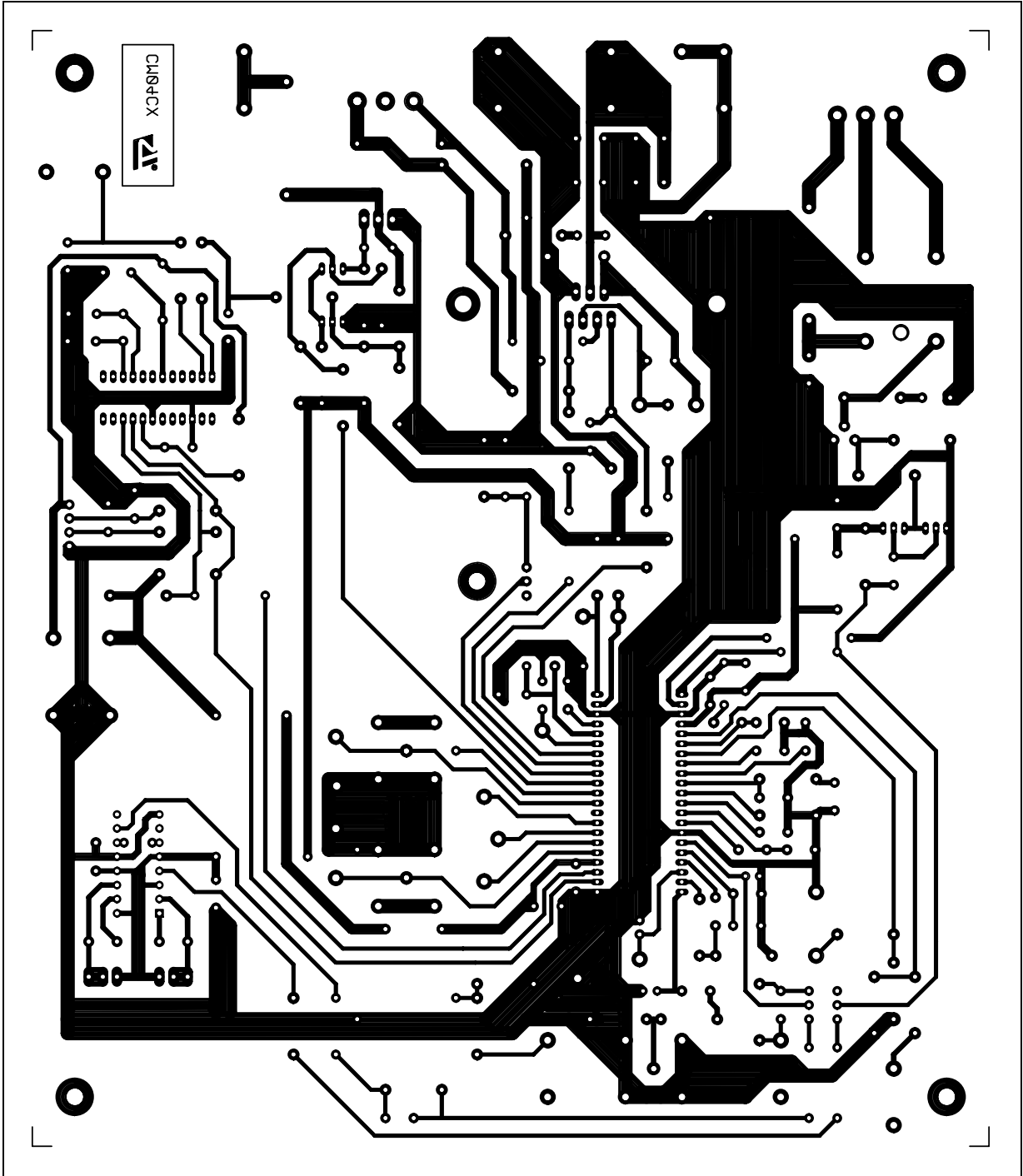**MICROELECTRONICS**

APPLICATION DIAGRAMS

Figure 23 : Demonstration Board

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APPLICATION DIAGRAMS (continued)

Figure 24 : PCB Layout

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APPLICATION DIAGRAMS (continued)

Figure 25 : Components Layout

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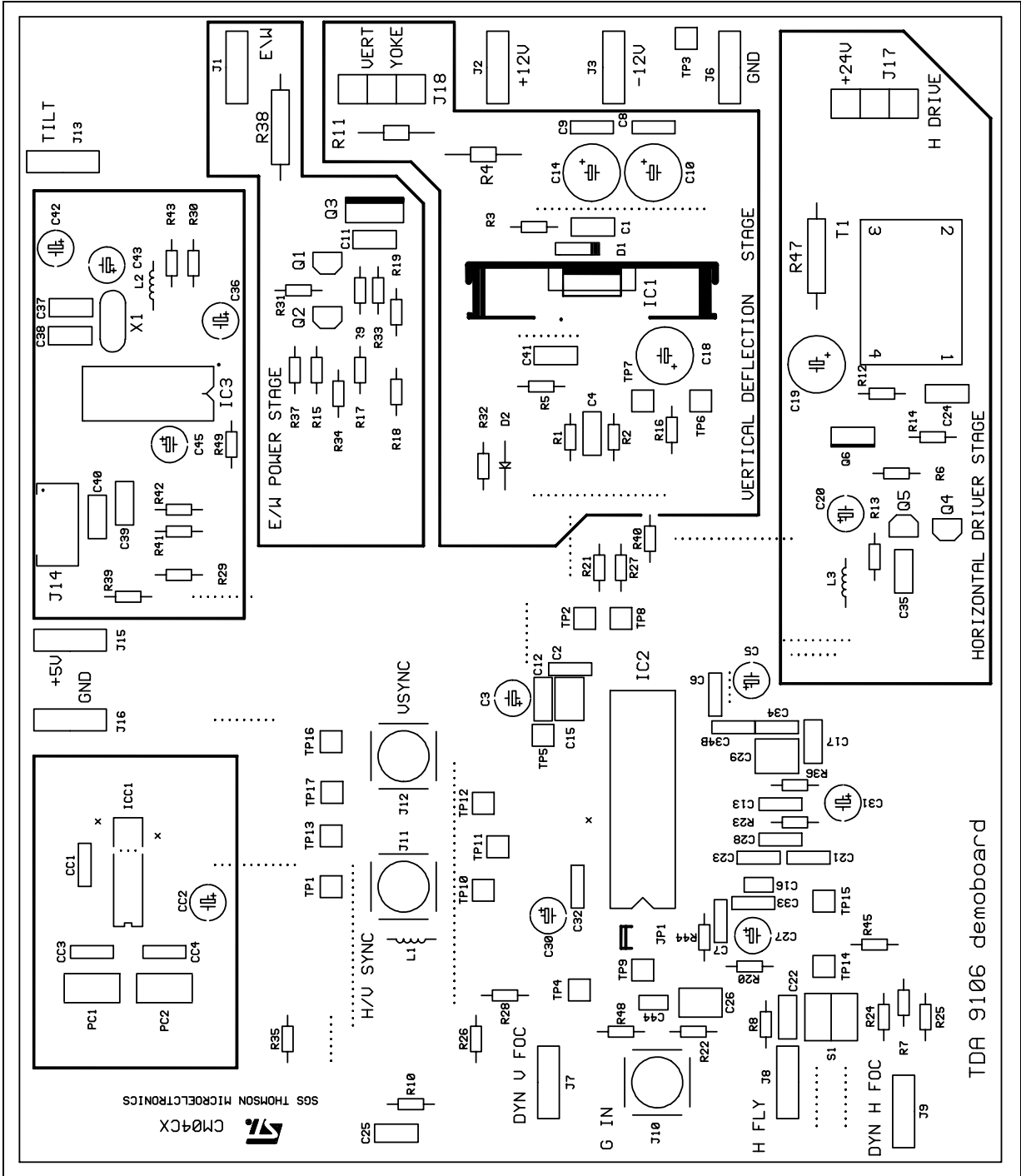
PACKAGE MECHANICAL DATA
42 PINS - PLASTIC SHRINK DIP
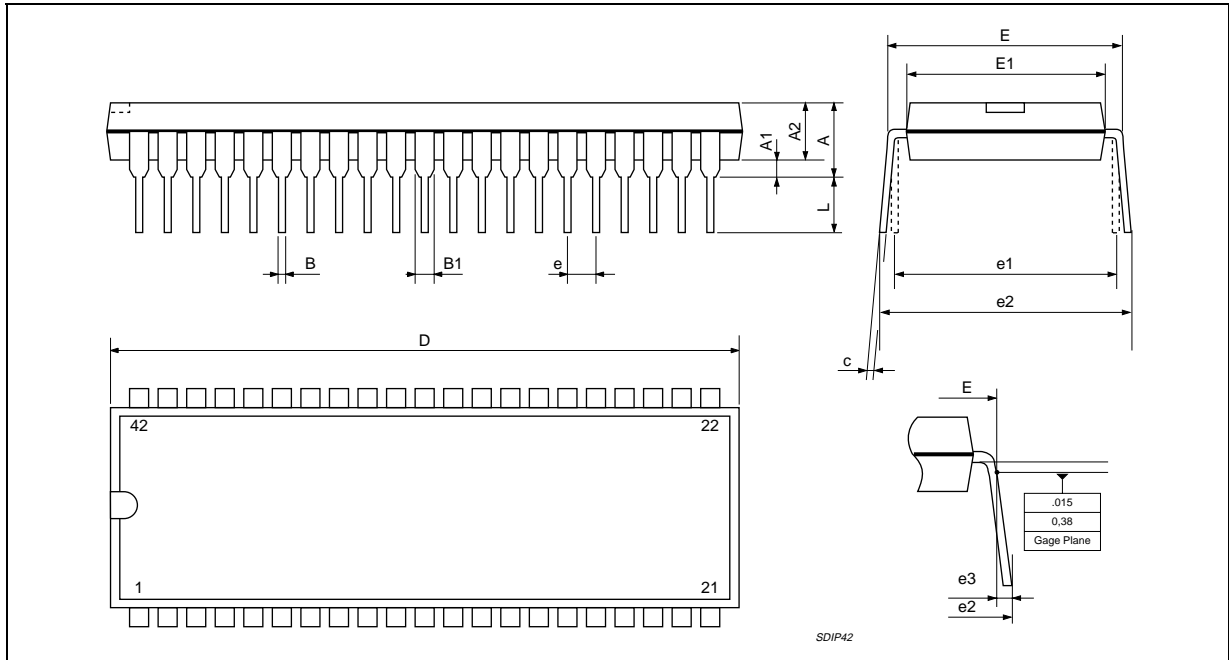
Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3		1.52			0.060	
L	2.54	3.30	3.56	0.10	0.130	0.140

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