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SSD1850/51

Advance Information

CMOS

LCD Segment / Common Driver with Controller

SSD1850/51 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. SSD1850 consists of 194 high voltage driving output pins for driving 128 Segments and 64 Commons and 1 icon line. SSD1851 consists of 210 high voltage driving output pins for driving 128 Segments and 80 Commons and 1 icon line.

SSD1850/51 display data directly from their internal 128x65x2 / 128x81x2 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through hardware selectable 6800-/8080-series compatible Parallel Interface or 3/4 wires Serial Peripheral Interface.

SSD1850/51 embeds a DC-DC Converter, a LCD Voltage Regulator, an On-Chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/package layout, SSD1850/51 is suitable for any portable battery-driven applications requiring long operation period and compact size.

FEATURES

128x64/80 + 1 icon line, 4 gray-levels Graphic Display
Programmable Multiplex ratio [16Mux - 65Mux/81Mux]
Single Supply Operation, 1.8 V - 3.3V
Low Current Sleep Mode(<1.0 uA)
On-Chip Voltage Generator / External Power Supply
Software selectable 2X / 3X / 4X / 5X / 6X On-Chip DC-DC Converter
On-Chip Oscillator
On-Chip Bias Dividers
Programmable 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 and 1/10 bias ratio
Maximum +15.0V LCD Driving Output Voltage
Hardware pin selectable for 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, 3-wire Serial Peripheral Interface or 4-wire Serial Peripheral Interface
On-Chip 128x65x2 / 128x81x2 Graphic Display Data RAM
Re-mapping of Row and Column Drivers
Vertical Scrolling
Display Offset Control
64 Level Internal Contrast Control
External Contrast Control
Maximum 15MHz SPI or 10MHz PPI (8 bit) operation
Selectable LCD Driving Voltage Temperature Coefficients (2 settings)
Available in Gold Bump Die, Standard TAB (Tape Automated Bonding) Package and COF (Chip On Foil)

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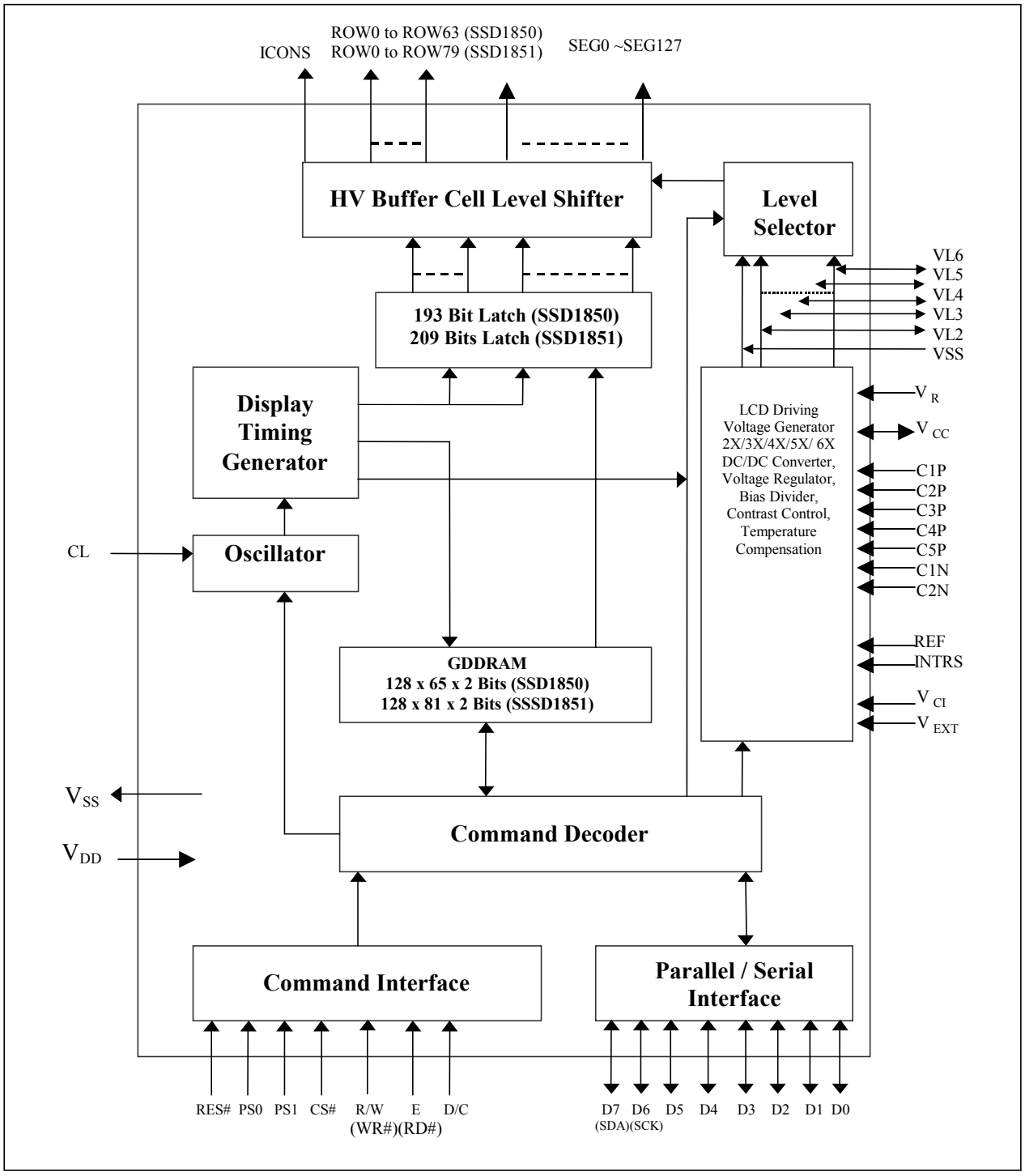
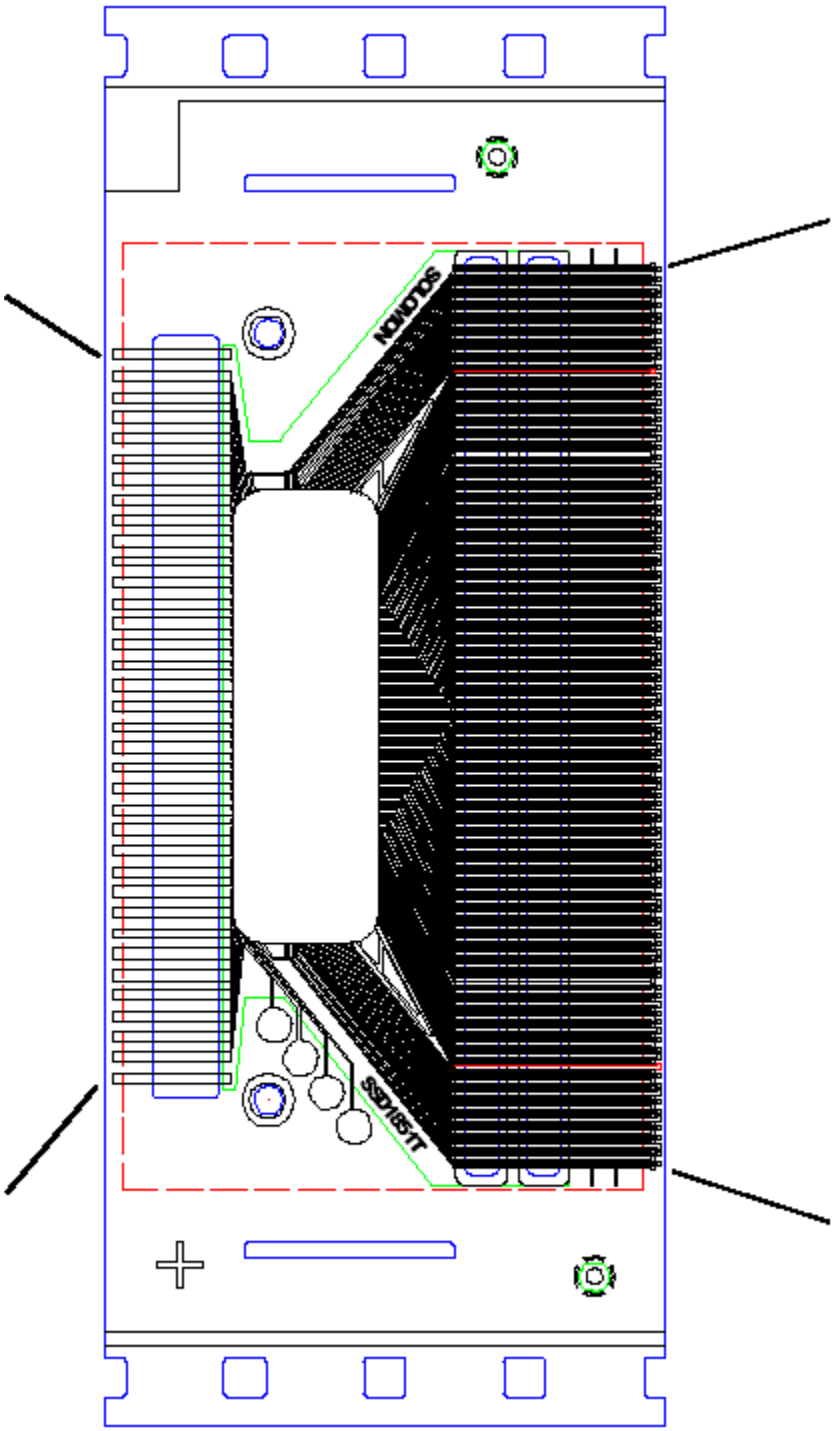
ORDERING INFORMATION

Ordering Part Number	SEG	COM	Default Bias	Package Form	Reference
SSD1850Z	128	64 + 1	1/9	Gold Bump Die	
SSD1851Z	128	80 + 1	1/10	Gold Bump Die	
SSD1851TR1	128	80 + 1	1/10	TAB	
SSD1851U	128	80 + 1	1/10	COF	

BLOCK DIAGRAM



TAB PAD ARRAGEMENT (SSD1851T PIN ASSIGNMENT) (Copper View)



N/C	1
CL	2
VR	3
VL6	4
VL5	5
VL4	6
VL3	7
VL2	8
INTRS	9
C4P	10
C2N	11
C2P	12
C1P	13
C1N	14
C3P	15
C5P	16
VCC	17
VSS	18
VCI	19
VDD	20
D7	21
D6	22
D5	23
D4	24
D3	25
D2	26
D1	27
D0	28
E(RD#)	29
R/W(WR#)	30
D/C	31
RES#	32
CS#	33
PS1	34
PS0	35
N/C	36

247 NC
246 NC
245 COM39
244 COM38
243 COM37

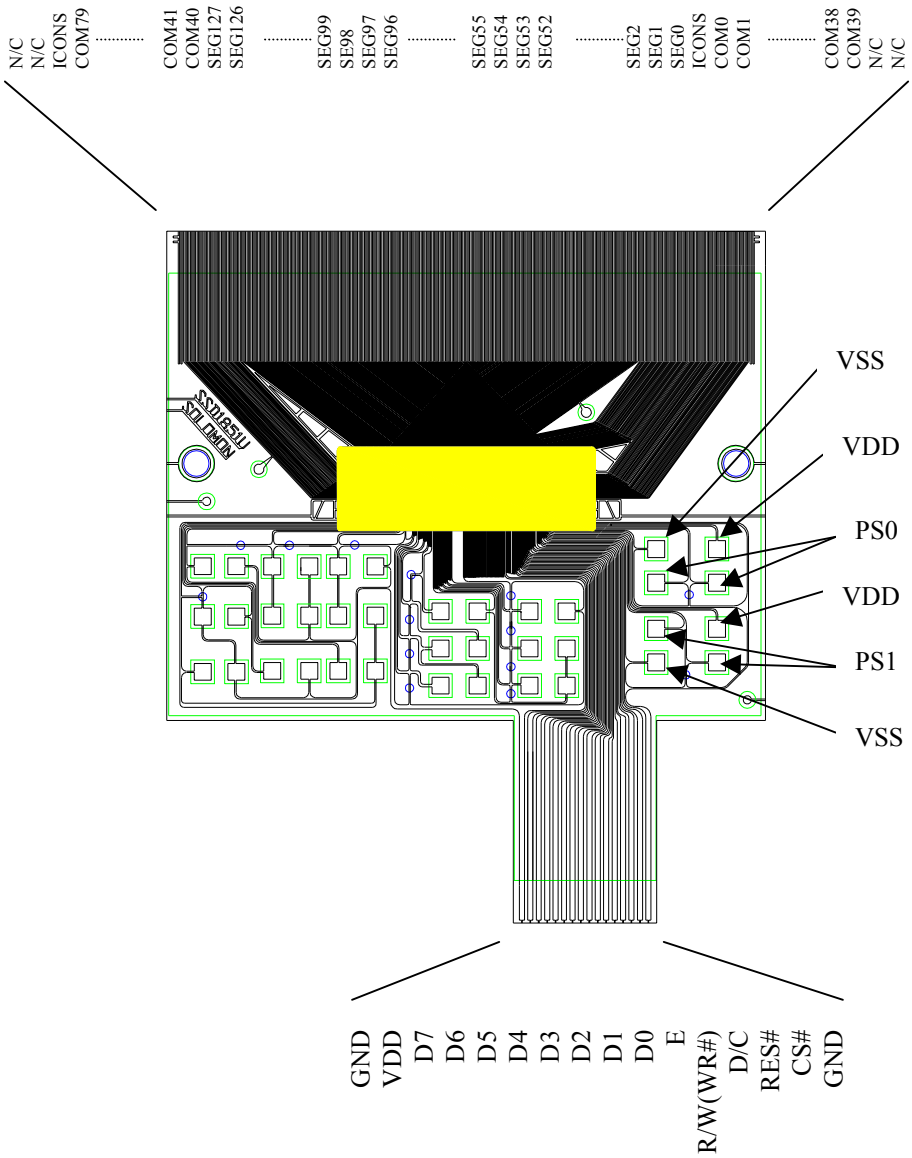
209 COM1
208 COM0
207 ICONS
206 SEG0
205 SEG1

81 SEG125
80 SEG126
79 SEG127
78 COM40
77 COM41

42 COM76
41 COM77
40 COM78
39 COM79
38 ICONS
37 N/C

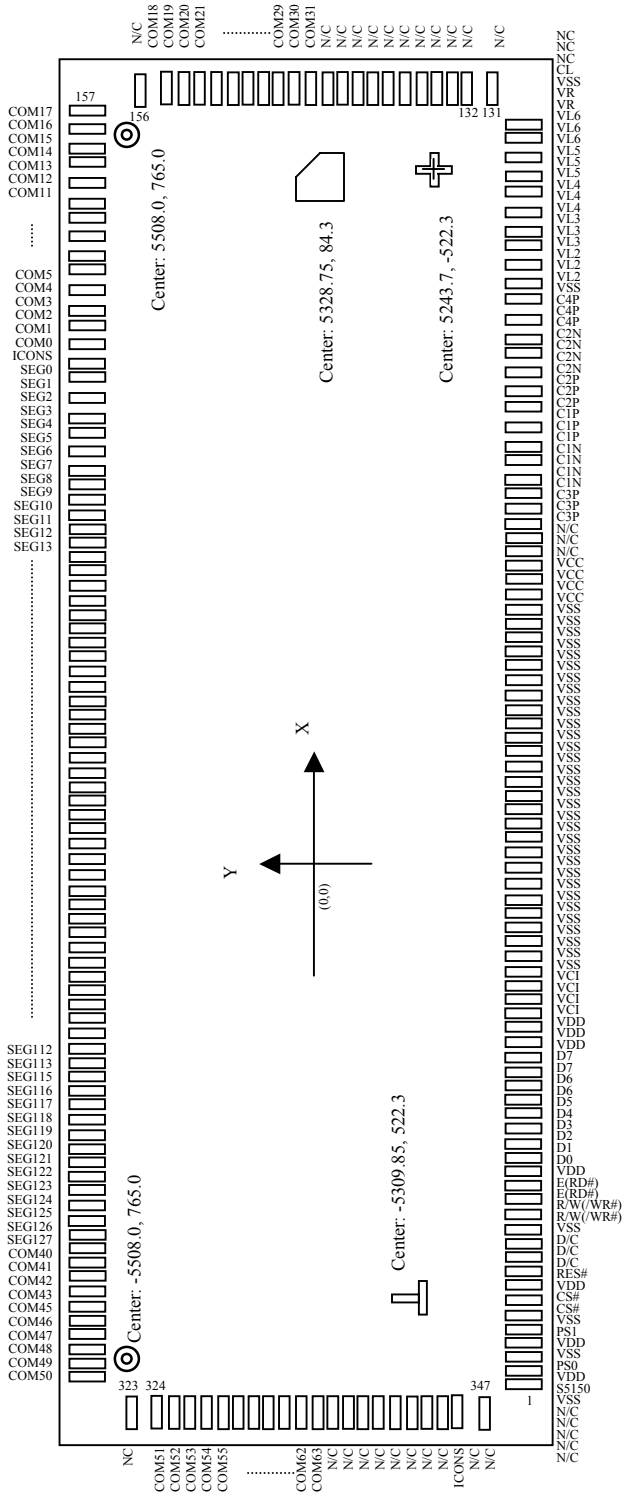
Remarks: REF is connected to VDD
VEXT is not connected

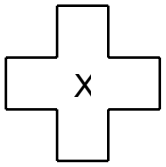
COF PAD ARRAGEMENT (SSD1851U PIN ASSIGNMENT)(Copper View)



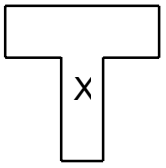
Remarks: **REF is connected to VDD**
VEXT is not connected
INTRS is connected to VDD
VR is not connected
Default Setting: PS0 and PS1 are connected to VDD (6800 Parallel Interface Mode)

DIE PAD ARRAGEMENT (SSD1850Z DIE PIN ASSIGNMENT)

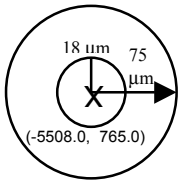


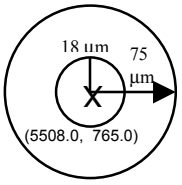


Center (-5243.7, -522.3)
Size: 78.5 x 78.5



Center (-5309.85, -522.3)
Size: 78.5 x 78.5

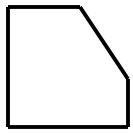




Note:

5. The gold bumps face up in this diagram.
6. Coordinates reference to center of the chip.
7. All dimensions and coordinates in um.
8. All alignment keys do not contain gold bump.

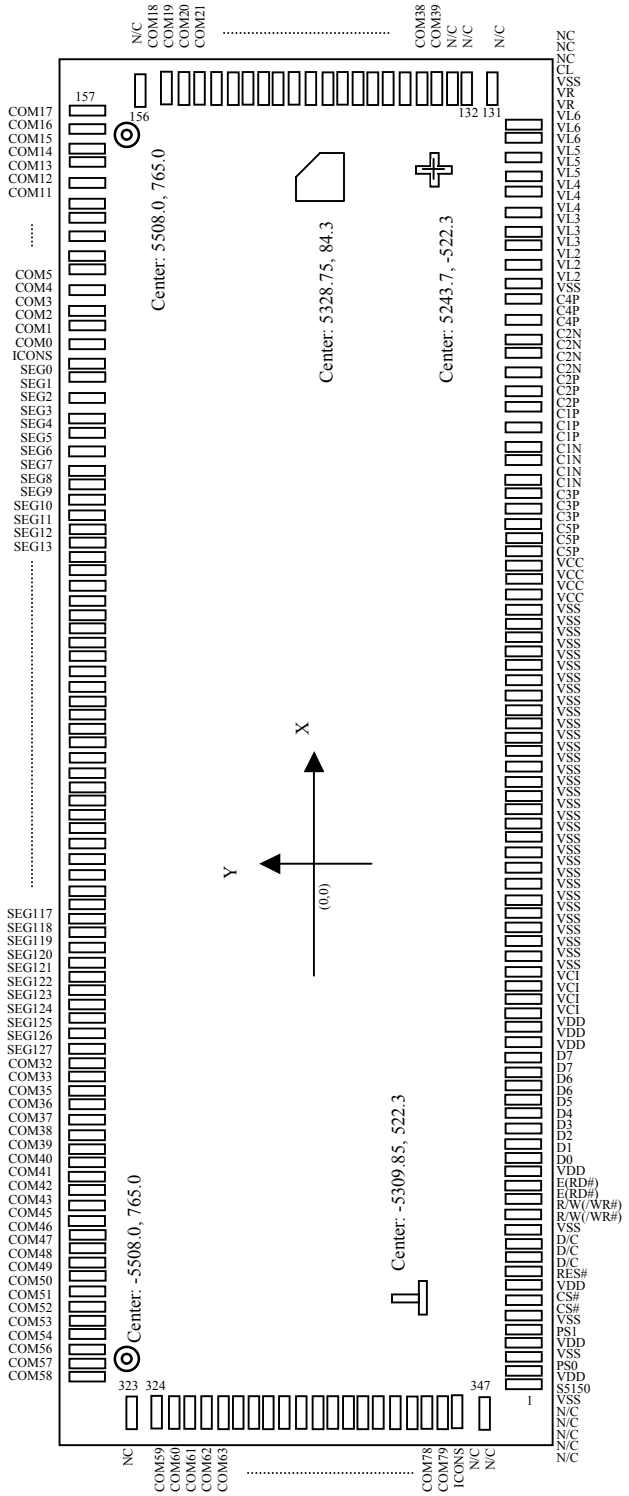
Die Size:	12300um x 1960um
Die Thickness:	534um +/- 25 um
Bump Height:	Nominal 18 um
Tolerance	< 3 um within die

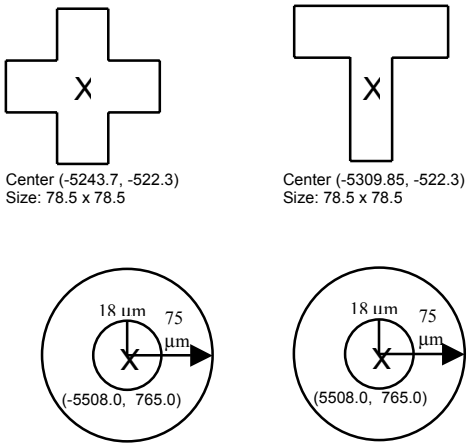


Center (5328.75, 84.3)
Size: 78.5 x 78.5

SSD1850Z Die Pin Assignment
DRAWING NOT SCALE

DIE PAD ARRANGEMENT (SSD1851Z DIE PIN ASSIGNMENT)

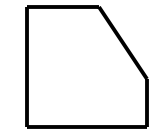




Note:

1. The gold bumps face up in this diagram.
2. Coordinates reference to center of the chip.
3. All dimensions and coordinates in um.
4. All alignment keys do not contain gold bump.

Die Size:	12300um x 1960um
Die Thickness:	534um +/- 25 um
Bump Height:	Nominal 18 um
Tolerance	< 3 um within die



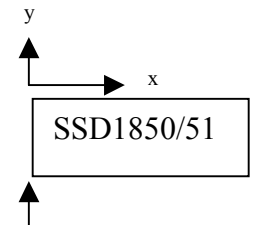
SSD1851Z Die Pin Assignment
DRAWING NOT SCALE

Table 1 - SSD1850/51 Die Pad Coordinates

Pad #	SSD 1851	SSD 1850	X-pos	Y-pos	Pad #	SSD 1851	SSD 1850	X-pos	Y-pos	Pad #	SSD 1851	SSD 1850	X-pos	Y-pos
1	N/C	N/C	-5698.05	-830.85	51	VSS	VSS	-1687.2	-863.55	101	C4P	C4P	3016.05	-804.15
2	N/C	N/C	-5620.65	-830.85	52	VSS	VSS	-1611	-863.55	102	C4P	C4P	3097.35	-804.15
3	N/C	N/C	-5543.25	-830.85	53	VSS	VSS	-1534.8	-863.55	103	VSS	VSS	3173.55	-804.15
4	N/C	N/C	-5465.85	-830.85	54	VSS	VSS	-1458.6	-863.55	104	REF	REF	3249.75	-804.15
5	N/C	N/C	-5355.68	-830.85	55	VSS	VSS	-1382.4	-863.55	105	VEXT	VEXT	3366.45	-804.15
6	VSS	VSS	-5279.48	-830.85	56	VSS	VSS	-1306.2	-863.55	106	VDD	VDD	3442.65	-804.15
7	S5150	S5150	-5203.28	-830.85	57	VSS	VSS	-1230	-863.55	107	INTRS	INTRS	3518.85	-804.15
8	VDD	VDD	-5127.08	-830.85	58	VSS	VSS	-1153.8	-863.55	108	VSS	VSS	3595.05	-804.15
9	PS0	PS0	-5050.88	-830.85	59	VSS	VSS	-1077.6	-863.55	109	VL2	VL2	3671.25	-804.15
10	VSS	VSS	-4974.68	-830.85	60	VSS	VSS	-1001.4	-863.55	110	VL2	VL2	3752.55	-804.15
11	VDD	VDD	-4898.48	-830.85	61	VSS	VSS	-925.2	-863.55	111	VL2	VL2	3833.85	-804.15
12	PS1	PS1	-4822.28	-830.85	62	VSS	VSS	-849	-863.55	112	VL3	VL3	3915.15	-804.15
13	VSS	VSS	-4746.08	-830.85	63	VSS	VSS	-772.8	-863.55	113	VL3	VL3	3996.45	-804.15
14	CS#	CS#	-4669.88	-830.85	64	VSS	VSS	-696.6	-863.55	114	VL3	VL3	4077.75	-804.15
15	CS#	CS#	-4593.68	-830.85	65	VSS	VSS	-620.4	-863.55	115	VL4	VL4	4159.05	-804.15
16	VDD	VDD	-4517.48	-830.85	66	VSS	VSS	-544.2	-863.55	116	VL4	VL4	4240.35	-804.15
17	RES#	RES#	-4441.28	-830.85	67	VSS	VSS	-468	-863.55	117	VL4	VL4	4321.65	-804.15
18	D/C	D/C	-4365.08	-830.85	68	VSS	VSS	-391.8	-863.55	118	VL5	VL5	4402.95	-804.15
19	D/C	D/C	-4288.88	-830.85	69	VSS	VSS	-315.6	-863.55	119	VL5	VL5	4484.25	-804.15
20	D/C	D/C	-4212.68	-830.85	70	VSS	VSS	-239.4	-863.55	120	VL5	VL5	4565.55	-804.15
21	VSS	VSS	-4136.48	-830.85	71	VSS	VSS	-163.2	-863.55	121	VL6	VL6	4646.85	-804.15
22	R/W (WR#)	R/W (WR#)	-4060.28	-830.85	72	VSS	VSS	-87	-863.55	122	VL6	VL6	4728.15	-804.15
23	R/W (WR#)	R/W (WR#)	-3984.08	-830.85	73	VSS	VSS	-10.8	-863.55	123	VL6	VL6	4809.45	-804.15
24	E(RD#)	E(RD#)	-3907.88	-830.85	74	VSS	VSS	65.4	-863.55	124	VR	VR	4926.15	-804.15
25	E(RD#)	E(RD#)	-3831.68	-830.85	75	VSS	VSS	141.6	-863.55	125	VR	VR	5002.35	-804.15
26	VDD	VDD	-3755.48	-830.85	76	VCC	VCC	872.55	-804.15	126	VSS	VSS	5078.55	-804.15
27	D0	D0	-3679.28	-830.85	77	VCC	VCC	953.85	-804.15	127	CL	CL	5154.75	-804.15
28	D1	D1	-3603.08	-830.85	78	VCC	VCC	1035.15	-804.15	128	N/C	N/C	5267.55	-830.85
29	D2	D2	-3526.88	-830.85	79	VCC	VCC	1116.45	-804.15	129	N/C	N/C	5344.95	-830.85
30	D3	D3	-3450.68	-830.85	80	C5P	N/C	1197.75	-804.15	130	N/C	N/C	5422.35	-830.85
31	D4	D4	-3374.48	-830.85	81	C5P	N/C	1279.05	-804.15	131	N/C	N/C	5974.20	-898.05
32	D5	D5	-3298.28	-830.85	82	C5P	N/C	1360.35	-804.15	132	N/C	N/C	5974.20	-665.25
33	D6	D6	-3222.08	-830.85	83	C3P	C3P	1441.65	-804.15	133	N/C	N/C	5974.20	-600.45
34	D6	D6	-3145.88	-830.85	84	C3P	C3P	1522.95	-804.15	134	COM39	N/C	5974.20	-535.65
35	D7	D7	-3069.68	-830.85	85	C3P	C3P	1604.25	-804.15	135	COM38	N/C	5974.20	-470.85
36	D7	D7	-2993.48	-830.85	86	C1N	C1N	1685.55	-804.15	136	COM37	N/C	5974.20	-406.05
37	VDD	VDD	-2917.28	-830.85	87	C1N	C1N	1766.85	-804.15	137	COM36	N/C	5974.20	-341.25
38	VDD	VDD	-2841.08	-830.85	88	C1N	C1N	1848.15	-804.15	138	COM35	N/C	5974.20	-276.45
39	VDD	VDD	-2764.88	-830.85	89	C1N	C1N	1929.45	-804.15	139	COM34	N/C	5974.20	-211.65
40	VCI	VCI	-2620.05	-804.15	90	C1P	C1P	2066.25	-804.15	140	COM33	N/C	5974.20	-146.85
41	VCI	VCI	-2538.75	-804.15	91	C1P	C1P	2147.55	-804.15	141	COM32	N/C	5974.20	-82.05
42	VCI	VCI	-2457.45	-804.15	92	C1P	C1P	2228.85	-804.15	142	COM31	COM31	5974.20	-17.25
43	VCI	VCI	-2376.15	-804.15	93	C2P	C2P	2310.15	-804.15	143	COM30	COM30	5974.20	47.55
44	VSS	VSS	-2266.35	-804.15	94	C2P	C2P	2391.45	-804.15	144	COM29	COM29	5974.20	112.35
45	VSS	VSS	-2190.15	-804.15	95	C2P	C2P	2472.75	-804.15	145	COM28	COM28	5974.20	177.15
46	VSS	VSS	-2113.95	-804.15	96	C2N	C2N	2554.05	-804.15	146	COM27	COM27	5974.20	241.95
47	VSS	VSS	-2037.75	-804.15	97	C2N	C2N	2635.35	-804.15	147	COM26	COM26	5974.20	306.75
48	VSS	VSS	-1961.55	-804.15	98	C2N	C2N	2716.65	-804.15	148	COM25	COM25	5974.20	371.55
49	VSS	VSS	-1885.35	-804.15	99	C2N	C2N	2797.95	-804.15	149	COM24	COM24	5974.20	436.35
50	VSS	VSS	-1763.4	-863.55	100	C4P	C4P	2934.75	-804.15	150	COM23	COM23	5974.20	501.15

Pad #	SSD 1851	SSD 1850	X-pos	Y-pos	Pad #	SSD 1851	SSD 1850	X-pos	Y-pos	Pad #	SSD 1851	SSD 1850	X-pos	Y-pos
151	COM22	COM22	5974.20	565.95	201	SEG25	SEG25	2494.80	788.55	251	SEG75	SEG75	-745.20	788.55
152	COM21	COM21	5974.20	630.75	202	SEG26	SEG26	2430.00	788.55	252	SEG76	SEG76	-810.00	788.55
153	COM20	COM20	5974.20	695.55	203	SEG27	SEG27	2365.20	788.55	253	SEG77	SEG77	-847.80	788.55
154	COM19	COM19	5974.20	760.35	204	SEG28	SEG28	2300.40	788.55	254	SEG78	SEG78	-939.60	788.55
155	COM18	COM18	5974.20	825.15	205	SEG29	SEG29	2235.60	788.55	255	SEG79	SEG79	-1004.40	788.55
156	N/C	N/C	5974.20	889.95	206	SEG30	SEG30	2170.80	788.55	256	SEG80	SEG80	-1069.20	788.55
157	COM17	COM17	5346.00	788.55	207	SEG31	SEG31	2106.00	788.55	257	SEG81	SEG81	-1134.00	788.55
158	COM16	COM16	5281.20	788.55	208	SEG32	SEG32	2041.20	788.55	258	SEG82	SEG82	-1198.80	788.55
159	COM15	COM15	5216.40	788.55	209	SEG33	SEG33	1976.40	788.55	259	SEG83	SEG83	-1263.60	788.55
160	COM14	COM14	5151.60	788.55	210	SEG34	SEG34	1911.60	788.55	260	SEG84	SEG84	-1328.40	788.55
161	COM13	COM13	5086.80	788.55	211	SEG35	SEG35	1846.80	788.55	261	SEG85	SEG85	-1393.20	788.55
162	COM12	COM12	5022.00	788.55	212	SEG36	SEG36	1782.00	788.55	262	SEG86	SEG86	-1458.00	788.55
163	COM11	COM11	4957.20	788.55	213	SEG37	SEG37	1717.20	788.55	263	SEG87	SEG87	-1522.80	788.55
164	COM10	COM10	4892.40	788.55	214	SEG38	SEG38	1652.40	788.55	264	SEG88	SEG88	-1587.60	788.55
165	COM9	COM9	4827.60	788.55	215	SEG39	SEG39	1587.60	788.55	265	SEG89	SEG89	-1652.40	788.55
166	COM8	COM8	4762.80	788.55	216	SEG40	SEG40	1522.80	788.55	266	SEG90	SEG90	-1717.20	788.55
167	COM7	COM7	4698.00	788.55	217	SEG41	SEG41	1458.00	788.55	267	SEG91	SEG91	-1782.00	788.55
168	COM6	COM6	4633.20	788.55	218	SEG42	SEG42	1393.20	788.55	268	SEG92	SEG92	-1846.80	788.55
169	COM5	COM5	4568.40	788.55	219	SEG43	SEG43	1328.40	788.55	269	SEG93	SEG93	-1911.60	788.55
170	COM4	COM4	4503.60	788.55	220	SEG44	SEG44	1263.60	788.55	270	SEG94	SEG94	-1976.40	788.55
171	COM3	COM3	4438.80	788.55	221	SEG45	SEG45	1198.80	788.55	271	SEG95	SEG95	-2041.20	788.55
172	COM2	COM2	4374.00	788.55	222	SEG46	SEG46	1134.00	788.55	272	SEG96	SEG96	-2106.00	788.55
173	COM1	COM1	4309.20	788.55	223	SEG47	SEG47	1096.20	788.55	273	SEG97	SEG97	-2170.80	788.55
174	COM0	COM0	4244.40	788.55	224	SEG48	SEG48	1004.40	788.55	274	SEG98	SEG98	-2235.60	788.55
175	ICONS	ICONS	4179.60	788.55	225	SEG49	SEG49	939.60	788.55	275	SEG99	SEG99	-2300.40	788.55
176	SEG0	SEG0	4114.80	788.55	226	SEG50	SEG50	874.80	788.55	276	SEG100	SEG100	-2365.20	788.55
177	SEG1	SEG1	4050.00	788.55	227	SEG51	SEG51	810.00	788.55	277	SEG101	SEG101	-2430.00	788.55
178	SEG2	SEG2	3985.20	788.55	228	SEG52	SEG52	745.20	788.55	278	SEG102	SEG102	-2494.80	788.55
179	SEG3	SEG3	3920.40	788.55	229	SEG53	SEG53	680.40	788.55	279	SEG103	SEG103	-2559.60	788.55
180	SEG4	SEG4	3855.60	788.55	230	SEG54	SEG54	615.60	788.55	280	SEG104	SEG104	-2624.40	788.55
181	SEG5	SEG5	3790.80	788.55	231	SEG55	SEG55	550.80	788.55	281	SEG105	SEG105	-2689.20	788.55
182	SEG6	SEG6	3726.00	788.55	232	SEG56	SEG56	486.00	788.55	282	SEG106	SEG106	-2754.00	788.55
183	SEG7	SEG7	3661.20	788.55	233	SEG57	SEG57	421.20	788.55	283	SEG107	SEG107	-2818.80	788.55
184	SEG8	SEG8	3596.40	788.55	234	SEG58	SEG58	356.40	788.55	284	SEG108	SEG108	-2883.60	788.55
185	SEG9	SEG9	3531.60	788.55	235	SEG59	SEG59	291.60	788.55	285	SEG109	SEG109	-2948.40	788.55
186	SEG10	SEG10	3466.80	788.55	236	SEG60	SEG60	226.80	788.55	286	SEG110	SEG110	-3013.20	788.55
187	SEG11	SEG11	3402.00	788.55	237	SEG61	SEG61	162.00	788.55	287	SEG111	SEG111	-3078.00	788.55
188	SEG12	SEG12	3337.20	788.55	238	SEG62	SEG62	97.20	788.55	288	SEG112	SEG112	-3142.80	788.55
189	SEG13	SEG13	3272.40	788.55	239	SEG63	SEG63	32.40	788.55	289	SEG113	SEG113	-3207.60	788.55
190	SEG14	SEG14	3207.60	788.55	240	SEG64	SEG64	-32.40	788.55	290	SEG114	SEG114	-3272.40	788.55
191	SEG15	SEG15	3142.80	788.55	241	SEG65	SEG65	-97.20	788.55	291	SEG115	SEG115	-3337.20	788.55
192	SEG16	SEG16	3078.00	788.55	242	SEG66	SEG66	-162.00	788.55	292	SEG116	SEG116	-3402.00	788.55
193	SEG17	SEG17	3013.20	788.55	243	SEG67	SEG67	-226.80	788.55	293	SEG117	SEG117	3466.80	788.55
194	SEG18	SEG18	2948.40	788.55	244	SEG68	SEG68	-291.60	788.55	294	SEG118	SEG118	-3531.60	788.55
195	SEG19	SEG19	2883.60	788.55	245	SEG69	SEG69	-356.40	788.55	295	SEG119	SEG119	-3596.40	788.55
196	SEG20	SEG20	2818.80	788.55	246	SEG70	SEG70	-421.20	788.55	296	SEG120	SEG120	-3661.20	788.55
197	SEG21	SEG21	2754.00	788.55	247	SEG71	SEG71	-486.00	788.55	297	SEG121	SEG121	-3726.00	788.55
198	SEG22	SEG22	2689.20	788.55	248	SEG72	SEG72	-550.80	788.55	298	SEG122	SEG122	-3790.80	788.55
199	SEG23	SEG23	2624.40	788.55	249	SEG73	SEG73	-615.60	788.55	299	SEG123	SEG123	-3855.60	788.55
200	SEG24	SEG24	2559.60	788.55	250	SEG74	SEG74	-680.40	788.55	300	SEG124	SEG124	-3920.40	788.55

Pad #	SSD 1851	SSD 1850	X-pos	Y-pos
301	SEG125	SEG125	-3985.20	788.55
302	SEG126	SEG126	-4050.00	788.55
303	SEG127	SEG127	-4114.80	788.55
304	COM40	COM32	-4179.60	788.55
305	COM41	COM33	-4244.40	788.55
306	COM42	COM34	-4309.20	788.55
307	COM43	COM35	-4374.00	788.55
308	COM44	COM36	-4438.80	788.55
309	COM45	COM37	-4503.60	788.55
310	COM46	COM38	-4568.40	788.55
311	COM47	COM39	-4633.20	788.55
312	COM48	COM40	-4698.00	788.55
313	COM49	COM41	-4762.80	788.55
314	COM50	COM42	-4827.60	788.55
315	COM51	COM43	-4892.40	788.55
316	COM52	COM44	-4957.20	788.55
317	COM53	COM45	-5022.00	788.55
318	COM54	COM46	-5086.80	788.55
319	COM55	COM47	-5151.60	788.55
320	COM56	COM48	-5216.40	788.55
321	COM57	COM49	-5281.20	788.55
322	COM58	COM50	-5346.00	788.55
323	N/C	N/C	-5974.20	889.95
324	COM59	COM51	-5974.20	825.15
325	COM60	COM52	-5974.20	760.35
326	COM61	COM53	-5974.20	695.55
327	COM62	COM54	-5974.20	630.75
328	COM63	COM55	-5974.20	565.95
329	COM64	COM56	-5974.20	501.15
330	COM65	COM57	-5974.20	436.35
331	COM66	COM58	-5974.20	371.55
332	COM67	COM59	-5974.20	306.75
333	COM68	COM60	-5974.20	241.95
334	COM69	COM61	-5974.20	177.15
335	COM70	COM62	-5974.20	112.35
336	COM71	COM63	-5974.20	47.55
337	COM72	N/C	-5974.20	-17.25
338	COM73	N/C	-5974.20	-82.05
339	COM74	N/C	-5974.20	-146.85
340	COM75	N/C	-5974.20	-211.65
341	COM76	N/C	-5974.20	-276.45
342	COM77	N/C	-5974.20	-341.25
343	COM78	N/C	-5974.20	-406.05
344	COM79	N/C	-5974.20	-470.85
345	ICONS	ICONS	-5974.20	-535.65
346	N/C	N/C	-5974.20	-600.45
347	N/C	N/C	-5974.20	-898.05



Pad 1 to 130

Bump Size

PAD#	X [um]	Y [um]
1 – 130	52.2	60
131 – 156	75	45
323 – 347	75	45
157 – 322	45	75

PIN DESCRIPTIONS

$\overline{\text{RES}}$
This pin is reset signal input. When the pin is low, initialization of the chip is executed.

PS0, PS1
PS0 and PS1 determine the interface protocol between the driver and MCU. Refer to the following table for details.

PS0	PS1	Interface
L	L	3-wire SPI (write only)
L	H	4-wire SPI (write only)
H	L	8080 parallel interface (read and write allowed)
H	H	6800 parallel interface (read and write allowed)

$\overline{\text{CS}}$
This pin is chip select input. The chip is enabled for display data/command transfer only when $\overline{\text{CS}}$ is low.

D/$\overline{\text{C}}$
This input pin is to identify display data/command cycle. When the pin is high, the data written to the driver will be written into display RAM. When the pin is low, the data will be interpreted as command. This pin must be connected to VSS when 3-lines SPI interface is used.

R/$\overline{\text{W}}$ ($\overline{\text{WR}}$)
This pin is microprocessor interface signal. When 6800 interface mode is selected (by PS0 and PS1), the signal indicates read mode when high and write mode when low. When 8080 interface mode is selected (by PS0 and PS1), a data write operation is initiated when R/$\overline{\text{W}}$($\overline{\text{WR}}$) is low and the chip is selected.

E($\overline{\text{RD}}$)
This pin is microprocessor interface signal. When 6800 interface mode is selected (by PS0 and PS1), a data operation is initiated when E($\overline{\text{RD}}$) is high and the chip is selected. When 8080 interface mode is selected (PS0 and PS1), a data read operation is initiated when E($\overline{\text{RD}}$) is low and the chip is selected.

D0-D7
These pins are 8-bit bi-directional data/command bus to be connected to the microprocessor's data bus. When serial mode is selected, D7 is the serial data input SDA and D6 is the serial clock input SCK.

INTRS
This pin is an input pin to enable the internal resistor network for the voltage regulator when INTRS is high. When external regulator is used, this pin must be connected to VSS, and external resistor R1/R2 should be connected to VL6, VR and VSS.

REF
This pin is an input pin to enable the internal reference voltage used for the internal regulator. When it is high, an internal reference voltage source will be used. When it is low, an external reference voltage source must be provided to VEXT pin if internal regulator is used.

VDD
Power supply pin.

VSS
Ground.

VCI
Reference voltage input for internal DC-DC converter. The voltage of generated VCC equals to the multiple factor (2X, 3X, 4X, 5X or 6X) times VCI with respect to VSS.
Note: voltage at this input pin must be larger than or equal to VDD. 6x is available for SSD1851 only.

VCC
This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter.
When using internal DC-DC converter as generator, voltage at this pin is for internal reference only. It CANNOT be used for driving external circuitries.

C1P, C2P, C3P, C4P, C5P, C1N and C2N
When internal DC-DC voltage converter is used, external capacitor(s) is/are connected to these pins. (Reference to application Circuit on P.42)

VL6
This pin is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

VR
This pin is an input of the internal voltage regulator. When the internal resistors network for the voltage regulator is disabled (INTRS is pulled low), external resistors should be connected between VSS and VR, and VR and VL6, respectively (Please refer to application circuit on P.43).

VEXT
This pin is an input to provide an external voltage reference for the internal voltage regulator when REF pin is pulled L.

VL5, VL4, VL3 and VL2
These are LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:
VL6 > VL5 > VL4 > VL3 > VL2 > VSS

	1:a bias
VL5	(a-1)/a*VL6
VL4	(a-2)/a*VL6
VL3	2/a*VL6
VL2	1/a*VL6

For SSD1851, “a” equals to 10 at POR.
For SSD1850, “a” equals to 9 at POR.

COM0 - COM79
These pins provide the row driving signal COM0 - COM79 to the LCD panel.

ICONS
This pin is the special icon line COM signal output.

SEG0 - SEG127
These pins provide the LCD column driving signal. Their voltage level is VSS during sleep mode and standby mode.

S5150
For SSD1851, this pin must be connected to VSS.
For SSD1850, this pin must be connected to VDD.

CL
This pin is the external clock input for the device if external clock mode is selected by software command. Under POR operation, this pin should be left opened and internal oscillator will be used after power on reset.

N/C
These No Connection pins should NOT be connected to any signal pins nor shorted together. They should be left open.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ is high, data is written to Graphic Display Data RAM (GDDRAM). If D/$\overline{C}$ is low, the input at D_0-D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once $\overline{RES}$ receives a negative reset pulse of about 1us, all internal circuitry will be back to its initial status. Refer to Command Description section for more information.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, E($\overline{RD}$) and $\overline{CS}$.

R/$\overline{W}$($\overline{WR}$) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$($\overline{WR}$) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E($\overline{RD}$) and $\overline{CS}$ input serves as data latch signal (clock) when they are high and low respectively. Refer to P.35, Figure 1 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 4 below.

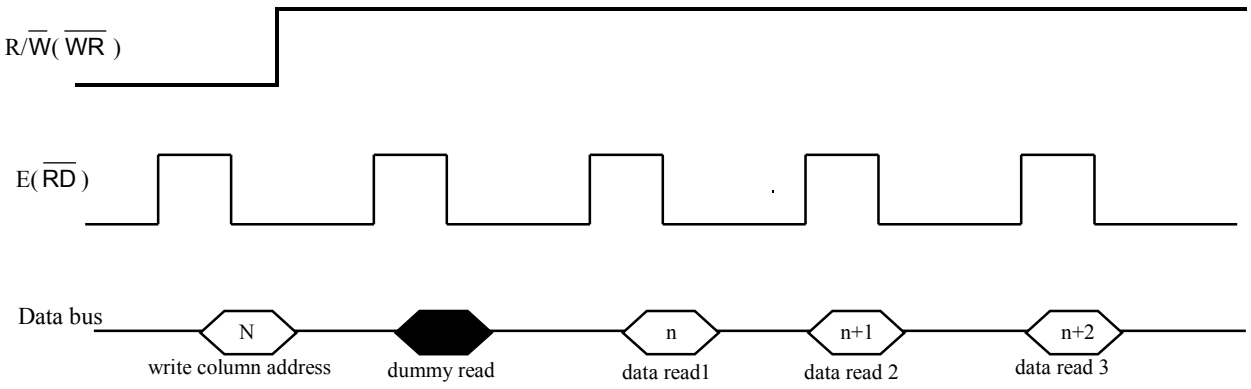


Figure 4 - display data read with the insertion of dummy read

MPU Parallel 8080-series interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{W}$($\overline{WR}$), E($\overline{RD}$), D/$\overline{C}$ and $\overline{CS}$. The $\overline{CS}$ input serves as data latch signal (clock) when it is low. Whether it is display data or status register read is controlled by D/$\overline{C}$. R/$\overline{W}$($\overline{WR}$) and E($\overline{RD}$) input indicate a write or read cycle when $\overline{CS}$ is low. Refer to P.37, Figure 2 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial 4-wire Interface

The serial interface consists of serial clock SCK, serial data SDA, $D/\overline{C}$ and $\overline{CS}$. Input to SDA is shifted into a 8-bit shift register on every rising edge of SCK in the order of D_7, D_6,...D_0. $D/\overline{C}$ is sampled on every eighth clock and the content in the shift register is written to the Display Data RAM or command register in the same clock. No extra clock or command is required to end the transmission.

MPU Serial 3-wire Interface

Operation is similar to 4-wire serial interface except $D/\overline{C}$ is not used. The Set Display Data Length command is used to indicate that a specified number display data byte (1-256) is to be transmitted. Next byte after the display data string is handled as a command.
It should be noted that if there is a signal glitch at SCK that causing an out of synchronization in the serial communication, a hardware reset pulse at $\overline{RES}$ pin is required to initialize the chip for re-synchronization.

Modes of operation

	6800 parallel	8080 parallel	Serial
Data Read	Yes	Yes	No
Data Write	Yes	Yes	Yes
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 81 x 2 = 20736bits. Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, remapping on both Segment and Common outputs are provided respectively. For vertical scrolling of display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5a and 5b show the cases in which the display start line register are set at 38H or 48H.

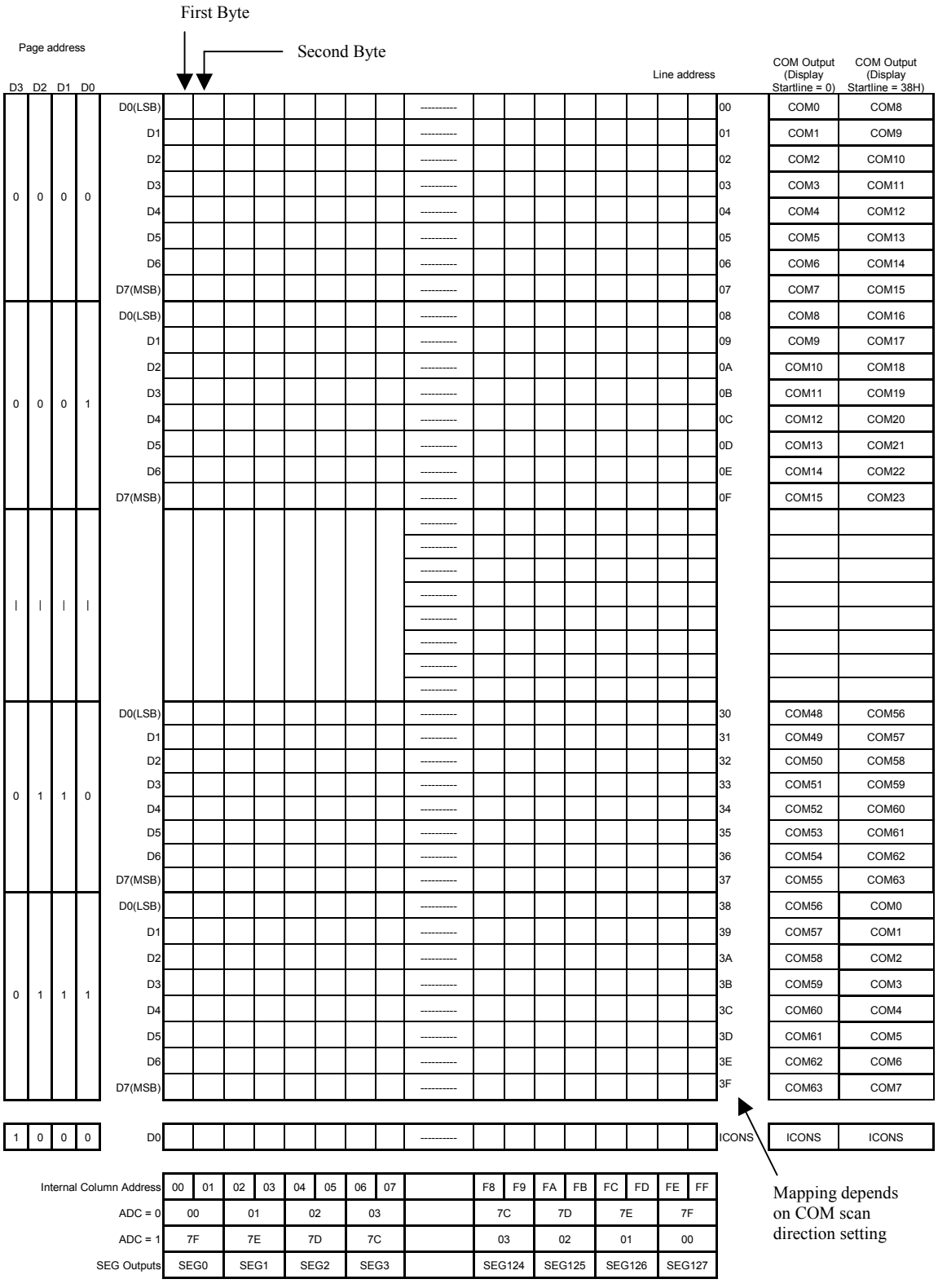


Figure 5a. Graphic Display Data RAM (GDDRAM) Address Map for SSD1850 (with vertical scroll value 38H)

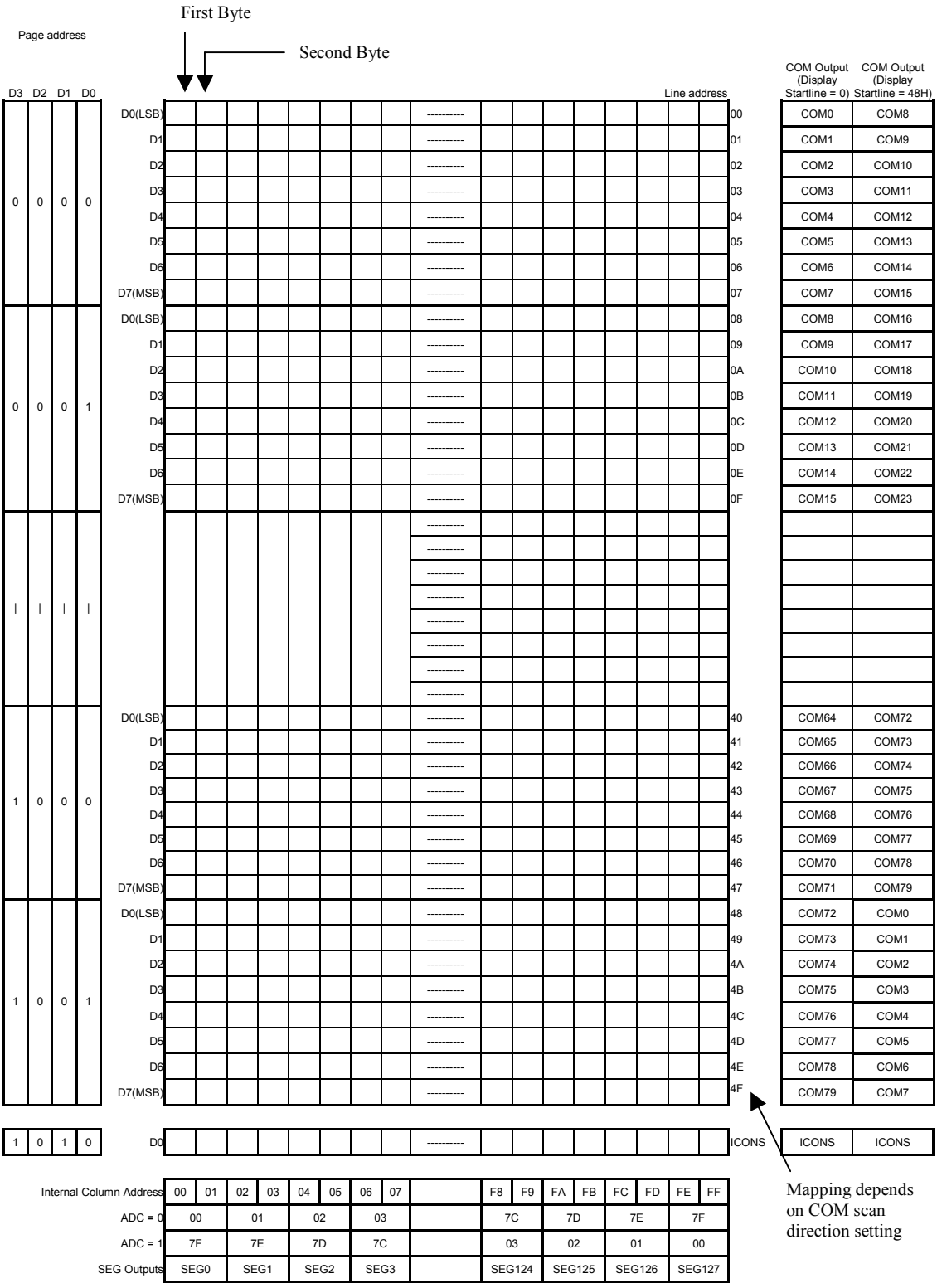


Figure 5b. Graphic Display Data RAM (GDDRAM) Address Map for SSD1851 (with vertical scroll value 48H)

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

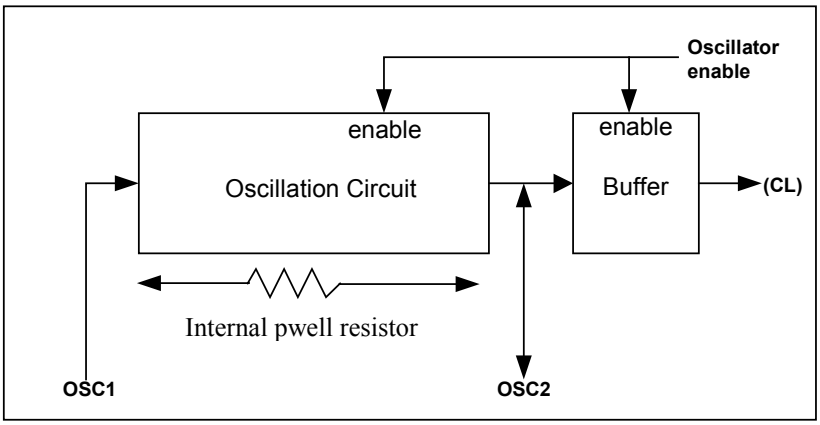


Figure 6. Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 2X, 3X, 4X, 5X and 6X DC-DC voltage converter
*Note: SSD1850 works up to 5X only.
Please refer to application notes on P.42.

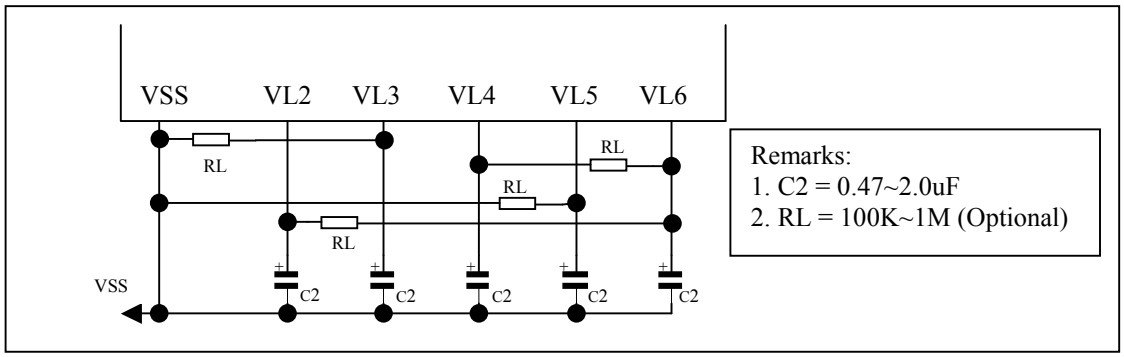
2. Voltage Regulator
Feedback gain control for initial LCD voltage. External resistors are connected between VSS and VR, and between VR and VL6. These resistors are chosen to give the desired VL6 according to the following equations:

$$V_{L6} = \left(1 + \frac{R_2}{R_1}\right) * V_{con} * G$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref}$$

where Vref is the internally generated reference voltage with a known R1 and R2. Typical value for Vref is 2.1V
R1 is the resistance of the resistor between VSS and VR.
R2 is the resistance of the resistors between VR and VL6.
α is the software contrast level from 0 to 63.
G = 1 if INTRS = VDD; REF = VDD
G = 0.80 if INTRS = VSS; REF = VDD

3. Bias Divider
If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (VL6) to give the LCD driving levels (VL2 -VL5).
A low power consumption circuit design in this bias divider saves most of the display current comparing to traditional design.
Stabilizing Capacitors (0.47~2uF) are required to be connected between these voltage level pins (VL2 - VL5) and VSS. If the LCD panel loading is heavy, four additional resistors are suggested to add to the application circuit as following:



Connections for heavy loading applications

4. Contrast Control
Software control of 64 voltage levels of LCD voltage.

5. Bias Ratio Selection circuitry
Software control of 1/4 to 1/10 bias ratio to match the characteristic of LCD panel.
Note: SSD1850 has 1/4 to 1/9 bias only.

6. Self adjust temperature compensation circuitry
Provide 2 different temperature compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
Default temperature coefficient (TC) value is -0.05%/°C.

193 / 209 Bit Latch
A register carries the display signal information. In 128X65/81 display mode, data will be fed to the HV-buffer Cell and level-shifted to the required level.

Level Selector
Level Selector is a control of the display synchronization.
Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)
HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Reset Circuit

When $\overline{RES}$ input is low, the chip is initialized to the following:

1. Page address is set to 0
2. Column address is set to 0
3. Display is OFF
4. Display Start Line is set to 0 (GDDRAM page 0, D0)
5. Display Offset is set to 0 (COM0 is mapped to ROW0)
6. 128x80 display mode for SSD1851 and 128x64 display mode for SSD1850.
7. Normal/Reverse Display is Normal
8. N-line Inversion Register is 0
9. Entire Display is OFF
10. Power Control Register (VC, VR, VF) is set to (0,0,0)
11. 3X Booster is selected
12. Internal Resistor Ratio register is set to 0H
13. Software Contrast is set to 32
14. LCD Bias Ratio is set to 1/10 for SSD1851 and 1/9 for SSD1850.
15. Normal scan direction of COM outputs
16. Segment remap is disabled (SEG0 display column address 0)
17. Internal oscillator is OFF
18. Test mode is OFF
19. Temperature coefficient is set to PTC0 (-0.05%)
20. Icon display line is OFF

When RESET command is issued, the following parameters are initialized only:

1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to 0H
5. Software Contrast is set to 32

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 7a and 7b illustrate the desired multiplex scheme with N-line Inversion feature is disabled (default).

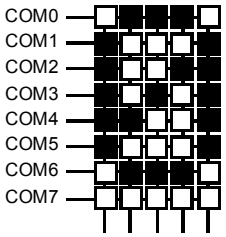
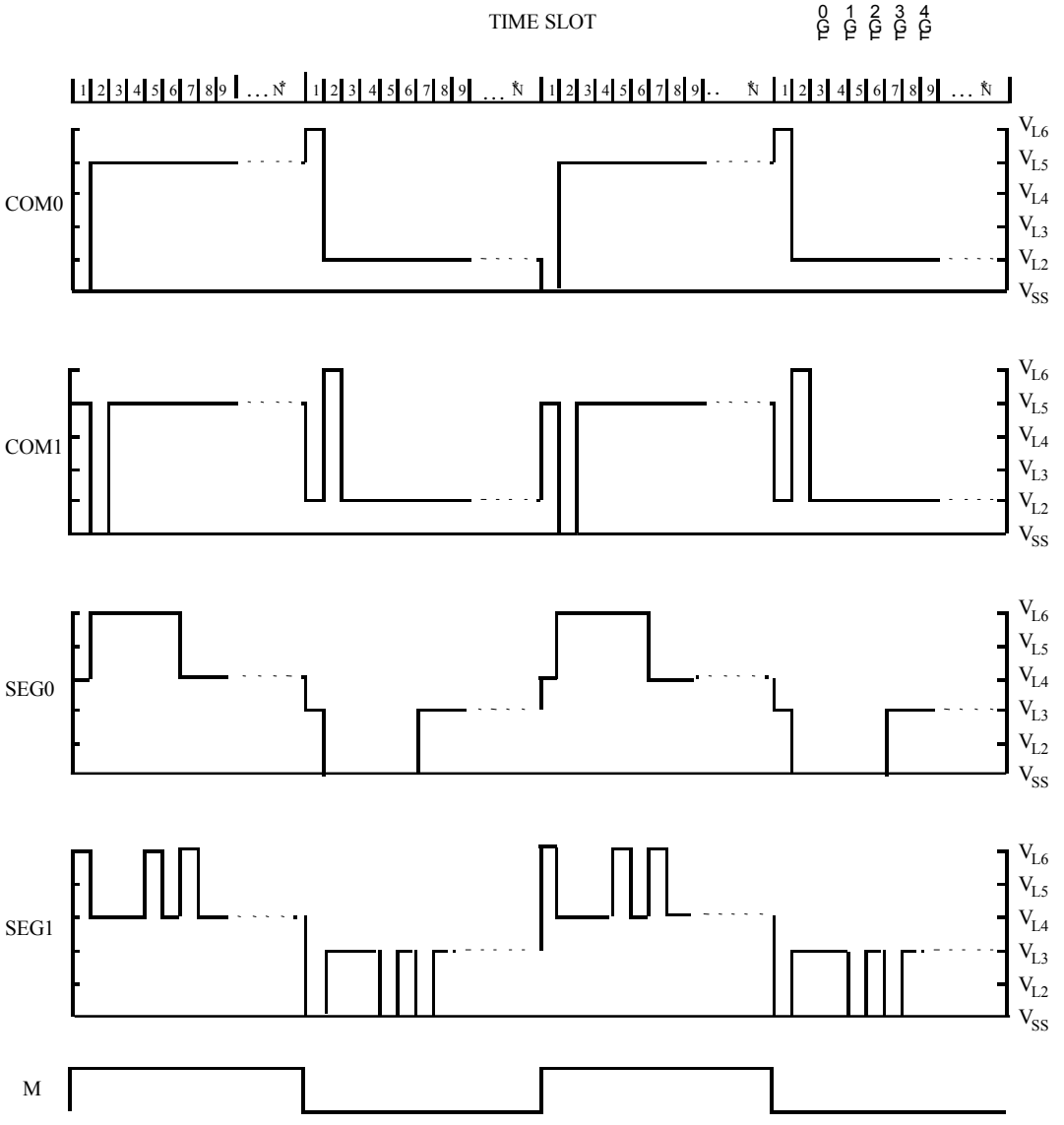


Figure 7a. LCD Display Example "0"



* Note: N is the number of multiplex ratio including Icon line. If it is enabled, N is equal to 80 for SSD1851 and 64 for SSD1850 on POR

Figure 7b. LCD Driving Signal From SSD1850/51

COMMAND TABLE

Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
00~0F	0	0	0	0	C3	C2	C1	C0	Set Lower Column Address	Set the lower nibble of the column address pointer for RAM access. The pointer is reset to 0 after rest.
10~17	0	0	0	1	0	C6	C5	C4	Set Upper Column Address	Set the upper nibble of the column address pointer for RAM access. The pointer is reset to 0 after rest.
18~1F									Reserved	Reserved
20~27	0	0	1	0	0	R2	R1	R0	Set Internal Regulator Resistor Ratio	The internal regulator gain (1+R2/R1)Vcon increases as R2R1R0 is increased from 000b to 111b. The factor, 1+R2/R1, is given by: R2R1R0 = 000: 2.3 (POR) R2R1R0 = 001: 3.0 R2R1R0 = 010: 3.7 R2R1R0 = 011: 4.4 R2R1R0 = 100: 5.1 R2R1R0 = 101: 5.8 R2R1R0 = 110: 6.5 R2R1R0 = 111: 7.2
28~2F	0	0	1	0	1	VC	VR	VF	Set Power Control Register	VC=0: turns OFF the internal voltage booster (POR) VC=1: turns ON the internal voltage booster VR=0: turns OFF the internal regulator (POR) VR=1: turns ON the internal regulator VF=0: turns OFF the output op-amp buffer (POR) VF=1: turns ON the output op-amp buffer
30~3F									Reserved	Reserved
40~43	0 X	1 L6	0 L5	0 L4	0 L3	0 L2	X L1	X L0	Set Display Start Line	The next command specifies the row address pointer (0-79) of the RAM data to be displayed in COM0. This command has no effect on ICONS. The pointer is set to 0 after reset.
44~47	0 X	1 C6	0 C5	0 C4	0 C3	1 C2	X C1	X C0	Set Display Offset	The next command specifies the mapping of first display line (COM0) to one of ROW0~79 (SSD1851) or (COM0) to one of ROW0~63 (SSD1850). This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.
48~4B	0 X	1 D6	0 D5	0 D4	1 D3	0 D2	X D1	X D0	Set Multiplex Ratio	The next command specifies the number of lines, excluding ICONS, to be displayed. With Icon is disabled (POR), duties 1/16~1/80 (SSD1851) or 1/16~1/64 (SSD1850) could be selected. With Icon enabled, the available duty ratios are 1/17~ 1/81 (SSD1851) or 1/17~1/65 (SSD1850).
4C~4F	0 X	1 X	0 X	0 N4	1 N3	1 N2	X N1	X N0	Set N-line Inversion	The next command sets the n-line inversion register from 3 to 33 lines to reduce display crosstalk. Register values from 00001b to 11111b are

										mapped to 3 lines to 33 lines respectively. Value 00000b disables the N-line inversion, which is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
50~56	0	1	0	1	0	B2	B1	B0	Set LCD Bias	Sets the LCD bias from 1/4 ~ 1/10 according to B2B1B0: 000: 1/4 bias 001: 1/5 bias 010: 1/6 bias 011: 1/7bias 100: 1/8 bias 101: 1/9 bias (POR for SSD1850) 110: 1/9 bias (SSD1850); 1/10 bias (POR for SSD1851)
57~63									Reserved	Reserved
64~67	0	1	1	0	0	1	B1	B0	Set DC-DC Converter Factor	Sets the DC-DC multiplying factor from 2X to 6X B1B0: 00: 2X/3X (POR, 2X or 3X multiplying depended on the DC-DC converter hardware configuration) 01: 4X 10: 5X 11: 5X (SSD1850); 6X (SSD1851)
68~80									Reserved	Reserved
81	1 X	0 X	0 C5	0 C4	0 C3	0 C2	0 C1	1 C0	Set Contrast Control Register	The next command sets one of the 64 contrast levels. The darkness increase as the contrast level increase. The level is set to 32 after POR.
82	1 1	0 1	0 1	0 1	0 X3	0 X2	1 X1	0 X0	OTP Setting	Set the desired VL6 voltage value: 0000: original contrast 0001: original contrast +1 step 0010: original contrast +2 steps 0011: original contrast +3 steps 0100: original contrast +4 steps 0101: original contrast +5 steps 0110: original contrast +6 steps 0111: original contrast +7 steps 1000: original contrast -8 steps 1001: original contrast -7 steps 1010: original contrast -6 steps 1011: original contrast -5 steps 1100: original contrast -4 steps 1101: original contrast -3 steps 1110: original contrast -2 steps 1111: original contrast -1 step
83	1	0	0	0	0	0	1	1	OTP Programming	Please refer the sequence of OTP programming
84~87									Reserved	Reserved
88	1 WB3	0 WB2	0 WB1	0 WB0	1 WA3	0 WA2	0 WA1	0 WA0	Set White mode, Frame 2nd & 1st	Set gray scale mode and register. These are two-byte commands used to specify the contrast levels for the gray scale, 4 levels available. After power on reset,
89	1 WD3	0 WD2	0 WD1	0 WD0	1 WC3	0 WC2	0 WC1	1 WC0	Set White mode, Frame 4th & 3rd	

<table>
<tr><td>8A</td><td>1
LB3</td><td>0
LB2</td><td>0
LB1</td><td>0
LB0</td><td>1
LA3</td><td>0
LA2</td><td>1
LA1</td><td>0
LA0</td><td>Set Light Gray mode, Frame 2nd & 1st</td><td rowspan="7">WA0~3 = WB0~3 = WC0~3 = WD0~3 = 0000
LA0~3 = LB0~3 = LC0~3 = LD0~3 = 0000
DA0~3 = DB0~3 = DC0~3 = DD0~3 = 1111
BA0~3 = BB0~3 = BC0~3 = BD0~3 = 1111

<table><tr><th colspan="2">Memory Content</th><th rowspan="2">Gray Mode</th></tr><tr><th>1st Byte</th><th>2nd Byte</th></tr><tr><td>0</td><td>0</td><td>White</td></tr><tr><td>0</td><td>1</td><td>Light Gray</td></tr><tr><td>1</td><td>0</td><td>Dark Gray</td></tr><tr><td>1</td><td>1</td><td>Black</td></tr></table></td></tr>
<tr><td>8B</td><td>1
LD3</td><td>0
LD2</td><td>0
LD1</td><td>0
LD0</td><td>1
LC3</td><td>0
LC2</td><td>1
LC1</td><td>1
LC0</td><td>Set Light Gray mode, Frame 4th & 3rd</td></tr>
<tr><td>8C</td><td>1
DB3</td><td>0
DB2</td><td>0
DB1</td><td>0
DB0</td><td>1
DA3</td><td>1
DA2</td><td>0
DA1</td><td>0
DA0</td><td>Set Dark Gray mode, Frame 2nd & 1st</td></tr>
<tr><td>8D</td><td>1
DD3</td><td>0
DD2</td><td>0
DD1</td><td>0
DD0</td><td>1
DC3</td><td>1
DC2</td><td>0
DC1</td><td>1
DC0</td><td>Set Dark Gray mode, Frame 4th & 3rd</td></tr>
<tr><td>8E</td><td>1
BB3</td><td>0
BB2</td><td>0
BB1</td><td>0
BB0</td><td>1
BA3</td><td>1
BA2</td><td>1
BA1</td><td>0
BA0</td><td>Set Black mode, Frame 2nd & 1st</td></tr>
<tr><td>8F</td><td>1
BD3</td><td>0
BD2</td><td>0
BD1</td><td>0
BD0</td><td>1
BC3</td><td>1
BC2</td><td>1
BC1</td><td>1
BC0</td><td>Set Black mode, Frame 4th & 3rd</td></tr>
<tr><td>90~97</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>FRC</td><td>PWM1</td><td>PWM0</td><td>Set PWM and FRC</td><td>Sets PWM and FRC for gray-scale operation.
FRC = 0 : 4-frame (POR)
FRC = 1 : 3-frame
PWM1 PWM0 = 00 & 01 : 9-levels (POR)
PWM1 PWM0 = 10 : 12-levels
PWM1 PWM0 = 11 : 15-levels</td></tr>
<tr><td>98~9F</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>A0~A1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>S0</td><td>Set Segment Re-map</td><td>S0=0: column address 00H is mapped to SEG0 (POR)
S0=1: column address 7FH is mapped to SEG0</td></tr>
<tr><td>A2~A3</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C0</td><td>Set Icon Enable</td><td>C0=0: Disable icon row (Mux = 16 to 80/64, POR)
C0=1: Enable icon row (Mux = 17 to 81/65)</td></tr>
<tr><td>A4~A5</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>E0</td><td>Set Entire Display On/Off</td><td>E0=0: Normal display (display according to RAM contents, POR)
E0=1: All pixels are ON regardless of the RAM contents
*Note: This command will override the effect of “Set Normal/Inverse Display”</td></tr>
<tr><td>A6~A7</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>R0</td><td>Set Normal/Inverse Display</td><td>R0=0: Normal display (display according to RAM contents, POR)
R0=1: Inverse display (ON and OFF pixels are inverted)
*Note: This command will not affect the display of the icon line</td></tr>
<tr><td>A8~A9</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>S0</td><td>Set Power Save Mode</td><td>S0=0: Standby mode (POR)
S0=1: Sleep mode</td></tr>
<tr><td>AA</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>AB</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Start Internal Oscillator</td><td>Oscillator is OFF, after reset, until this command is issued.</td></tr>
<tr><td>AC~AD</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>AE~AF</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>D0</td><td>Set Display On/Off</td><td>D0=0: Display OFF (POR)
D0=1: Display ON</td></tr>
</table>

B0~BF	1	0	1	1	P3	P2	P1	P0	Set Page Address	Set GDDRAM page address (0~10) using P3P2P1P0 for RAM access. The page address is sets to 0 after reset.
C0~CF	1	1	0	0	S0	X	X	X	Set COM Output Scan Direction	S0=0: Normal mode (POR) S0=1: Remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 when the duty is set to N. See Figure 5 as an example for N equals to 80. *Note: This command will not affect the display of the icon lines
D0~E0									Reserved	Reserved
E1	1	1	1	0	0	0	0	1	Exit Power-save Mode	DC-DC converter, regulator and divider status before entering the power-save mode is restored. At POR, Power-save Mode is released.
E2	1	1	1	0	0	0	1	0	Software Reset	Initialize some internal registers
E3									Reserved	Reserved
E4	1	1	1	0	0	1	0	0	Exit N-line Inversion	The frame will be inverted once per frame
E5~E7									Reserved	Reserved
E8	1 D7	1 D6	1 D5	0 D4	1 D3	0 D2	0 D1	0 D0	Set Display Data Length	This command is valid only at 3-wire SPI (PS0=PS1=L) The next command specifies the number of bytes of display data to be written after this composite command. D(7:0)=00: 1 byte of display data is to be sent D(7:0)=FF: 256 bytes of display data is to be sent
E9~EF									Reserved	Reserved
F0~FF	1	1	1	1	X	X	X	X	Extended Features	Test mode commands and Extended features, see Extended Command Table.

Extended Command Table

Bit Pattern	Command	Description
11110000 000000X_1X_0	X_1X_0 : Set VL6 noise reduction	X_1X_0 = 00: Enable (POR) X_1X_0 = 11: Normal Remarks: This command is only valid for the IC version with G prefix notation on the "DTE" (datecode) field of label printed on die tray cover, intermediates and outer boxes.
11110001 00001$X_2X_1X_0$	$X_2X_1X_0$: Set TC Value	$X_2X_1X_0$ = 000: -0.05%/°C (POR) $X_2X_1X_0$ = 001: -0.07%/°C
11110111 0000000X_0	Select Oscillator Source	X_0 = 0: Internal RC oscillator is selected (POR) X_0 = 1: External oscillator from CL pin is selected
11110010 00000$X_2X_1X_0$	Oscillator Adjustment	$X_2X_1X_0$ = 000: -9% $X_2X_1X_0$ = 001: -6% $X_2X_1X_0$ = 010: -3% $X_2X_1X_0$ = 011: 0 (POR) $X_2X_1X_0$ = 100: +3%

		$X_2X_1X_0$ = 101: +6% $X_2X_1X_0$ = 110: +9% $X_2X_1X_0$ = 111: +12%
11111101 xxxx0$X_2$10	Lock / Unlock Interface	X_2 = 0 : Unlock the IC. The driver accepts any command and data written. X_2 = 1 : Lock the IC. The driver ignores all command and data written, except the unlock command or pin reset.
11110110 000$X_4X_3X_2X_1X_0$	Frame Frequency Adjust (Please find the default setting in the following table)	**FRAMEFQ** $X_2X_1X_0$ = 000: 0 $X_2X_1X_0$ = 001: 1 $X_2X_1X_0$ = 010: 2 $X_2X_1X_0$ = 011: 3 $X_2X_1X_0$ = 100: 4 $X_2X_1X_0$ = 101: 5 $X_2X_1X_0$ = 110: 6 $X_2X_1X_0$ = 111: 7 **Fosc** X_4X_3 = 00: 59kHz X_4X_3 = 01: 75kHz X_4X_3 = 10: 94kHz X_4X_3 = 11: 113kHz
Other than the above	Set Test Mode	Reserved

Frame Frequency Default Setting

Frame Frequency = Fosc / [Mux x (FRAMEFQ + 1) x PWM]

Mux (Icon Enable)	FRAMEFQ	PWM	Fosc
Mux<=17	2	15	59kHz
	5	12	94kHz
	4	9	59kHz
18<=MUX<=33	1	15	75kHz
	1	12	59kHz
	2	9	75kHz
34<=MUX<=49	0	15	59kHz
	1	12	94kHz
	1	9	75kHz
50<=MUX<=65	0	15	75kHz
	0	12	59kHz
	1	9	94kHz
66<=MUX<=81	0	15	94kHz
	0	12	75kHz
	0	9	59kHz

PWM is defined in command Set PWM and FRC.

Read Status Byte

A 8 bits status byte will be placed onto the data bus when a read operation is performed if D/$\overline{C}$ is low. The status byte is defined as following:

D7	D6	D5	D4	D3	D2	D1	D0	Comment
BUSY	ON	$\overline{RES}$	0	1	0	DS1	DS0	BUSY=0 : Chip is idle BUSY=1 : Chip is executing instruction ON=0 : Display is OFF ON=1 : Display is ON $\overline{RES}$ =0: Chip is idle $\overline{RES}$ =1: Chip is executing reset DS1, DS0 = 00: SSD1850 DS1, DS0 = 01: SSD1851

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read. Also, a dummy read is required before the first data is read. See P.14, Figure 4 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{W}$($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write. After the data read/write operation (address=127) is executed, the address will be reset to 0 in next data read/write operation.

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$($\overline{WR}$)	Action	Auto Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

Address Increment is done automatically after data read/write. The column address pointer of GDDRAM is affected. After the data read/write operation (address=127) is executed, the address will be reset to 0 in next data read/write operation.

Commands Required for R/$\overline{W}$ ($\overline{WR}$) Actions on RAM

R/$\overline{W}$ ($\overline{WR}$) Actions on RAMs	**Commands Required**	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	(1011$X_3X_2X_1X_0$)* (0001$X_3X_2X_1X_0$)* (0000$X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$)

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed or not.

COMMAND DESCRIPTIONS

Set Display On/Off
This command turns the display on/off, by the value of the LSB.

Set Display Start Line
This command is to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63/79. With value equals to 0, D0 of Page 0 is mapped to COM0. With value equals to 1, D1 of Page0 is mapped to COM0. The display start line values of 0 to 63/79 are assigned to Page 0 to 9.

Set Page Address
This command positions the page address to 0 to 8/10 possible positions in GDDRAM. Refer to figure 5. Set Higher Column Address This command specifies the higher nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Lower Column Address
This command specifies the lower nibble of the 7-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU and returning to 0 once overflow (>127).

Set Segment Re-map
This commands changes the mapping between the display data column address and segment driver. It allows flexibility in layout during LCD module assembly. Refer to figure 5.

Set Normal/Inverse Display
This command sets the display to be either normal/inverse. In normal display, a RAM data of 1 indicates an “ON” pixel. While in reverse display, a RAM data of 0 indicates an “ON” pixel. The icon line is not affected by this command.

Set Entire Display On/Off
This command forces the entire display, including the icon row, to be “ON” regardless of the contents of the display data RAM. This command has priority over normal/inverse display.
To execute this command, Set Display On command must be sent in advance.

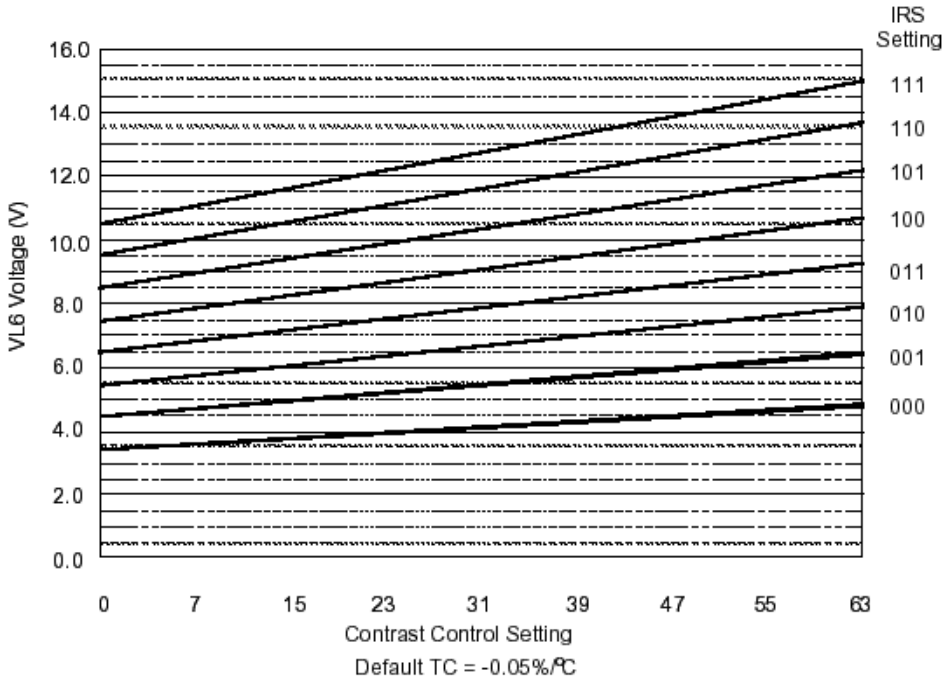
Set LCD Bias
This command is used to select a suitable bias ratio (1/4 to 1/11) required for driving the particular LCD panel in use. The POR default for SSD1851 is set to 1/10 bias and SSD1850 is set to 1/9.

Software Reset
This command causes some of the internal status of the chip to be initialized:
1. Page address is set to 0
2. Column address is set to 0
3. Initial Display Line is set to 0 (point to display RAM page 0, D0)
4. Internal Resistor Ratio register is set to (0,0,0)
5. Software Contrast is set to 32

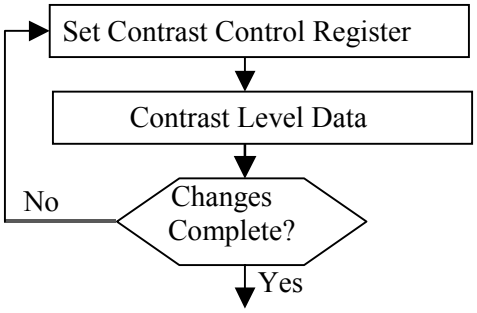
Set COM Output Scan Direction
This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly.

Set Power Control Register
This command turns on/off the various power circuits associated with the chip.

Set Internal Regulator Resistors Ratio
This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network (INTRS pin pulled high).
The Contrast Control Voltage Range curves is given in the figure below:



Set Contrast Control Register
This command adjusts the contrast of the LCD panel by changing VL6 of the LCD drive voltage provided by the On-Chip power circuits. VL6 is set with 64 steps (6-bit) contrast control register. It is a compound commands:



Set Display Offset
The next command specifies the mapping of display start line (COM0 if display start line register equals to 0) to one of ROW0-79. This command has no effect on ICONS. COM0 is mapped to ROW0 after reset.

Set Multiplex Ratio
This command switches default 80 multiplex mode to any multiplex from 16 to 80, if Icon is disabled (POR). When Icon is set enable, the corresponding multiplex ratio setting will be mapped to 17 to 81. The chip pads ROW0-ROW79 will be switched to corresponding COM signal output.

Set Power Save Mode
This command forces the chip to enter Standby or Sleep Mode. LSB of the command will define which mode will be entered.

Exit Power Save Mode
This command releases the chip from either Standby or Sleep Mode and return to normal operation.

Set N-line Inversion
Number of line inversion is set by this command for reducing crosstalk. 3 to 33-line inversion operations could be selected. At POR, this operation is disabled.
It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (N). Or else, some lines will not be changed their polarity during frame change.

Exit N-line Inversion
This command releases the chip from N-line inversion mode. The driving waveform will be inverted once per frame after issuing this command.

Set DC-DC Converter Factor
Internal DC-DC converter factor is set by this command. For SSD1850, 2X to 5X multiplying factors could be selected. 2X/3X, 4X, 5X and 6X factors are selected using this command. Hardware configuration is used for 2X or 3X setup. For SSD1851, 2X to 6X multiplying factors could be selected.

Set Icon Enable
This command enable/disable the Icon display.

Start Internal Oscillator
After POR, the internal oscillator is OFF. It should be turned ON by sending this command to the chip.

Set Display Data Length
This two-byte command only valid when 3-wire SPI configuration is set by H/W input (PS0=PS1=L). The second 8-bit is used to indicate that a specified number display data byte (1-256) are to be transmitted. Next byte after the display data string is handled as a command.

Set Gray Scale Mode (White/Light Gray/Dark Gray/Black)
Command 88(hex) to 8F(hex) are used to specify the four gray levels' pulse width at the four possible frames. The four gray levels are called white, light gray, dark gray and black. Each level is defined by 4 registers for 4 consecutive frames. For example, WA is a 4-bit register to define the pulse width of the 1st frame in White mode. WB is a register for 2nd frame in White mode etc. Each command specifies two registers.

For 4 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th
0	0	White	WA	WB	WC	WD
0	1	Light Gray	LA	LB	LC	LD
1	0	Dark Gray	DA	DB	DC	DD
1	1	Black	BA	BB	BC	BD

For 3 FRC,

Memory Content		Gray Mode	FRAME			
1st Byte	2nd Byte		1st	2nd	3rd	4th (No use)
0	0	White	WA	WB	WC	WD (XX)
0	1	Light Gray	LA	LB	LC	LD (XX)
1	0	Dark Gray	DA	DB	DC	DC (XX)
1	1	Black	BA	BB	BC	BC (XX)

Set PWM and FRC
This command selects the number of frames in frame rate control, or the number of levels in the pulse width modulation.

Set Test Mode
This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Status Register Read
This command is issued by setting D/$\overline{C}$ Low during a data read (refer to figure 1 and 2 parallel interface waveform, P.35-38). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

EXTENDED COMMANDS
These commands are used, in addition to basic commands, to trigger the enhanced features designed for the chip. These features are on top of general ones.

Set VL6 noise reduction
This command is to enable the VL6 noise reduction. This command is only valid for the IC version with G prefix notation on the “DTE” (datecode) field of label printed on die tray cover, intermediates and outer boxes. For details, please refer to the product change notification document of PC0010 from SSL.

Set Temperature Coefficient (TC) Value
This command is to set 1 out of 2 different temperature coefficients in order to match various liquid crystal temperature grades.

Select Oscillator Source
This command enables the external clock input from CL pin.

Oscillator adjustment
This command is used to adjust the oscillator frequency to desired frame frequency.

Lock/Unlock Interface
After sending the lock command, the interface will be disabled until the unlock command is received. The lock command is suggested whenever the LCD driver will not be accessed for some period. This can minimize incorrect data or command written due to noisy interface.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 4.0	V
V_{CC}		VSS-0.3 to VSS+18.0	V
V_{CI}	Booster Supply Voltage	VDD to 4.0	V
V_{in}	Input Voltage	VSS-0.3 to VDD+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +80	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range V_{SS} < or = (Vin or V_{OUT}) < or = V_{DD}. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, V_{DD}=1.8 to 3.3V, T_A=-40 to 85°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ (at 25°C)	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range Voltage Generator Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	1.8	2.7	3.3	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 4X Converter Enabled, Write accessing, Tcyc = 3.3MHz, Osc. Freq.=31kHz, Display On.	-	750	800	µA
I_{DP1}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{CC} = 10.8V, Voltage Generator Off, Divider Enabled, Read/Write Halt, Osc. Freq.=31kHz, Display On, V_{L6}=9V	-	40	60	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Vcc=10.8V, Voltage Generator On, 4x DC-DC Converter Enabled Divider Enabled, Read/Write Halt, Osc. Freq.=31kHz, Display On, V_{L6} = 9V.	-	200	500	µA
I_{SB}	Standby Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Osc. Freq. 31KHz, Read/Write halt.	-	27	40	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, Read/Write halt.	-	0.5	2.5	µA
V_{CC}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Osc. Freq. = 31kHz, Regulator Enabled, Divider Enabled.	VDD	-	15.0	V
	DC-DC Converter Efficiency	I_{CC} < 20uA	95	99		%
V_{LCD}	LCD Driving Voltage Input (V_{CC}Pin)	Voltage Generator Disabled.	4.0	-	15.0	V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{REF}	External Reference Voltage Input	Internal Reference Voltage Source Disable (REF pin pulled Low), External Reference voltage input to V_{EXT} pin.	2.04	2.10	2.16	V
	Internal Reference Voltage	Internal Reference Voltage Source Enabled (REF pin pulled High), V_{EXT} pin NC.		2.10		V
V_{OH1}	Output High voltage (D_0-D_7)	Iout = +500μA	0.8*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D_0-D_7)	Iout = -500μA	0.0	-	0.2*V_{DD}	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Enabled (VL6 voltage depends on Int/Ext Contrast Control)	V_{DD}	-	V_{CC}-0.5	V
V_{L6}	LCD Driving Voltage Source (V_{L6} Pin)	Regulator Disable	-	Floating	-	V
V_{IH1}	Input high voltage (RES#, PS0, PS1, CS, D/C#, R/W#, D_0-D_7, REF, INTRS)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage (RES#, PS0, PS1, CS, D/C#, R/W#, D_0-D_7, REF, INTRS)		0.0	-	0.2*V_{DD}	V
V_{L6}	LCD Display Voltage Output	Divider Enabled, 1:a bias ratio,	-	V_{L6}	-	V
V_{L5}	(V_{L6}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	a=4~10 for SSD1851 and a =4~9 for	-	(a-1)/a*V_{L6}	-	V
V_{L4}		SSD1850.	-	(a-2)/a*V_{L6}	-	V
V_{L3}			-	2/a*V_{L6}	-	V
V_{L2}			-	1/a*V_{L6}	-	V
V_{L6}	LCD Display Voltage Input	Voltage reference to V_{SS}, External	V_{L5}	-	V_{CC}	V
V_{L5}	(V_{L6}, V_{L5}, V_{L4}, V_{L3}, V_{L2} Pins)	Voltage Generator, Divider Disabled	V_{L4}	-	V_{L6}	V
V_{L4}			V_{L3}	-	V_{L5}	V
V_{L3}			V_{L2}	-	V_{L4}	V
V_{L2}			V_{SS}	-	V_{L3}	V
I_{OH}	Output High Current Source(D_0-D_7)	Vout=V_{DD}-0.4V	50	-	-	μA
I_{OL}	Output Low Current Drain (D_0-D_7)	Vout=0.4V	-	-	-50	μA
I_{OZ}	Output Tri-state Current Drain Source (D_0-D_7)		-1	-	1	μA
I_{IL}/I_{IH}	Input Current (RES#, PS0, PS1,CS#, E(RD#), D/C#,R/W#(WR#), D_0~D_7, REF, INTRS)		-1		1	μA
C_{IN}	Input Capacitance (all logic pins)			5	7.5	pF
ΔV_{L6}	Variation of VL6 Output (1.8V < V_{DD} < 3.3V)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-	± 2	-	%
	Temperature Coefficient Compensation					
PTC0	Temperature Coefficient [POR]	Voltage Regulator Enabled	-0.04	-0.05	-0.06	%
PTC1	Temperature Coefficient	Voltage Regulator Enabled	-0.06	-0.07	-0.08	%

*The formula for the temperature coefficient is:

$$TC(\%/^0C) = \frac{V_{ref}\,at\,50^0C - V_{ref}\,at\,0^0C}{50^0C - 0^0C} * \frac{1}{V_{ref}\,at\,25^0C} * 100\%$$

AC ELECTRICAL CHARACTERISTICS

(T_A=-40 to 85°C, Voltages referenced to V_{SS}, V_{DD}=V_{CI}=2.7V, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ (at 25°C)	Max	Unit
F_{FRM}	Frame Frequency (SSD1851) Fosc / [Mux x (FRAMEFQ+1) x PWM]	Display ON, Set 128 x 81 Graphic Display Mode, Icon Line Enabled, 15PWM, Default frame frequency setting	70	77.4	100	Hz
F_{FRM}	Frame Frequency (SSD1850) Fosc / [Mux x (FRAMEFQ+1) x PWM]	Display ON, Set 128 x 65 Graphic Display Mode, Icon Line Enabled, 15PWM, Default frame frequency setting	70	76.9	100	Hz

TABLE 3a. Parallel Timing Characteristics (TA=-40 to 85°C, VDD=2.7V, VSS=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	2	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	30	ns
t_{OH}	Output Disable Time	-	-	80	ns
t_{ACC}	Access Time	-	-	25	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read command) Chip Select Low Pulse Width (write)	95 40 15	- -	- -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	30 30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

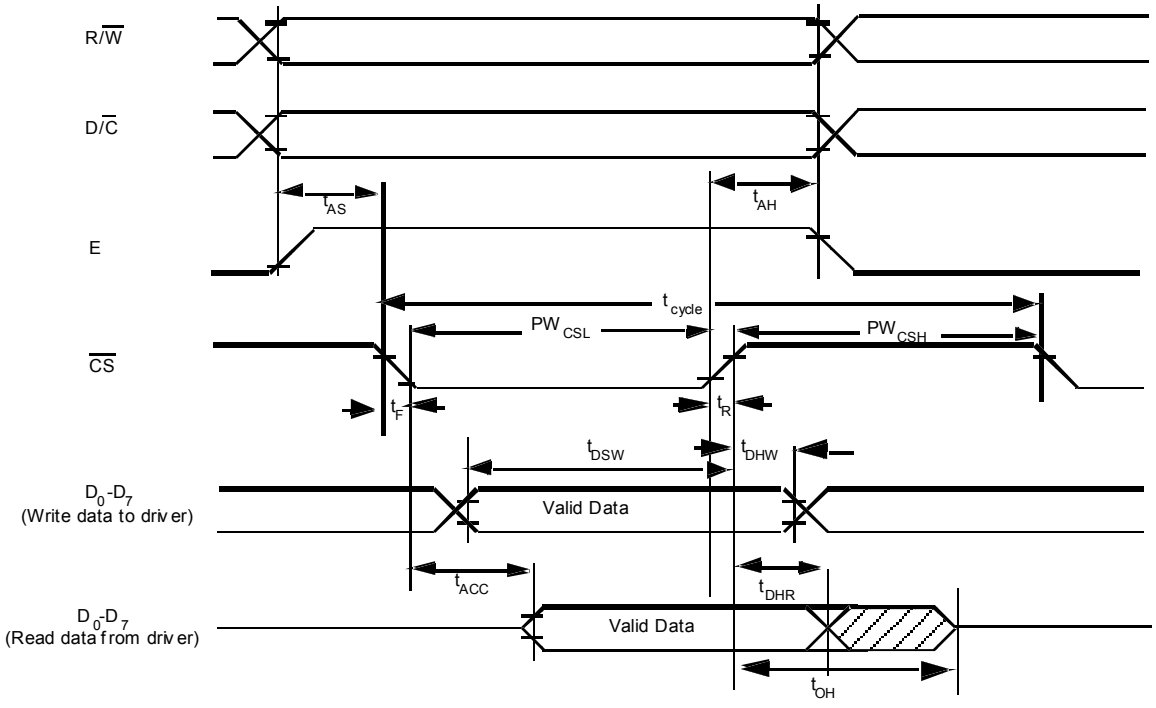


Figure 1a. Parallel 6800-series Interface Timing Characteristics (PS0=H, PS1=H)

TABLE 3b. Parallel Timing Characteristics (TA=-40 to 85°C, VDD=1.8V,VSS=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	15	-	-	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	- -	- -	100 35	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read command) Chip Select Low Pulse Width (write)	120 55 20	- -	- -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	40 40	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

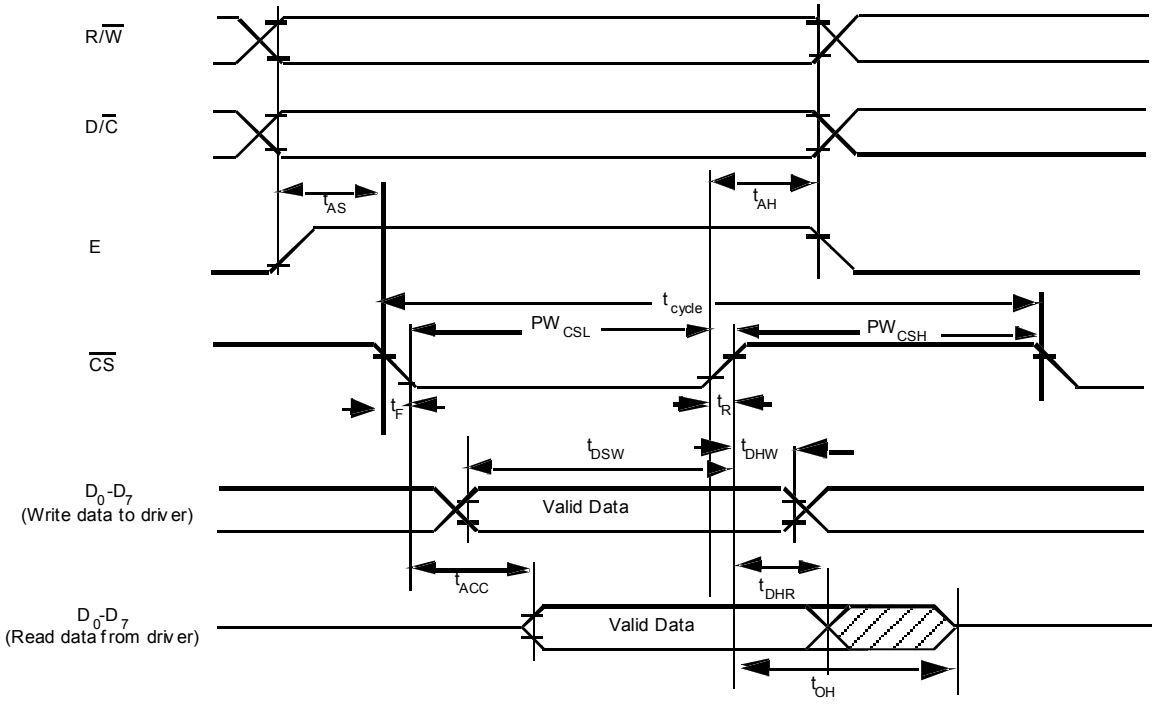


Figure 1b. Parallel 6800-series Interface Timing Characteristics (PS0=H, PS1=H)

TABLE 4a. Parallel Timing Characteristics (TA=-40 to 85°C, VDD=2.7V,VSS=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	2	-	-	ns
t_{DHR}	Read Data Hold Time	10	-	-	ns
t_{OH}	Output Disable Time	-	-	30	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	- -	-	80 25	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read command) Chip Select Low Pulse Width (write)	95 40 15	- -	- -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	30 30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

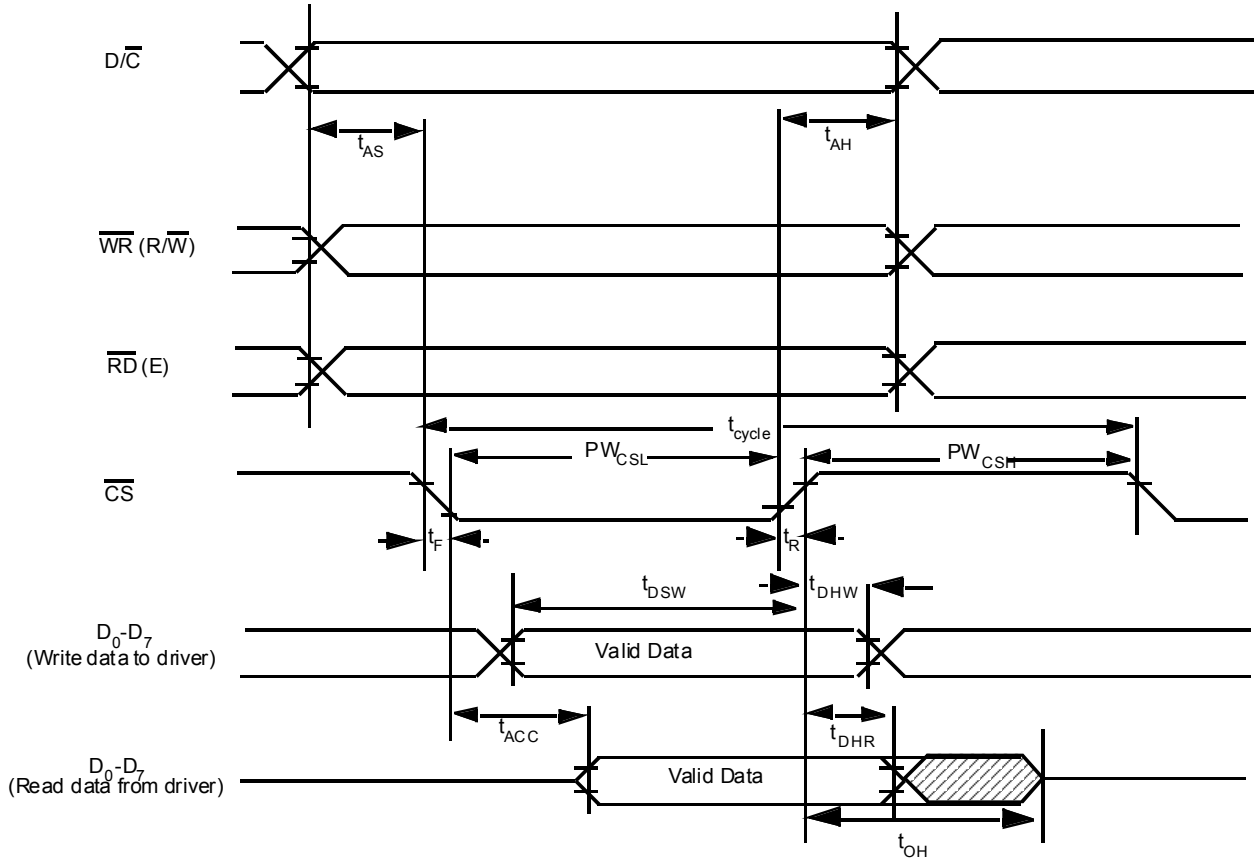


Figure 2a. Parallel 8080-series Interface Timing Characteristics (PS0=H, PS1=L)

TABLE 4b. Parallel Timing Characteristics (TA=-40 to 85°C, VDD=1.8V,VSS=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	5	-	-	ns
t_{DHR}	Read Data Hold Time	15	-	-	ns
t_{OH}	Output Disable Time	-	-	40	ns
t_{ACC}	Access Time (RAM) Access Time (Command)	- -	-	100 35	ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read command) Chip Select Low Pulse Width (write)	120 55 20	- - -	- - -	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	40 40	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

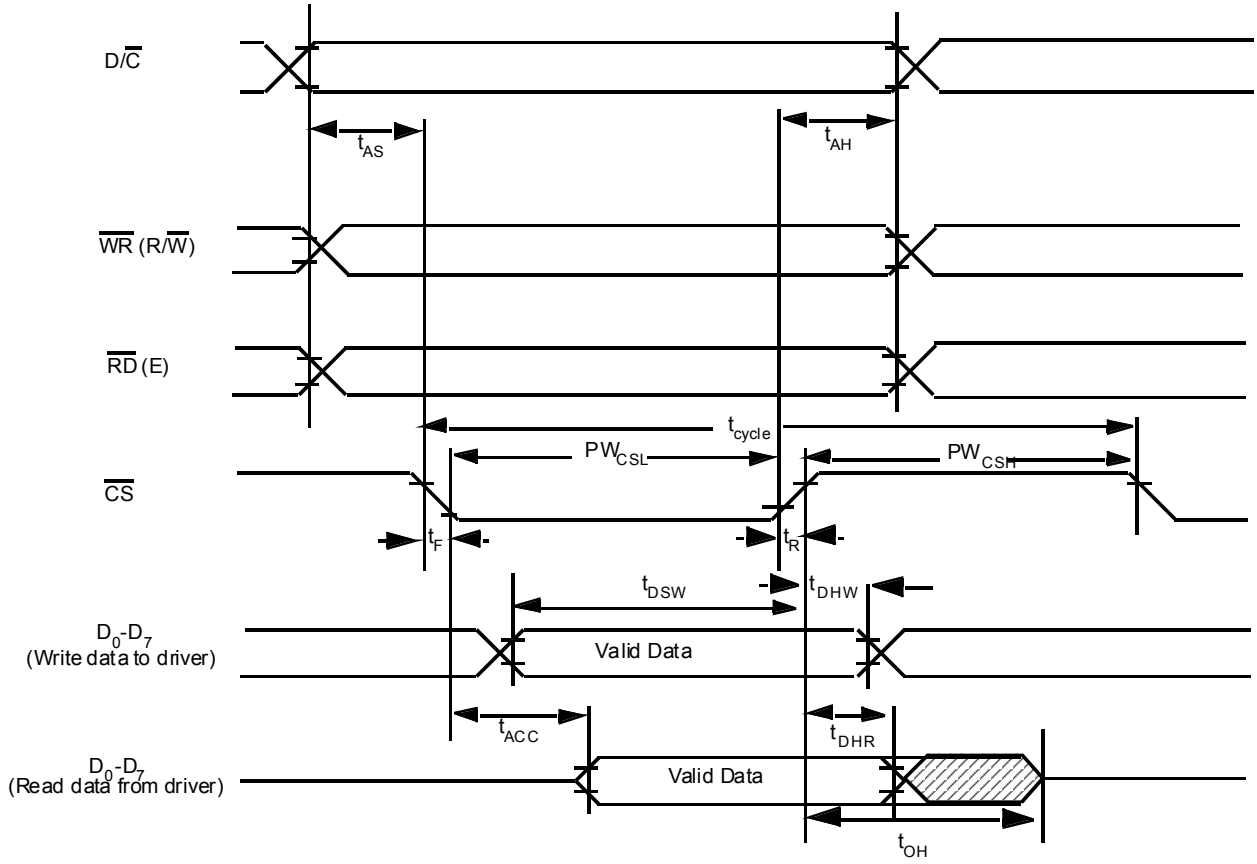


Figure 2b. Parallel 8080-series Interface Timing Characteristics (PS0=H, PS1=L)

TABLE 5a. Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.7V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	5	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	10	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

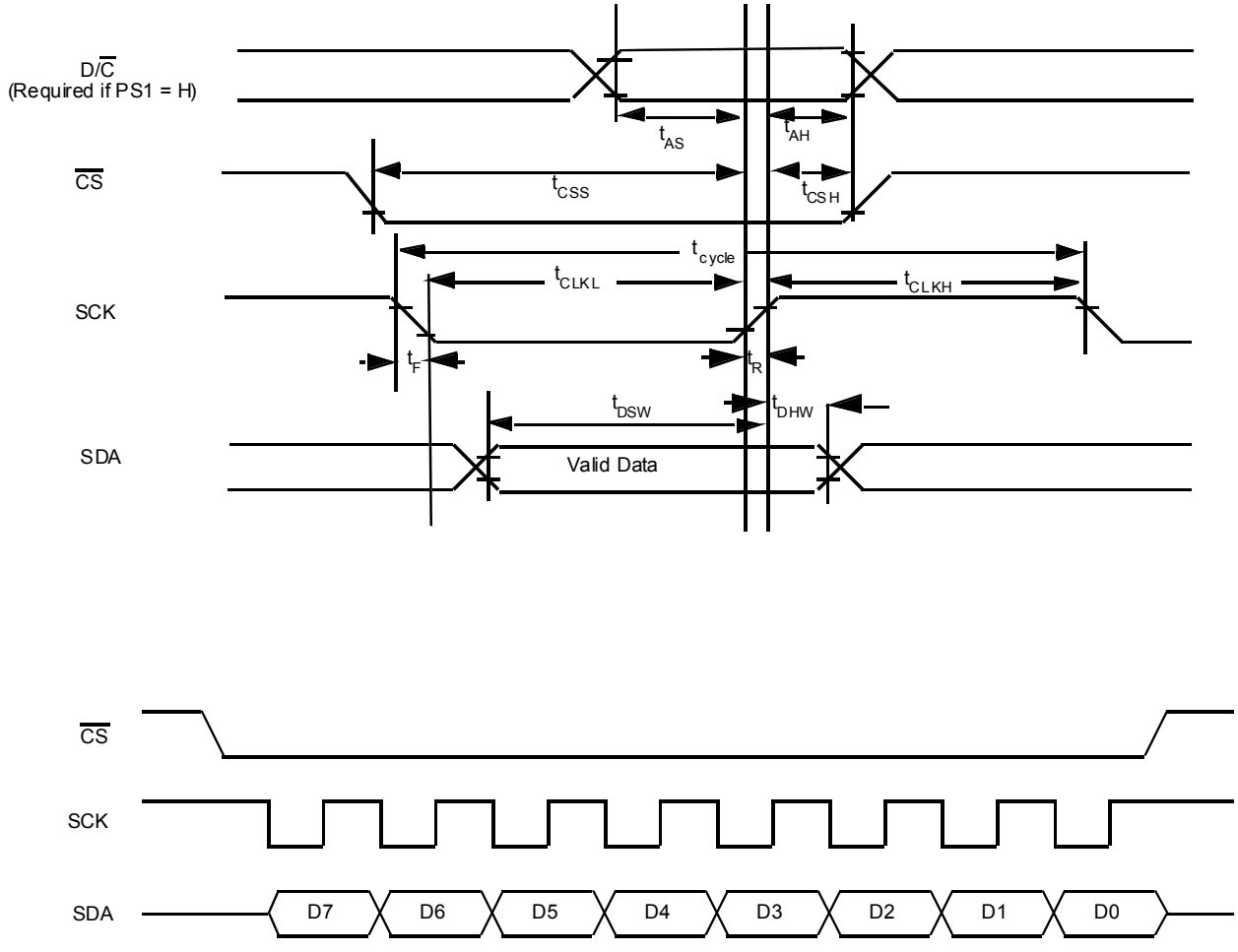


Figure 3a. Serial Timing Characteristics (PS0=L)

TABLE 5b. Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 1.8V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	70	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	15	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{OHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

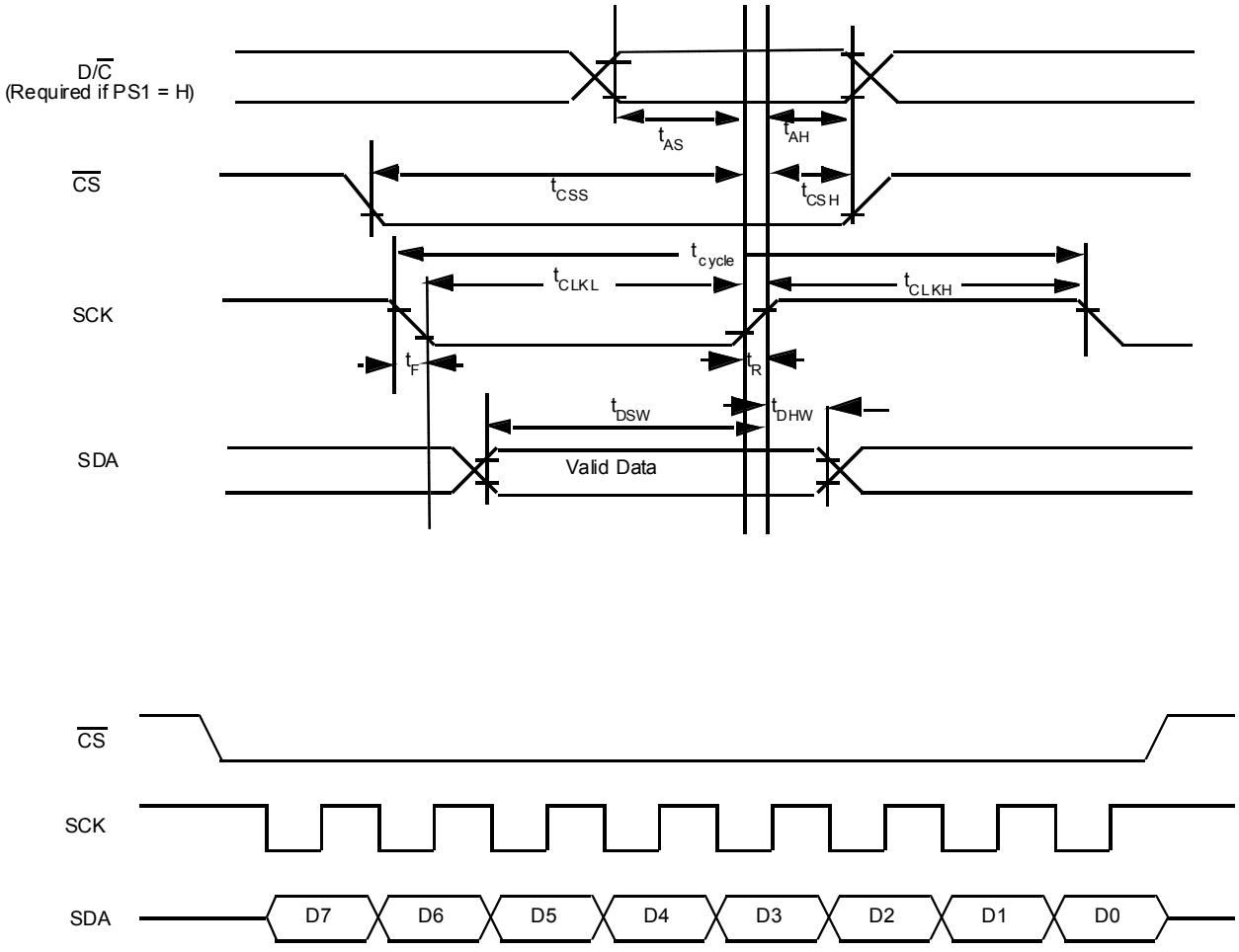
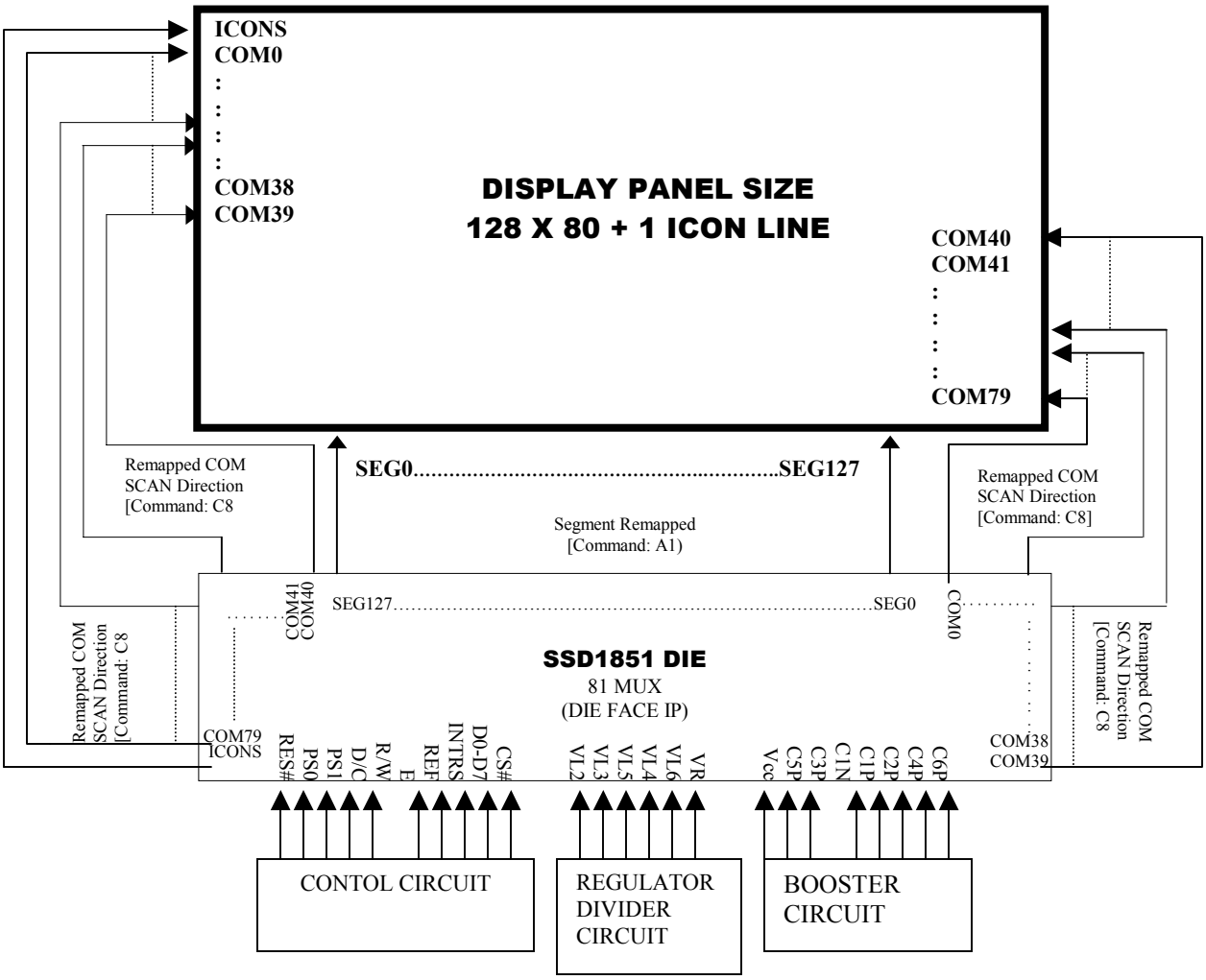


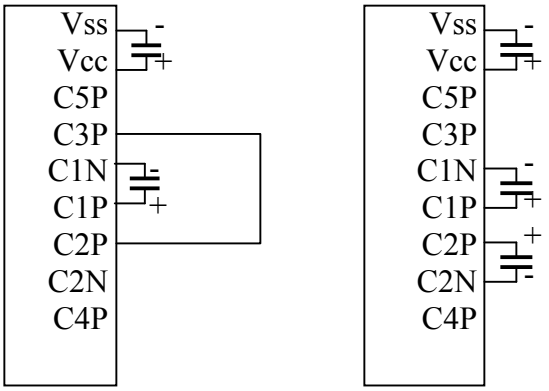
Figure 3b. Serial Timing Characteristics (PS0=L)

APPLICATION CIRCUIT



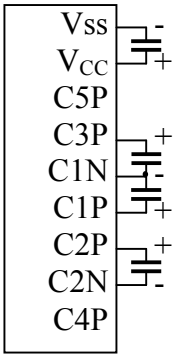
Application Circuit: DC-DC Converter Circuit Configuration

SSD1850/51 IC works from 2X to 6X DC-DC converter. For the capacitor connections, please refer to below circuit diagrams. Note that if the capacitor connection does not match with the software setting of DC-DC Converter Factor (0x64~0x67), abnormal current consumption will be observed.

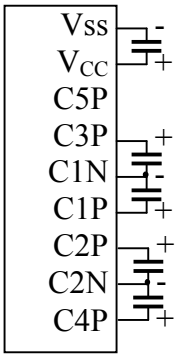


2X Converter

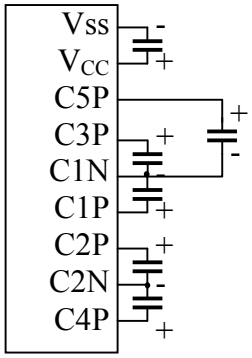
3X Converter



4X Converter



5X Converter

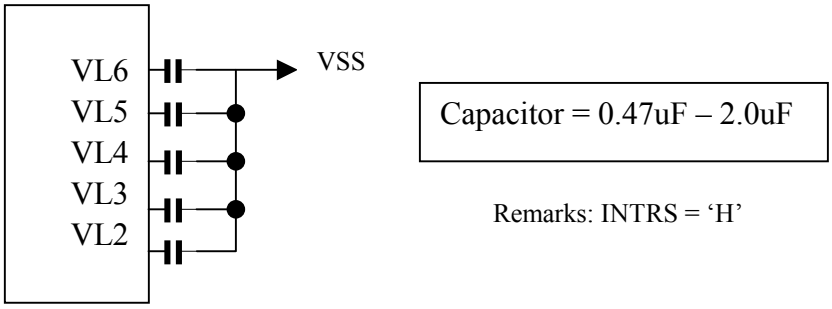


6X Converter

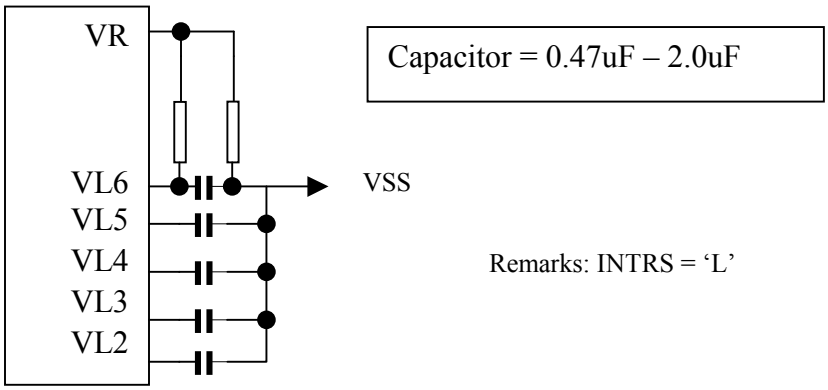
*Note: Capacitor value = 1.0uF to 4.7uF
*Note: SSD1850 works up to 5X only.

Application Circuit: Regulator Circuit and Bias Divider Circuit

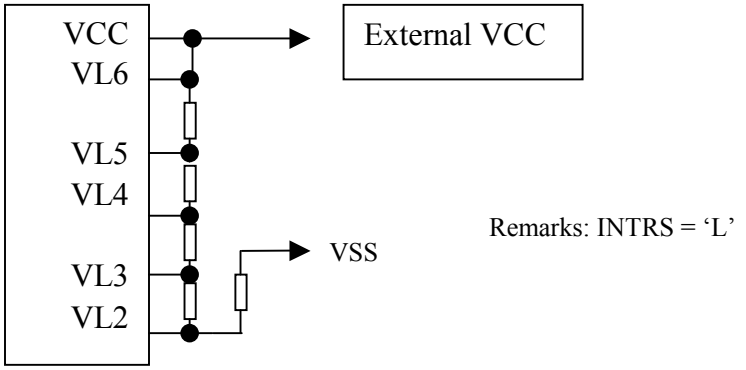
Internal Regulator and Bias Divider
[COMMAND: 2F]



External Regulator and Internal Bias Divider
[COMMAND: 2D]



External Regulator Bias Divider
[COMMAND: 28]



OTP Programming Circuit and Sequence

OTP (One Time Programming) is a method to adjust the VL6. In order to eliminate the variations of LCD module in term of contrast level, OTP can be used to achieve the best contrast of every LCD modules.

OTP setting and programming should include two major steps of (1) Find the OTP offset and (2) OTP programming as following,

Step 1. Find the OTP offset

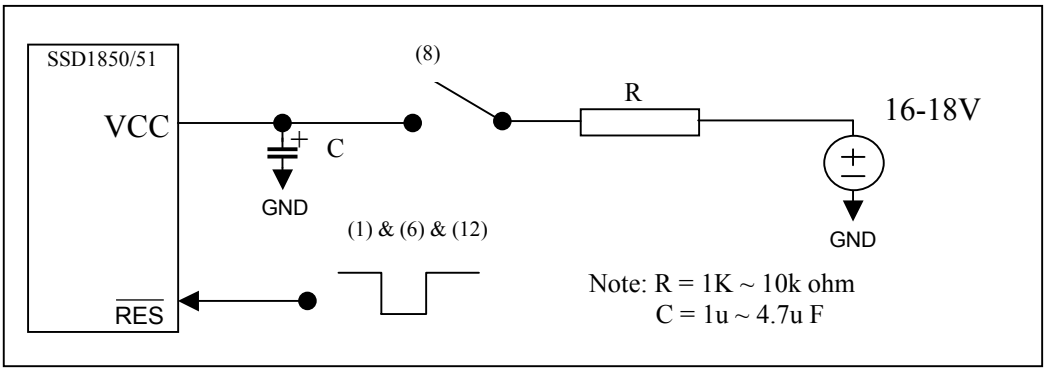
(1) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (0x81, 0x00~0x3F) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best visual contrast = 0x24
OTP setting steps = 0x24 - 0x20 = +4
OTP setting commands should be (0x82, 0xF4)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best visual contrast = 0x1B
OTP setting steps = 0x1B - 0x20 = -5
OTP setting commands should be (0x82, 0xFB)

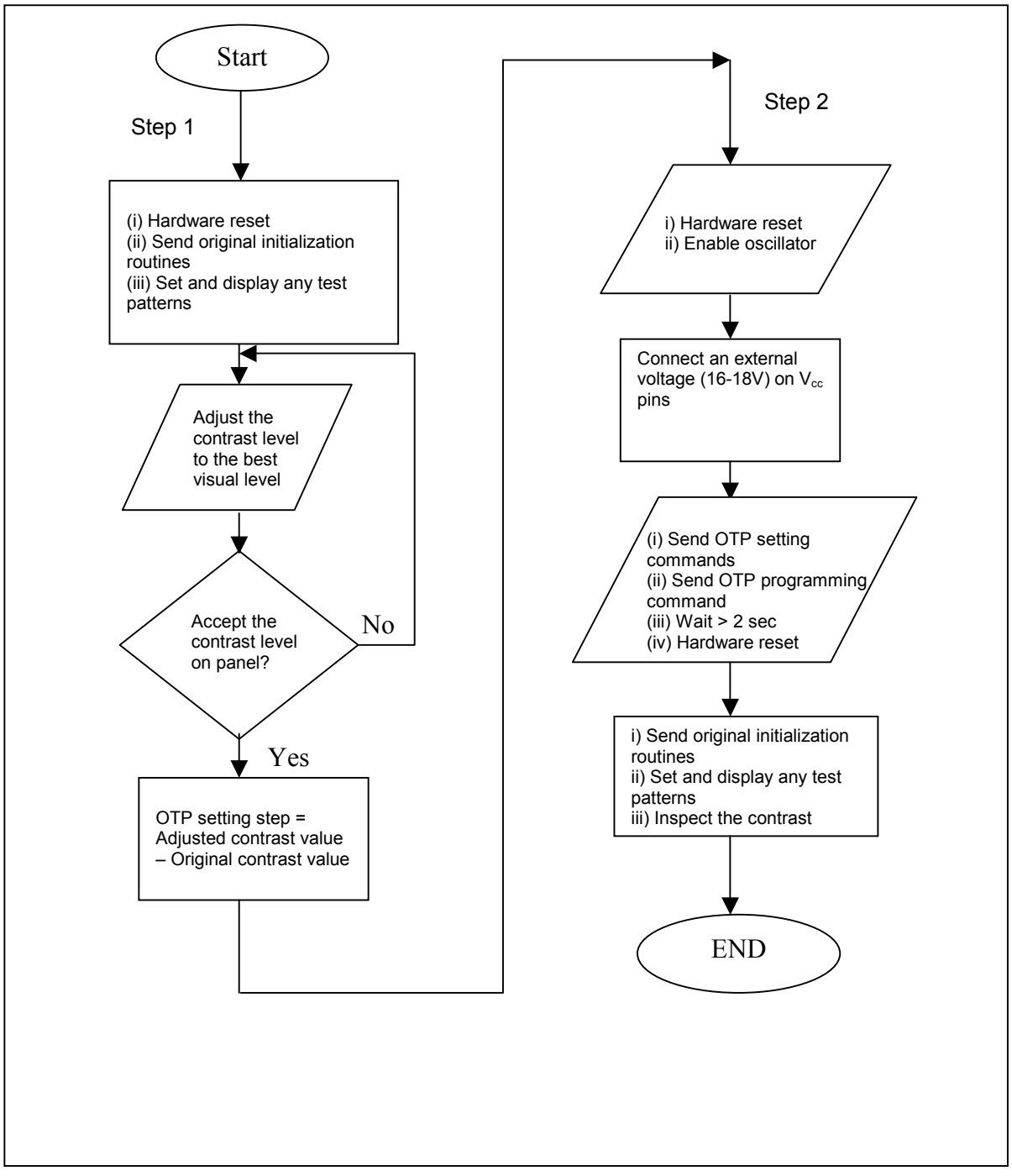
Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{RES}$ pin)
(7) Enable Oscillator (0xAB)
(8) Connect an external VCC (see diagram below)
(9) Send OTP setting commands that we find in step 1 (0x82, 0xF0~0xFF)
(10) Send OTP programming command (0x83)
(11) Wait at least 2 seconds
(12) Hardware Reset
Verify the result by repeating step 1. (2) – (3)



OTP Programming Circuit

Flow Chart of OTP Program



OTP Example program

Find the OTP offset:

1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
2. COMMAND(0XAB) \\Enable oscillator
   COMMAND(0X2F) \\ turn on the internal voltage booster, internal regulator and output op-amp buffer; Select booster level
3. COMMAND(0X48) \\ Set Duty ratio
   COMMAND(0X40) \\ 64Mux
   COMMAND(0X55) \\ Set Biasing ratio (1/9 BIAS)
4. COMMAND(0X81) \\ Set target gain and contrast.
   COMMAND(0X2D) \\ contrast = 45
   COMMAND(0X24) \\ gain = 5.1
5. \\ Set target display contents
   COMMAND(0XB0) \\ set page address
   COMMAND(0x00) \\ set lower nibble column address
   COMMAND(0X10) \\ set higher nibble column address
   DATA(…) \\ write target content to GDDRAM
   COMMAND(0XAF) \\ Set Display On
6. OTP offset calculation… target OTP offset value is +3

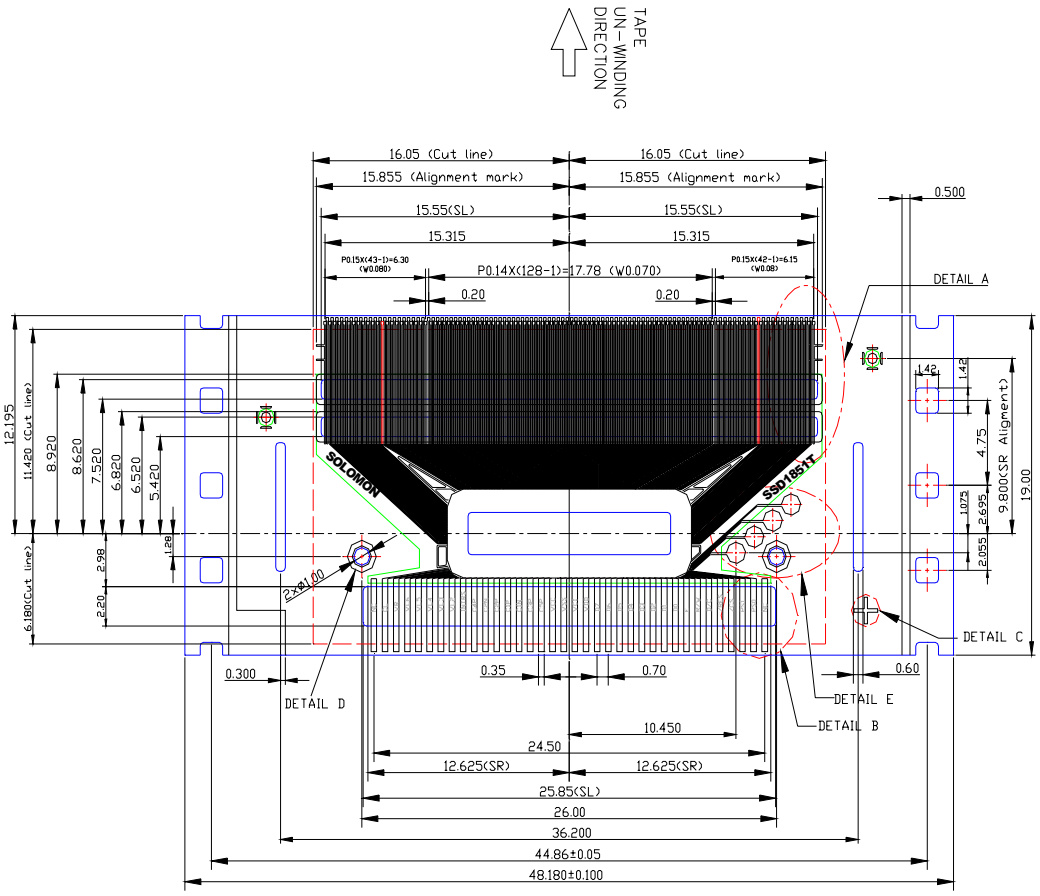
OTP programming:

7. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin
8. COMMAND(0XAB) \\ Enable Oscillator
9. Connect an external VCC (16V-18V)
10. COMMAND(0X82) \\ Set OTP offset value to +3 (0011)
    COMMAND(0XF3) \\ 0001 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value
11. COMMAND(0X83) \\ Send the OTP programming command
12. Wait at least 2 seconds for programming wait time
13. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

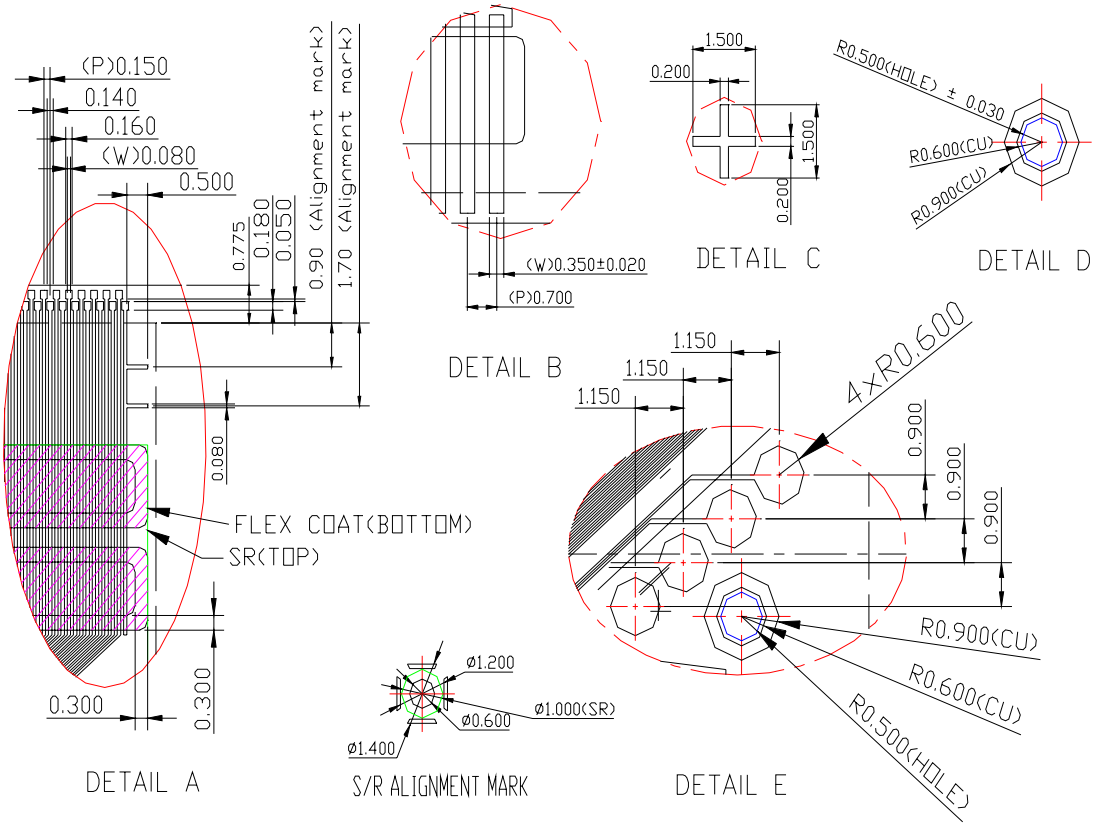
Verify the result:

14. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel

SSD1851T TAB PACKAGE DIMENSION (1 OF 3)
DO NOT SCALE THIS DRAWING



SSD1851T TAB PACKAGE DIMENSION (2 OF 3)
DO NOT SCALE THIS DRAWING



SSD1851T TAB PACKAGE DIMENSION (3 OF 3)

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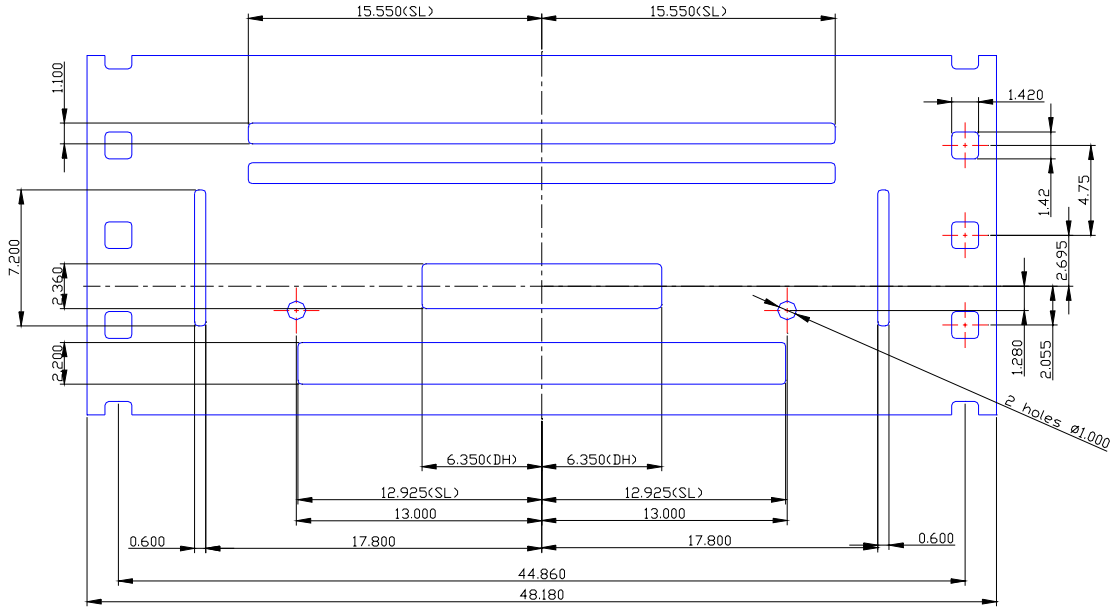

SSD1851U COF PACKAGE DIMENSION (1 OF 2)

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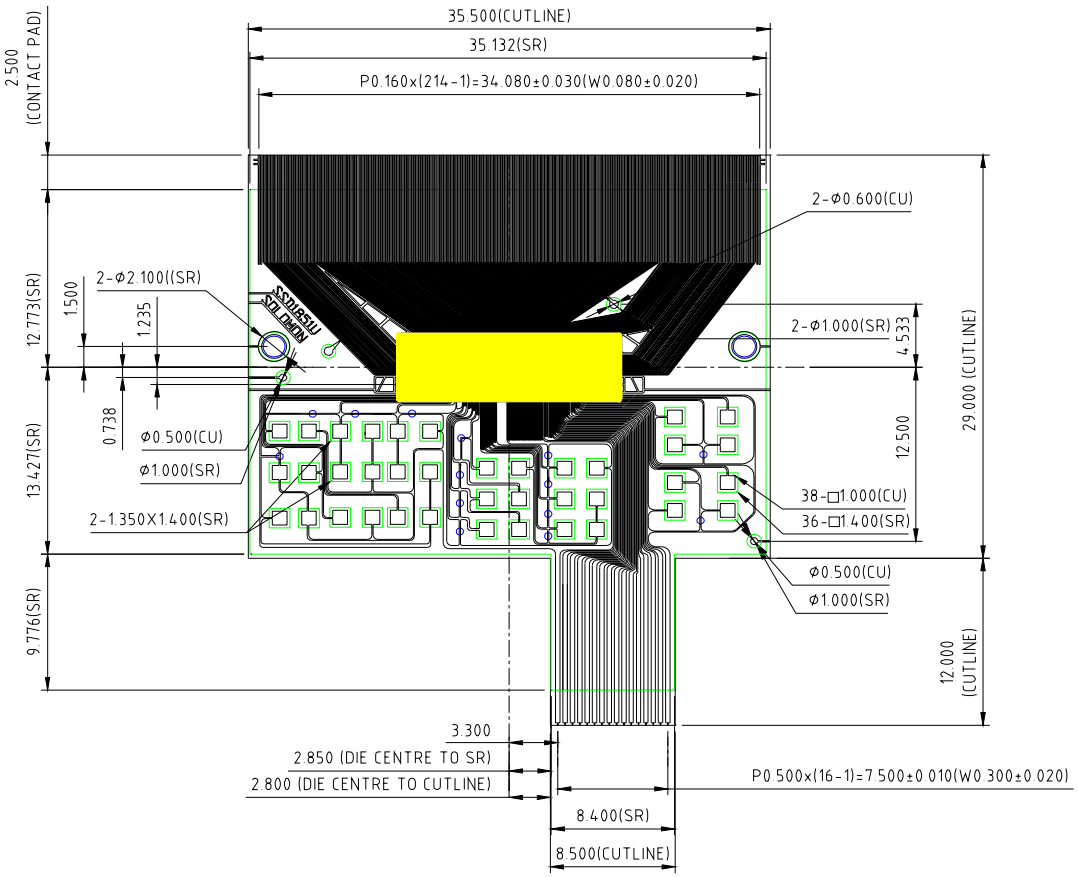
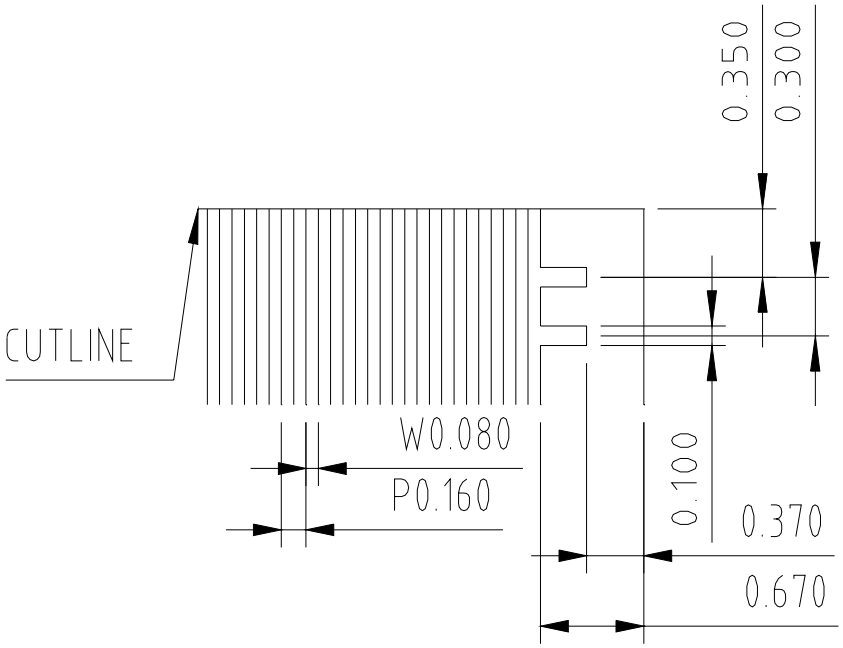


SSD1851U COF PACKAGE DIMENSION (2 OF 2)
DO NOT SCALE THIS DRAWING



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