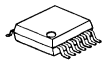
SYNCHRONOUS SEPARATOR WITH COUNT DOWN

■GENERAL DESCRIPTION

The NJW1303 is a synchronous separator performs Horizontal and Vertical synchronous signal from composit video signals. It contains count down circuit for H,V keeping high sync separation in the weak signal. It is suitable for car navigation and LCD TV.

■PACKAGE OUTLINE

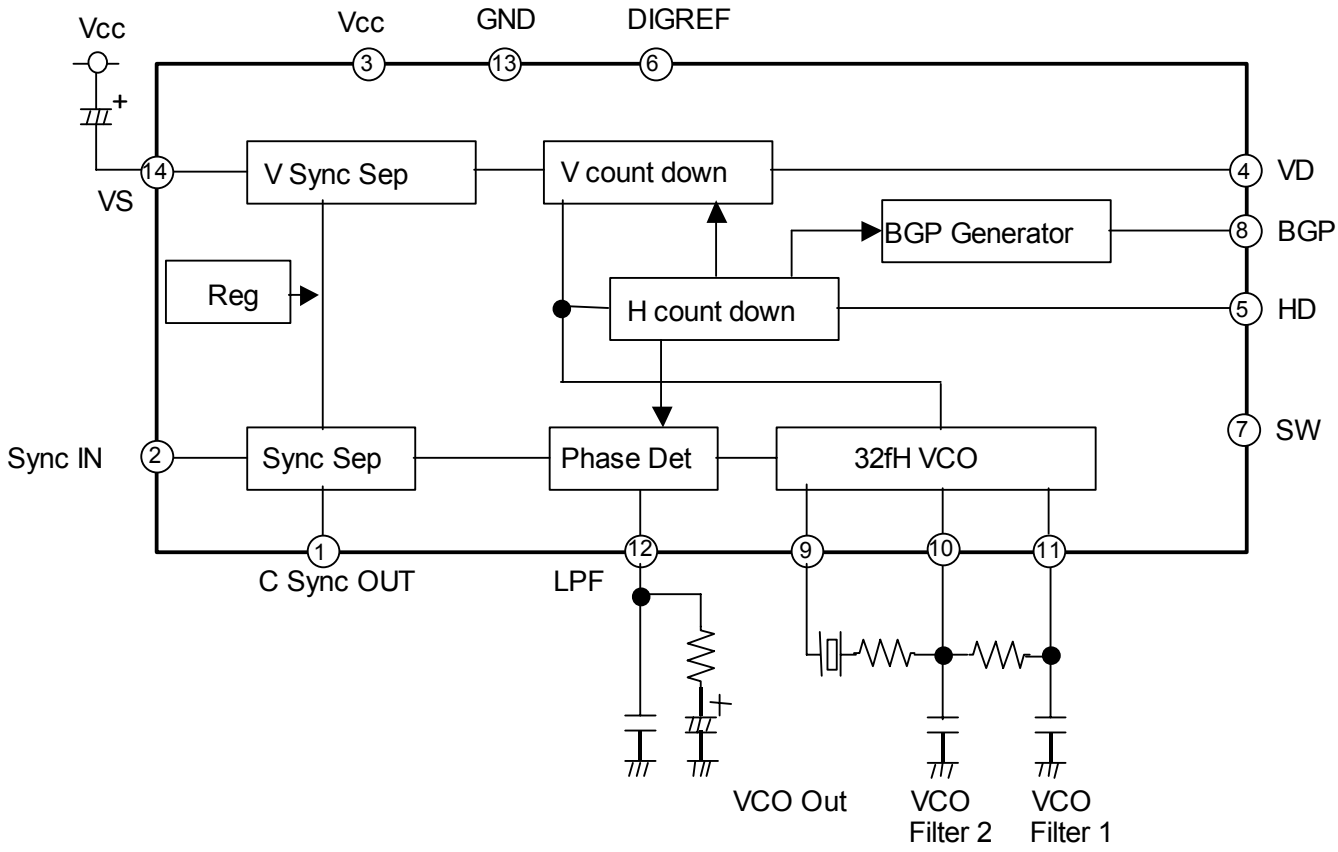


NJW1303V

■FEATURES

- ●Operating Voltage V^+ =2.7V to 5.3V
- ●Operating Current 5mA typ. at V^+ =5V
- ●Output for HD,VD,C sync
- ●unnecessary adjustment of oscillation frequency for internal count down circuit
- ●Internal BGP
- ●Bi-CMOS Technology
- ●Package Outline SSOP14

■PIN FUNCTION, BLOCK DIAGLAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	8.0	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature	Tstg	-40 to +125	°C

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	Vopr	2.7 to 5.3	V

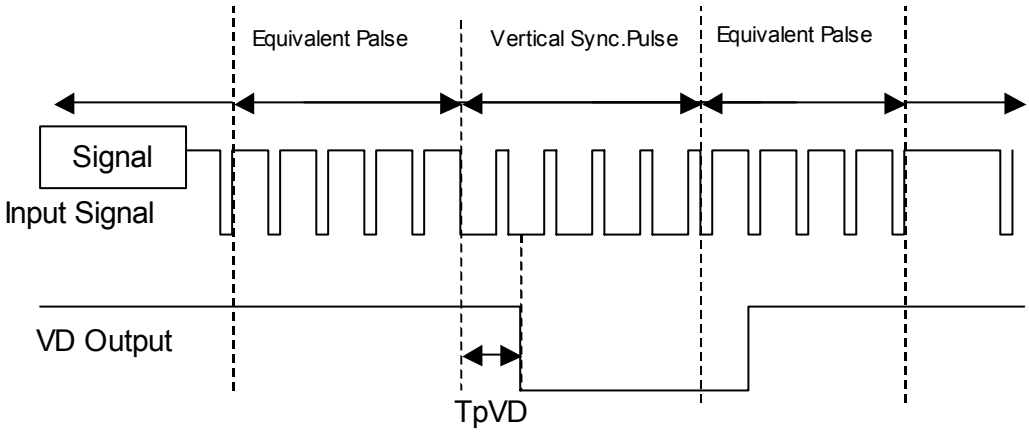
■ ELECTRICAL CHARACTERISTICS (V^+=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	No input signal	3.3	5.0	7.5	mA
AFC Free Run Frequency	f_{OH}	Measure the Input connect to GND under 300ohm	15.654	15.734	15.814	kHz
AFC Lock Range	$\Delta f_{HL}1$	Miss lock to high frequency	+600	+700	-	Hz
	$\Delta f_{HL}2$	Miss lock to Low frequency	-	-700	-600	
AFC Capture Range	$\Delta f_{HP}1$	Capture from high frequency	+600	+700	-	Hz
	$\Delta f_{HP}2$	Capture from Low frequency	-	-700	-600	
Horizontal Output Pulse Width	PwHD	**Input Signal** 4.8us 286mVpp	3.5	3.9	4.3	us
Horizontal Output Delay	TpDH	**Output Signal** TpDH	0.48	0.64	0.8	us
Horizontal Output Saturation Level	VoLH	PwHD VoLH 0V ***point1**	-0.2	0.1	0.3	V
Horizontal AFC Keep Limit Input	V_{IN}GM	Input is Color Bar of 1Vpp,and Horizontal signal of 4.8 uS pulth width. ATT less of miss lock Sync at valuable of input signal level.	-	-	-20	dB
BGP Pulse Width	PwGP	**Input Signal** 4.8us 286mVpp TpDG	3.1	3.6	4.1	us
BGP Delay	TpDG	**Output Signal** PwGP 0V ***point1**	0.35	0.6	0.85	us
BGP Limit Input	V_{MIN}BGP	Input is Color Bar of 1Vpp,and Horizontal signal of 4.8 uS pulth width. ATT less of changeable BGP output at less of input signal level.	-	-	-17	dB

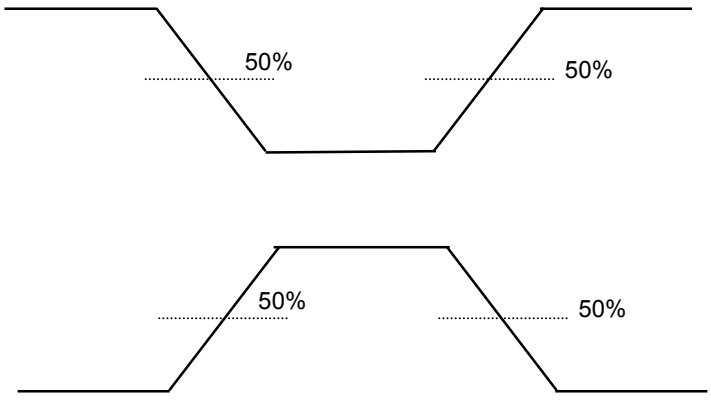
■ **ELECTRICAL CHARACTERISTICS** (V^+=5V, Ta=25°C)

PARAMETER	SYMBOLS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical Output Pulse Width	PwVD	*point	2.5	3.0	3.5	H
Vertical Output Delay	TpVD		0.47	0.66	0.85	H
Vertical Output Saturation Level	V_LVD	Low level of Vertical output	-	0.2	0.5	V
C.SYNC Output Delay	TpCS		0.32	0.5	0.64	us
C.SYNC Output Saturation Voltage	V_LCS		-	0.2	0.5	V

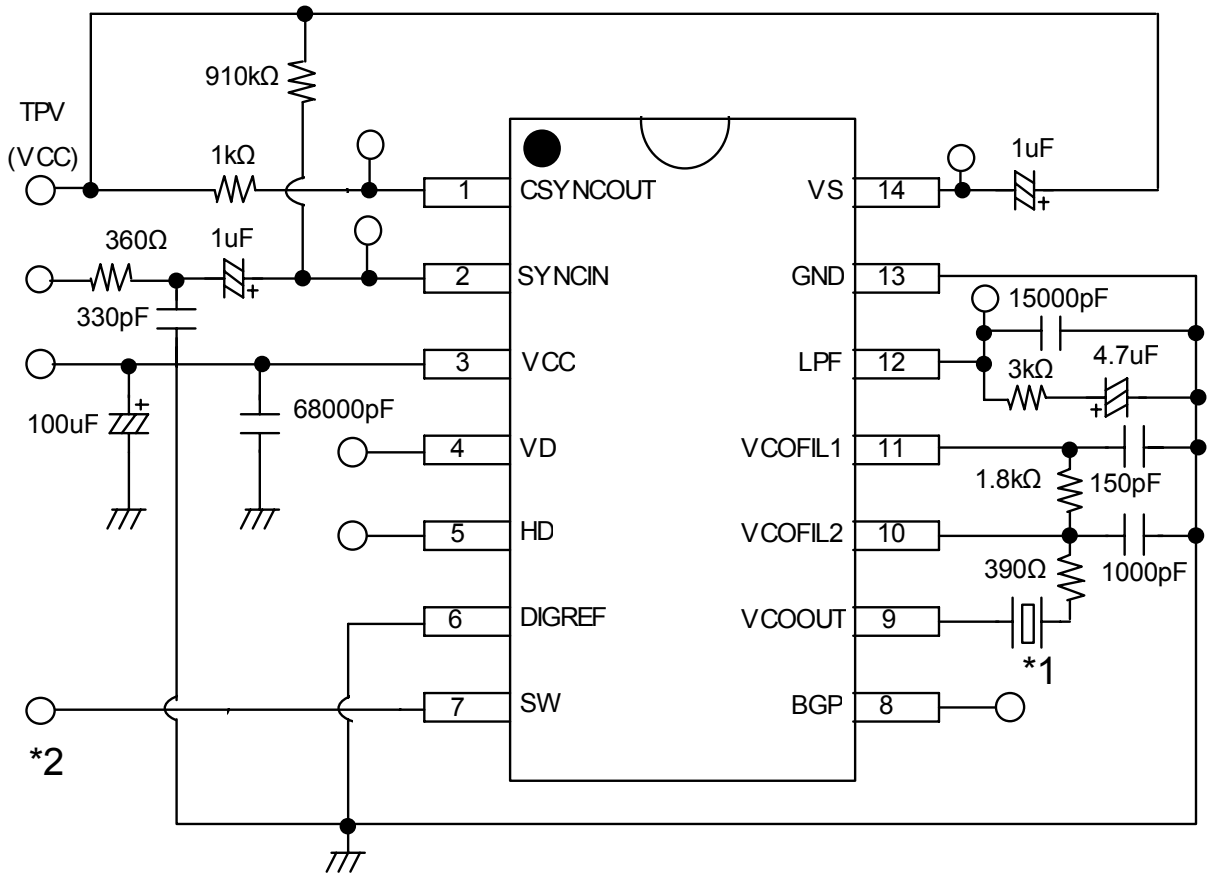
***point**



***When measure of pulse timing**



■TEST CIRCUIT



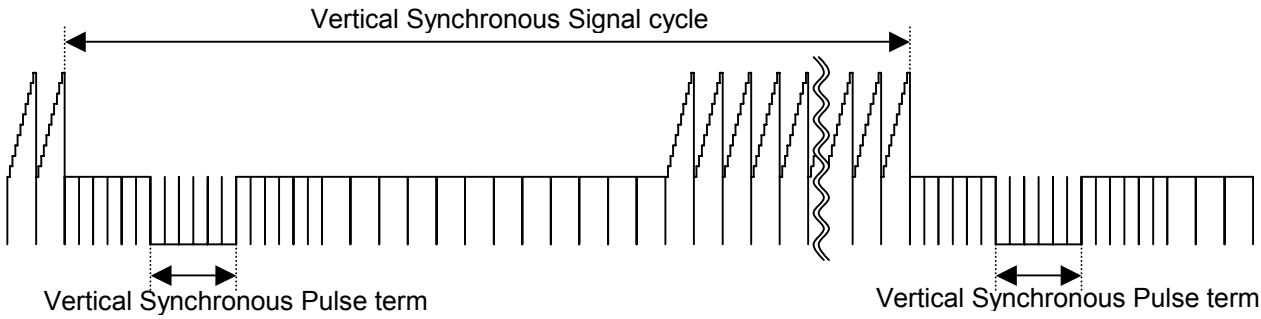
*1: CSBLA503KE5ZF10 at MURATA

*2: NTSC/PAL SW
NTSC : GND
PAL :Vcc,and 9 to10pin is 360 ohm, 10 to 11pin is 2 k ohm

■APPLICATION NOTES

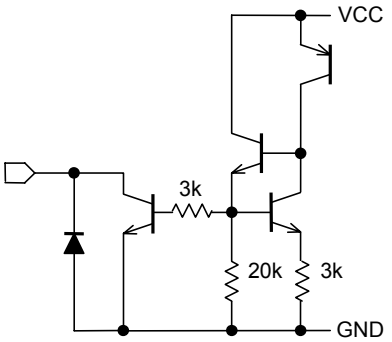
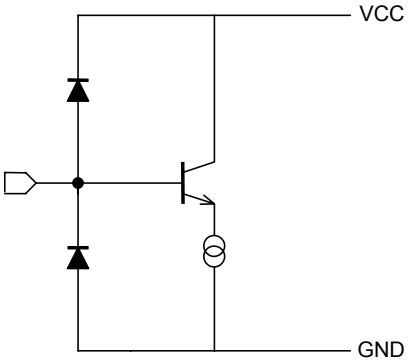
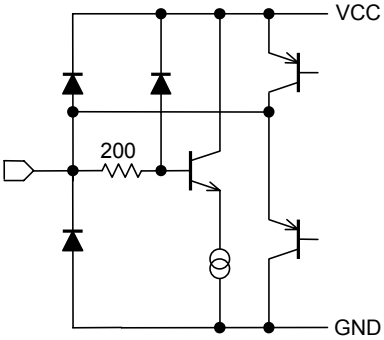
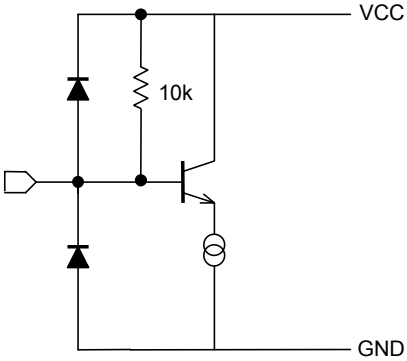
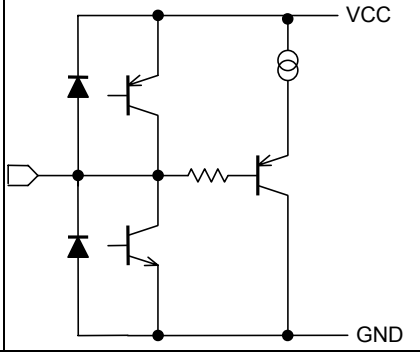
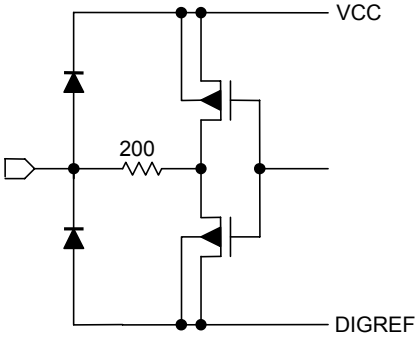
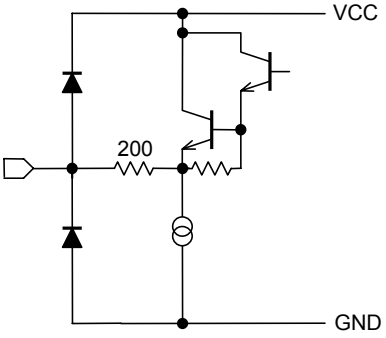
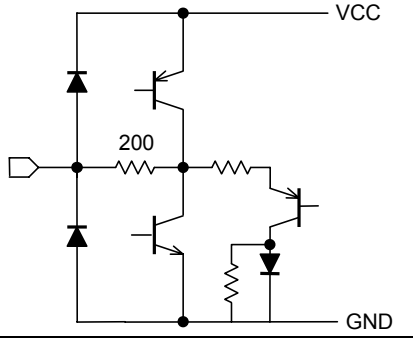
- The ratio of the vertical synchronous pulse term and the vertical synchronous signal cycle
  Please adjust following expression.

  The vertical synchronous signal cycle / The vertical synchronous pulse term ≥ 75 (see following figure)



- The pulse width of horizontal synchronous signal shall be set 3.7 to 5.7μs

■ EQUIVALENT CIRCUIT

No.	NAME	INSIDE EQUIVALENT CIRCUIT	No.	NAME	INSIDE EQUIVALENT CIRCUIT
1	Csync. Out		10	VCO Filter 2	
2	Sync. In		11	VCO Filter 1	
3	Vcc		12	LPF	
4 5 7 8	VD HD SW BGP		6 13	DIGREF GND	
9	VCO Out		14	VS	

MEMO