184pin Registered DIMM
SPD Specification(256Mb B-die base)

Rev. 0.4

Jan. 2001

Revision 0.0 (December 1999)
1. First release for internal use only.

Revision 0.1 (February 2000)
1. First edition for external release.

Revision 0.2 (April 2000)
1. Byte 9, Byte10 : Add tCC and tAC at CL=2.5 in A0 (DDR200@CL=2)and A2(DDR266@CL=2).
2. Byte 23, Bte24 : Add tCC and tAC at CL=2 in B0 (DDR266@CL=2.5).

Revision 0.3 (June 2000)
1. Byte 85 : Changed PCB Revision from T0 to T1.

Revision 0.4 (Jan 2001)
1. Byte 30 : Changed tRAS of B0 from 48ns to 45ns.

M383L2828BT1-CA0/B0/A2

- Organization : 128MX72
- Composition : 128MX4 *18*2
- Used component part # : K4H560438B-TCA0/B0/A2
- # of rows in module : 2 row
- # of banks in component : 4 banks
- Feature : 1,700 mil height & double sided component
- Refresh : 8K/64ms
- Bin Sort : A0 (DDR200@CL=2),B0 (DDR266@CL=2.5), A2(DDR266@CL=2)
- **Contents** :

Byte #	Function described	Function Supported			Hex value			Note
		A0	B0	A2	A0	B0	A2	
0	Defines # of Bytes written into serial memory at module manufacturer	128bytes			80h			
1	Total # of Bytes of SPD memory device	256bytes (2K-bit)			08h			
2	Fundamental memory type	SDRAM DDR			07h			
3	# of row address on this assembly	13			0Dh			1
4	# of column address on this assembly	11			0Bh			1
5	# of module Rows on this assembly	2 Row			02h			
6	Data width of this assembly	72 bits			48h			
7	.....Data width of this assembly	-			00h			
8	VDDQ and interface standard of this assembly	SSTL 2.5V			04h			
9	DDR SDRAM cycle time at CAS Latency =2.5	8ns	7.5ns	7ns	80h	75h	70h	2
10	DDR SDRAM Access time from clock at CL=2.5	±0.8ns	±0.75n	±0.75n	80h	75h	75h	2
11	DIMM configuration type(Non-parity, Parity, ECC)	ECC			02h			
12	Refresh rate & type	7.8us & Self refresh			82h			
13	Primary DDR SDRAM width	x4			04h			
14	Error checking DDR SDRAM data width	x4			04h			
15	Minimum clock delay for back-to-back random column address	tCCD=1CLK			01h			
16	DDR SDRAM device attributes : Burst lengths supported	2,4,8			0Eh			
17	DDR SDRAM device attributes : # of banks on each DDR SDRAM	4 banks			04h			
18	DDR SDRAM device attributes : CAS Latency supported	2,2.5			0Ch			
19	DDR SDRAM device attributes : CS Latency	0CLK			01h			
20	DDR SDRAM device attributes : WE Latency	1CLK			02h			
21	DDR SDRAM module attributes	Registered address& control inputs and On-card DLL			26h			
22	DDR SDRAM device attributes : General	+/-0.2V voltage tolerance			00h			
23	DDR SDRAM cycle time at CL =2.0	10ns	10ns	7.5ns	A0h	A0h	75h	2
24	DDR SDRAM Access time from clock at CL =2.0	±0.8ns	±0.75n	±0.75	80h	75h	75h	2
25	DDR SDRAM cycle time at CL =1.5	-	-	-	00h			2
26	DDR SDRAM Access time from clock at CL =1.5	-	-	-	00h			2
27	Minimum row precharge time (=tRP)	20ns	20ns	20ns	50h	50h	50h	
28	Minimum row activate to row active delay(=tRRD)	15ns	15ns	15ns	3Ch	3Ch	3Ch	
29	Minimum RAS to CAS delay(=tRCD)	20ns	20ns	20ns	50h	50h	50h	
30	Minimum active to precharge time(=tRAS)	48ns	45ns	45ns	30h	2Dh	2Dh	
31	Module ROW density	512MB			80h			
32	Command and address signal input setup time	1.1ns	0.9ns	0.9ns	B0h	90h	90h	
33	Command and address signal input hold time	1.1ns	0.9ns	0.9ns	B0h	90h	90h	
34	Data signal input setup time	0.6ns	0.5ns	0.5ns	60h	50h	50h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported			Hex value			Note
		A0	B0	A2	A0	B0	A2	
35	Data signal input hold time	0.6ns	0.5ns	0.5ns	60h	50h	50h	
36-61	Superset information (may be used in future)	-			00h			
62	SPD data revision code	Initial release			00h			
63	Checksum for Bytes 0 ~ 62	-			95h	11h	E1h	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65 - 71	..... Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			
73	Manufacturer part # (Memory Module)	M			4Dh			
74	Manufacturer part # (DIMM Configuraion)	3			33h			
75	Manufacturer part # (Data bits & Module type)	Blank			20h			
76	..... Manufacturer part # (Data bits & Module type)	8			38h			
77	..... Manufacturer part # (Data bits & Module type)	3			33h			
78	Manufacturer part # (Operating Voltage)	L			4Ch			
79	Manufacturer part # (Module depth)	2			32h			
80	Manufacturer part # (Module depth)	8			38h			
81	Manufacturer part # (Refresh, # of rows in comp.&interface)	2			32h			
82	Manufacturer part # (Composition component)	8			38h			
83	Manufacturer part # (Component Revision)	B-die			42h			
84	Manufacturer part # (Package type)	T			54h			
85	Manufacturer part # (PCB Revision)	1			31h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	A	B	A	41h	42h	41h	
89	Manufacturer part # (Minimum cycle time)	0	0	2	30h	30h	32h	
90	Manufacturer part # (T.B.D)	Blank			20h			
91	Manufacturer revison code (For PCB)	0			30h			
92	Manufacturer revison code (For component)	B-die			42h			
93	Manufacturing date (Week)	-			-			3
94	Manufacturing date (Year)	-			-			3
95~98	Assembly serial #	-			-			4
99~127	Manufacturer specific data (may be used in future)	Undefined			00h			5
128~255	Open for customer use	Undefined			00h			5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and coded with 00h'.