



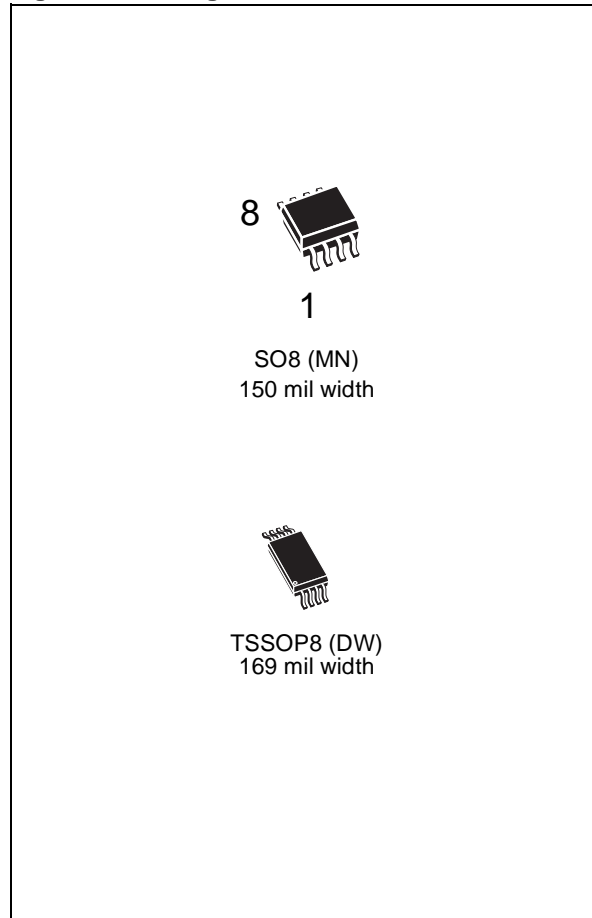
M34D64

64 Kbit Serial I²C Bus EEPROM With Hardware Write Control on Top Quarter of Memory

FEATURES SUMMARY

- Two Wire I²C Serial Interface
Supports 400 kHz Protocol
- Single Supply Voltage:
 - 2.5V to 5.5V for M34D64-W
 - 1.8V to 5.5V for M34D64-R
- Hardware Write Control of the top quarter of memory
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 1M Erase/Write Cycles
- More than 40 Year Data Retention

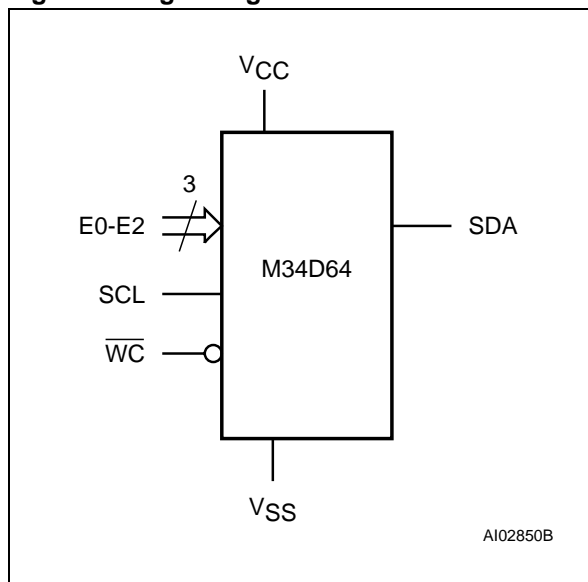
Figure 1. Packages



SUMMARY DESCRIPTION

These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192 x 8.

Figure 2. Logic Diagram



These devices are compatible with the I²C memory protocol. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I²C bus definition.

The device behaves as a slave in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and RW bit (as described in Table 2), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

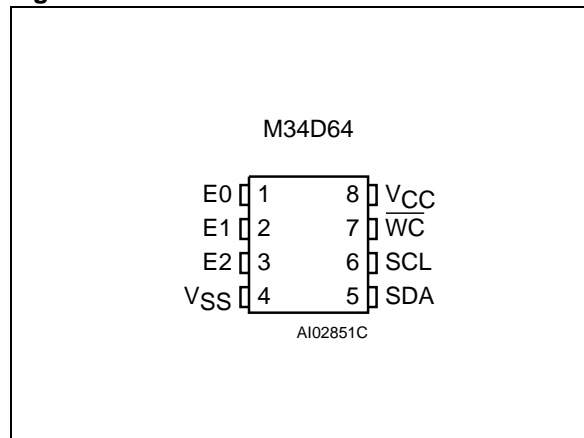
Table 1. Signal Names

| | |
|------------|----------------|
| E0, E1, E2 | Chip Enable |
| SDA | Serial Data |
| SCL | Serial Clock |
| WC | Write Control |
| VCC | Supply Voltage |
| VSS | Ground |

Power On Reset: VCC Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. The internal reset is held active until VCC has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when VCC drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid VCC must be applied before applying any logic signal.

Figure 3. SO and TSSOP Connections



Note: 1. See page 17 (onwards) for package dimensions, and how to identify pin-1.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (Figure 5 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 5 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code.

Write Control (\overline{WC})

The hardware Write Control pin (\overline{WC}) is useful for protecting the top quarter of the memory (as shown in Figure 4) from inadvertent erase or write. The Write Control signal is used to enable

($\overline{WC}=V_{IL}$) or disable ($\overline{WC}=V_{IH}$) write instructions to the top quarter of the memory area. When unconnected, the \overline{WC} input is internally read as V_{IL}, and write operations are allowed.

Figure 4. Memory Map showing Write Control Area

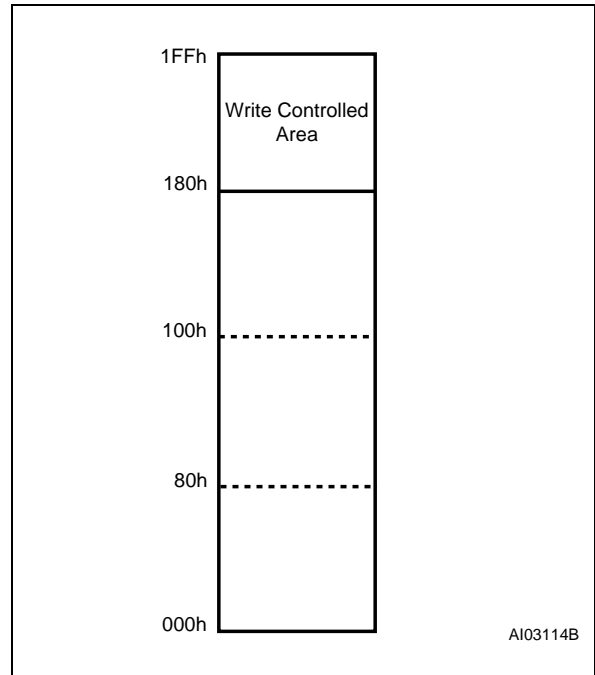


Figure 5. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

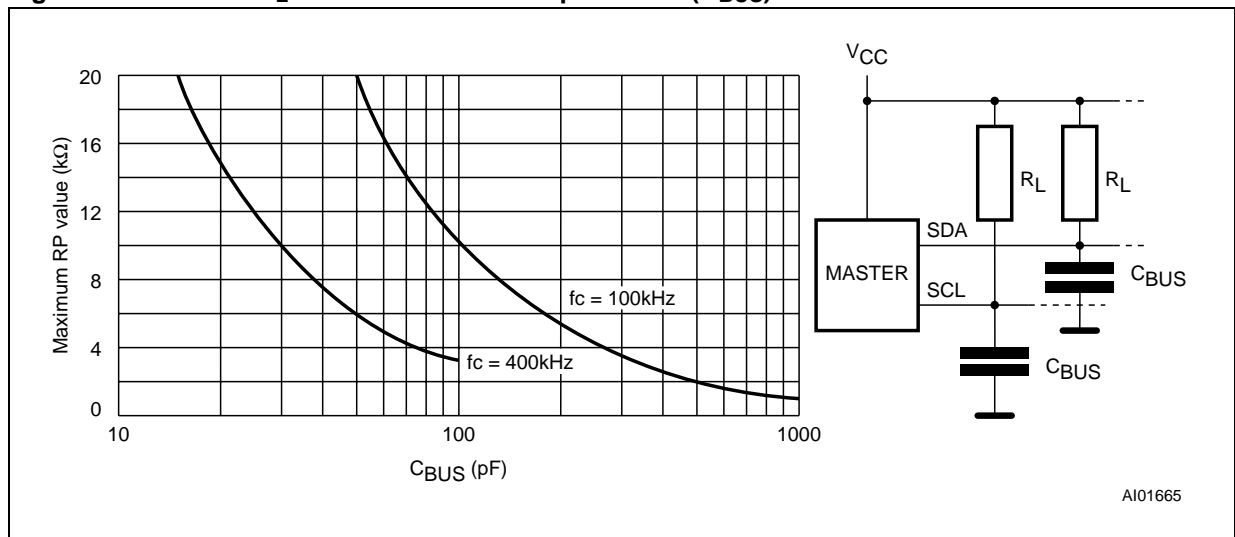


Figure 6. I²C Bus Protocol

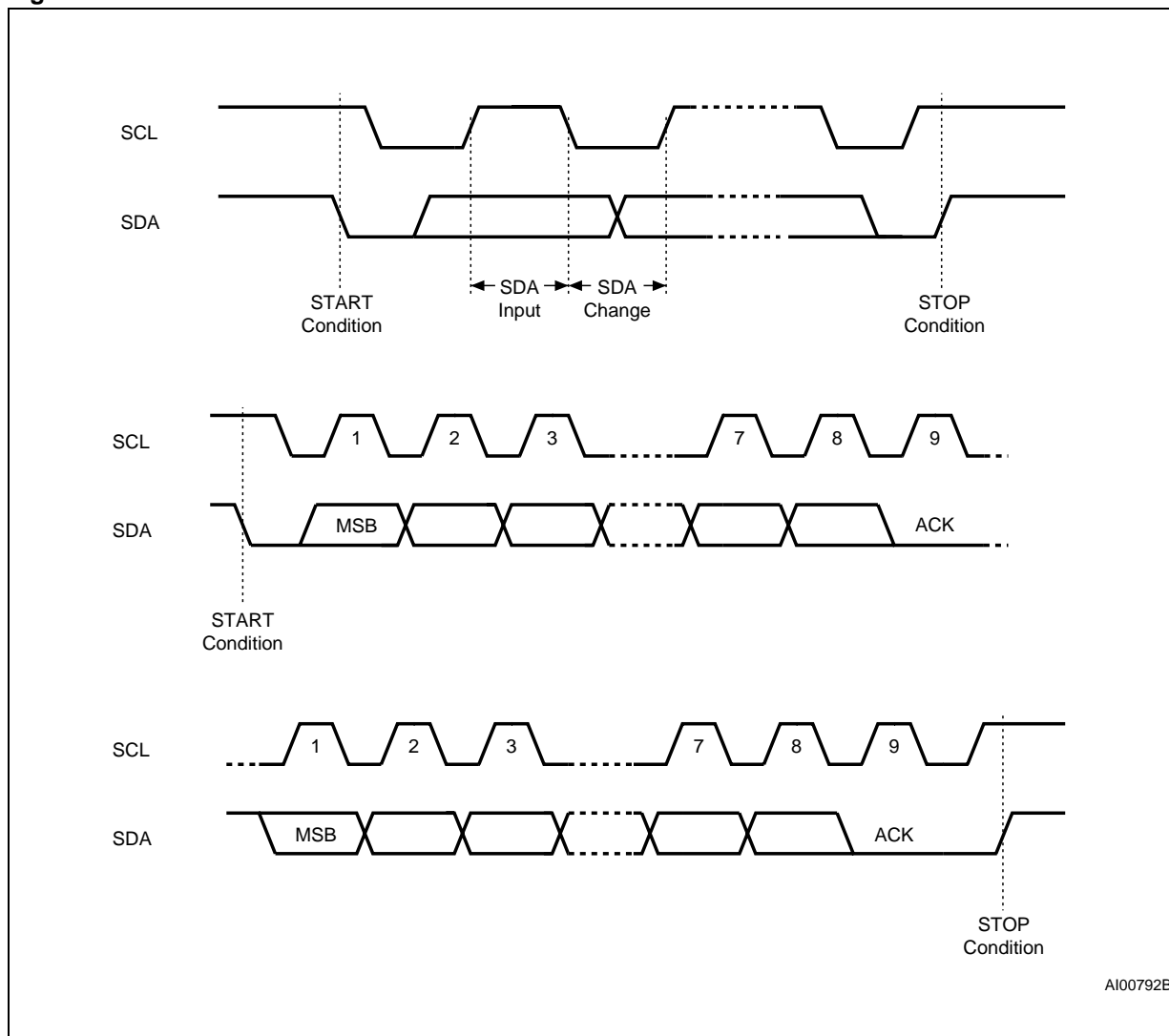


Table 2. Device Select Code

| | Device Type Identifier ¹ | | | | Chip Enable Address ² | | | R \bar{W} |
|--------------------|-------------------------------------|----|----|----|----------------------------------|----|----|-------------|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Device Select Code | 1 | 0 | 1 | 0 | E2 | E1 | E0 | R \bar{W} |

Note: 1. The most significant bit, b7, is sent first.

2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 3. Most Significant Byte

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 |
|-----|-----|-----|-----|-----|-----|----|----|

Table 4. Least Significant Byte

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|----|----|----|----|----|----|----|----|

DEVICE OPERATION

The device supports the I²C protocol. This is summarized in Figure 6. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M34D64 device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls

Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to eight memory devices can be connected on a single I²C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received on Serial Data (SDA), the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

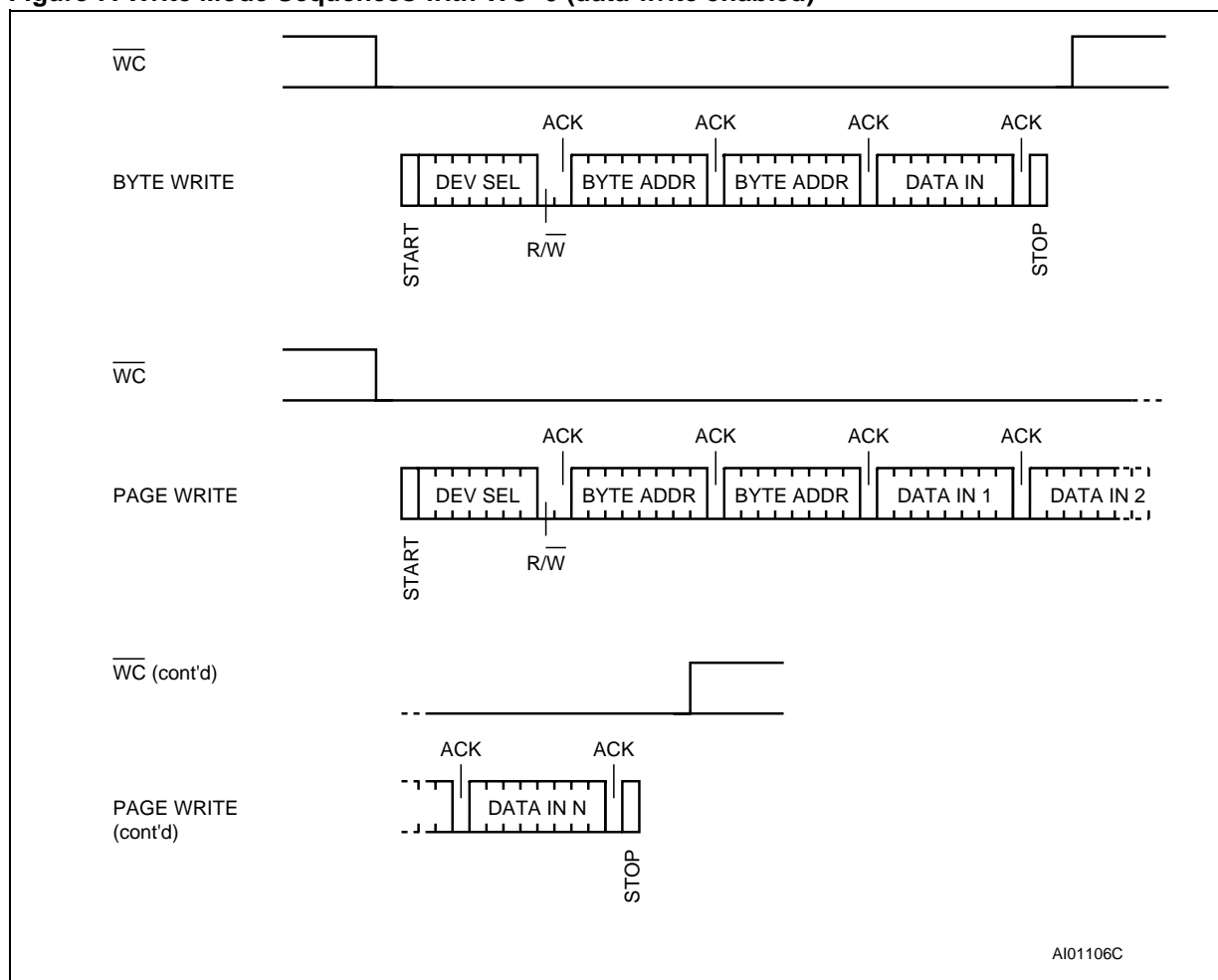
The 8th bit is the Read/Write bit (\overline{RW}). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselected itself from the bus, and goes into Stand-by mode.

Table 5. Operating Modes

| Mode | \overline{RW} bit | \overline{WC} ¹ | Bytes | Initial Sequence |
|----------------------|---------------------|------------------------------|-------|---|
| Current Address Read | 1 | X | 1 | START, Device Select, $\overline{RW} = 1$ |
| Random Address Read | 0 | X | 1 | START, Device Select, $\overline{RW} = 0$, Address |
| | 1 | X | | reSTART, Device Select, $\overline{RW} = 1$ |
| Sequential Read | 1 | X | ≥ 1 | Similar to Current or Random Address Read |
| Byte Write | 0 | V _{IL} | 1 | START, Device Select, $\overline{RW} = 0$ |
| Page Write | 0 | V _{IL} | ≤ 32 | START, Device Select, $\overline{RW} = 0$ |

Note: 1. X = V_{IH} or V_{IL}.

Figure 7. Write Mode Sequences with $\overline{WC}=0$ (data write enabled)

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Write Operations

Following a Start condition the bus master sends a Device Select Code with the R/W bit reset to 0. The device acknowledges this, as shown in Figure 7, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte(s).

Writing to the memory may be inhibited if Write Control (\overline{WC}) is driven High. Any Write instruction with Write Control (\overline{WC}) driven High (during a period of time from the Start condition until the end of the two address bytes) will not modify the contents of the top quarter of the memory.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 3) is sent first, followed by the Least Significant Byte (Table 4). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page

Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

Byte Write

After the Device Select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected (top quarter of the memory), by Write Control (\overline{WC}) being driven High, the location is not modified. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7.

Page Write

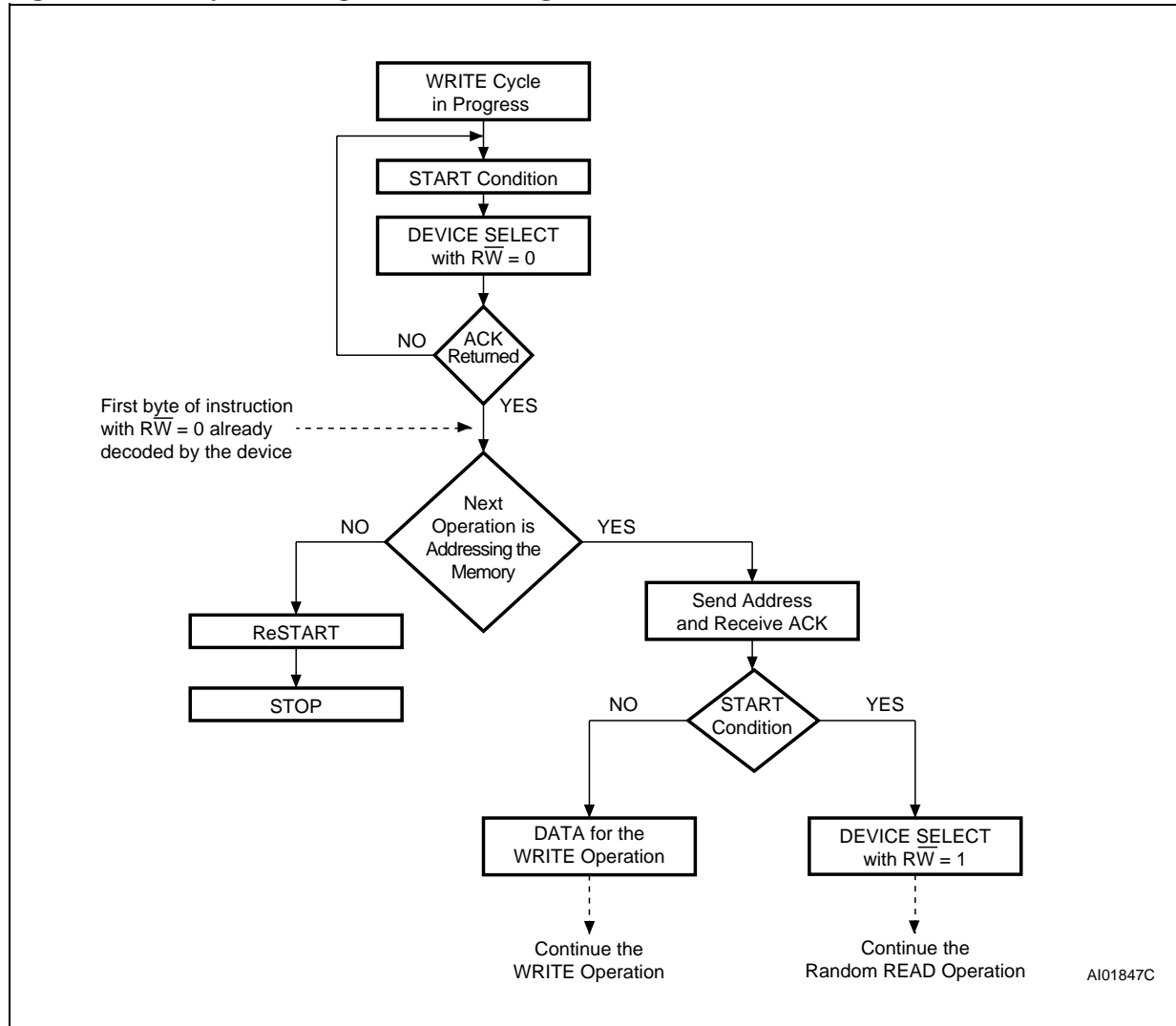
The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b12-b5) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as

data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data. If Write Control (WC) is High, the contents of the addressed top quarter of the memory location are

not modified. After each byte is transferred, the internal byte address counter (the 5 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 8. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in Tables 13 and 14, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

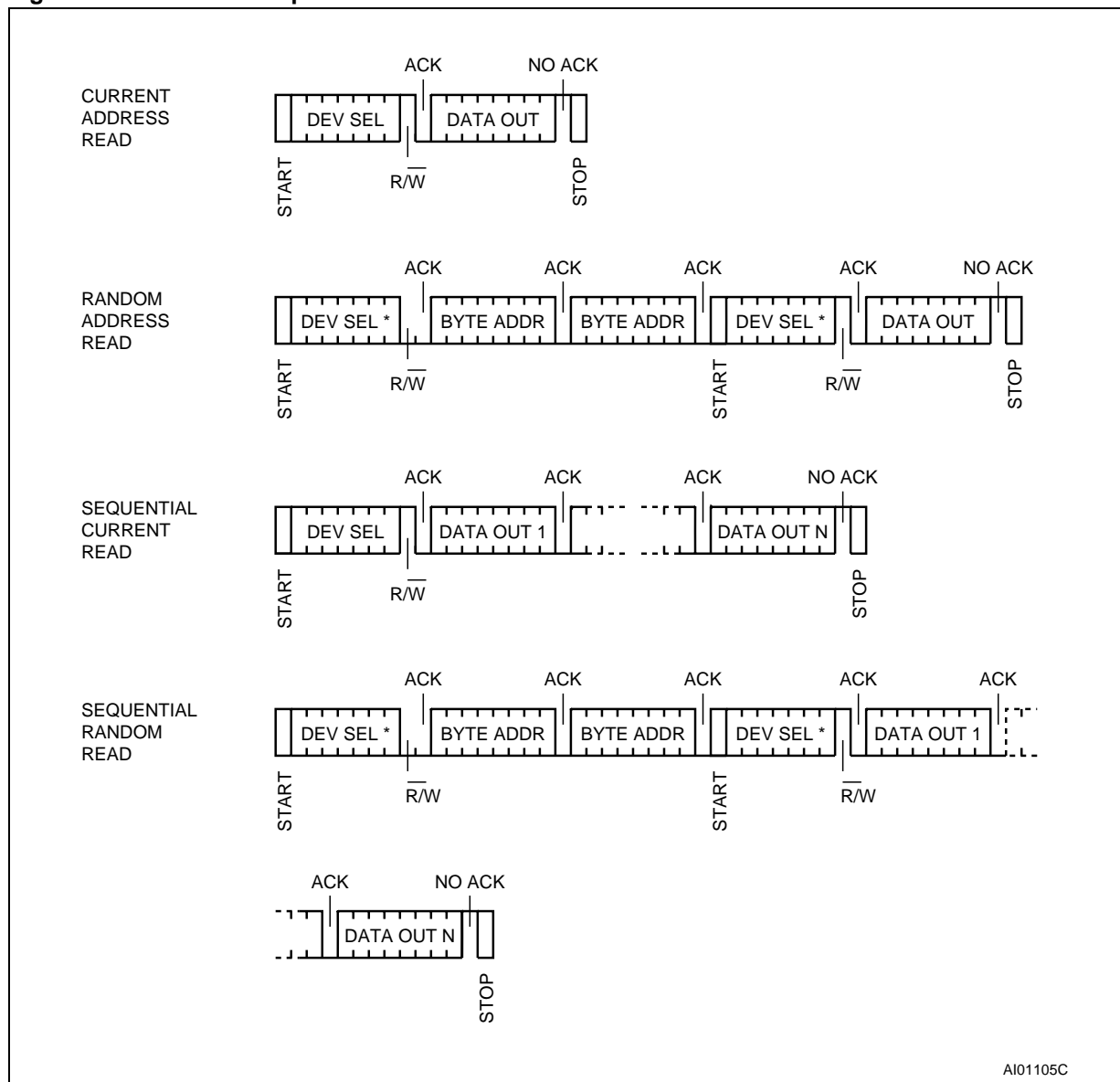
The sequence, as shown in Figure 8, is:

- Initial condition: a Write cycle is in progress.

- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).

- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 9. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

Read Operations

Read operations are performed independently of the state of the Write Control (WC) signal.

Random Address Read

A dummy Write is performed to load the address into the address counter (as shown in Figure 9) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/W bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master

must not acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 9, *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 9.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output.

After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|-------------------|---|-------|------------|------|
| T _{STG} | Storage Temperature | -65 | 150 | °C |
| T _{LEAD} | Lead Temperature during Soldering | | 235 235 | °C |
| V _{IO} | Input or Output range | -0.6 | 6.5 | V |
| V _{CC} | Supply Voltage | -0.3 | 6.5 | V |
| V _{ESD} | Electrostatic Discharge Voltage (Human Body model) ² | -4000 | 4000 | V |

Note: 1. IPC/JEDEC J-STD-020A

2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measure-

ment Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating Conditions (M34D64-W)

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|-------------------------------|------|------|------|
| V _{CC} | Supply Voltage | 2.5 | 5.5 | V |
| T _A | Ambient Operating Temperature | -40 | 85 | °C |

Table 8. Operating Conditions (M34D64-R)

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|-------------------------------|------|------|------|
| V _{CC} | Supply Voltage | 1.8 | 5.5 | V |
| T _A | Ambient Operating Temperature | -40 | 85 | °C |

Table 9. AC Measurement Conditions

| Symbol | Parameter | Min. | Max. | Unit |
|--------|--|--|------|------|
| C_L | Load Capacitance | 100 | | pF |
| | Input Rise and Fall Times | | 50 | ns |
| | Input Levels | 0.2V _{CC} to 0.8V _{CC} | | V |
| | Input and Output Timing Reference Levels | 0.3V _{CC} to 0.7V _{CC} | | V |

Figure 10. AC Measurement I/O Waveform

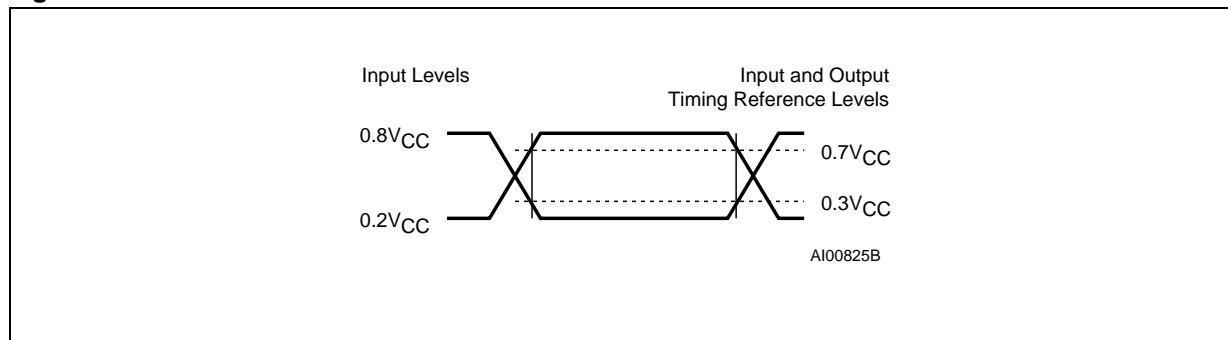


Table 10. Input Parameters

| Symbol | Parameter ^{1,2} | Test Condition | Min. | Max. | Unit |
|-----------|---|----------------------|------|------|------------|
| C_{IN} | Input Capacitance (SDA) | | | 8 | pF |
| C_{IN} | Input Capacitance (other pins) | | | 6 | pF |
| Z_{WCL} | \overline{WC} Input Impedance | $V_{IN} < 0.5 V$ | 50 | 300 | k Ω |
| Z_{WCH} | \overline{WC} Input Impedance | $V_{IN} > 0.7V_{CC}$ | 500 | | k Ω |
| t_{NS} | Pulse width ignored (Input Filter on SCL and SDA) | Single glitch | | 100 | ns |

Note: 1. $T_A = 25^\circ C$, $f = 400 kHz$
 2. Sampled only, not 100% tested.

Table 11. DC Characteristics (M34D64-W)

| Symbol | Parameter | Test Condition (in addition to those in Table 7) | Min. | Max. | Unit |
|-----------|--|--|-------------|-------------|---------|
| I_{LI} | Input Leakage Current (SCL, SDA) | $V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode | | ± 2 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = V_{SS}$ or V_{CC} , SDA in Hi-Z | | ± 2 | μA |
| I_{CC} | Supply Current | $V_{CC} = 2.5V$, $f_c = 400kHz$ (rise/fall time < 30ns) | | 1 | mA |
| I_{CC1} | Stand-by Supply Current | $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5V$ | | 10 | μA |
| | | $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5V$ | | 2 | μA |
| V_{IL} | Input Low Voltage (E2, E1, E0, SCL, SDA) | | -0.3 | $0.3V_{CC}$ | V |
| | Input Low Voltage (\overline{WC}) | | -0.3 | 0.5 | V |
| V_{IH} | Input High Voltage (E2, E1, E0, SCL, SDA, \overline{WC}) | | $0.7V_{CC}$ | $V_{CC}+1$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1 mA$, $V_{CC} = 2.5V$ | | 0.4 | V |

Table 12. DC Characteristics (M34D64-R)

| Symbol | Parameter | Test Condition (in addition to those in Table 8) | Min. | Max. | Unit |
|-----------|--|--|-------------|-------------|---------|
| I_{LI} | Input Leakage Current (SCL, SDA) | $V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode | | ± 2 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = V_{SS}$ or V_{CC} , SDA in Hi-Z | | ± 2 | μA |
| I_{CC} | Supply Current | $V_{CC} = 1.8V$, $f_c = 100kHz$ (rise/fall time < 30ns) | | 0.8 | mA |
| I_{CC1} | Stand-by Supply Current | $V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 1.8V$ | | 0.2 | μA |
| V_{IL} | Input Low Voltage (E2, E1, E0, SCL, SDA) | | -0.3 | $0.3V_{CC}$ | V |
| | Input Low Voltage (\overline{WC}) | | -0.3 | 0.5 | V |
| V_{IH} | Input High Voltage (E2, E1, E0, SCL, SDA, \overline{WC}) | | $0.7V_{CC}$ | $V_{CC}+1$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 0.7 mA$, $V_{CC} = 1.8V$ | | 0.2 | V |

Table 13. AC Characteristics (M34D64-W)

| Test conditions specified in Table 9 and Table 7 | | | | | |
|--|--------------|--|------|------|------|
| Symbol | Alt. | Parameter | Min. | Max. | Unit |
| f_c | f_{SCL} | Clock Frequency | | 400 | kHz |
| t_{CHCL} | t_{HIGH} | Clock Pulse Width High | 600 | | ns |
| t_{CLCH} | t_{LOW} | Clock Pulse Width Low | 1300 | | ns |
| t_{CH1CH2} | t_R | Clock Rise Time | | 300 | ns |
| t_{CL1CL2} | t_F | Clock Fall Time | | 300 | ns |
| t_{DH1DH2}^2 | t_R | SDA Rise Time | 20 | 300 | ns |
| t_{DL1DL2}^2 | t_F | SDA Fall Time | 20 | 300 | ns |
| t_{DXCX} | $t_{SU:DAT}$ | Data In Set Up Time | 100 | | ns |
| t_{CLDX} | $t_{HD:DAT}$ | Data In Hold Time | 0 | | ns |
| t_{CLQX} | t_{DH} | Data Out Hold Time | 200 | | ns |
| t_{CLQV}^3 | t_{AA} | Clock Low to Next Data Valid (Access Time) | 200 | 900 | ns |
| t_{CHDX}^1 | $t_{SU:STA}$ | Start Condition Set Up Time | 600 | | ns |
| t_{DLCL} | $t_{HD:STA}$ | Start Condition Hold Time | 600 | | ns |
| t_{CHDH} | $t_{SU:STO}$ | Stop Condition Set Up Time | 600 | | ns |
| t_{DHDL} | t_{BUF} | Time between Stop Condition and Next Start Condition | 1300 | | ns |
| t_W | t_{WR} | Write Time | | 10 | ms |

Note: 1. For a reSTART condition, or following a Write cycle.

2. Sampled only, not 100% tested.

3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Table 14. AC Characteristics (M34D64-R)

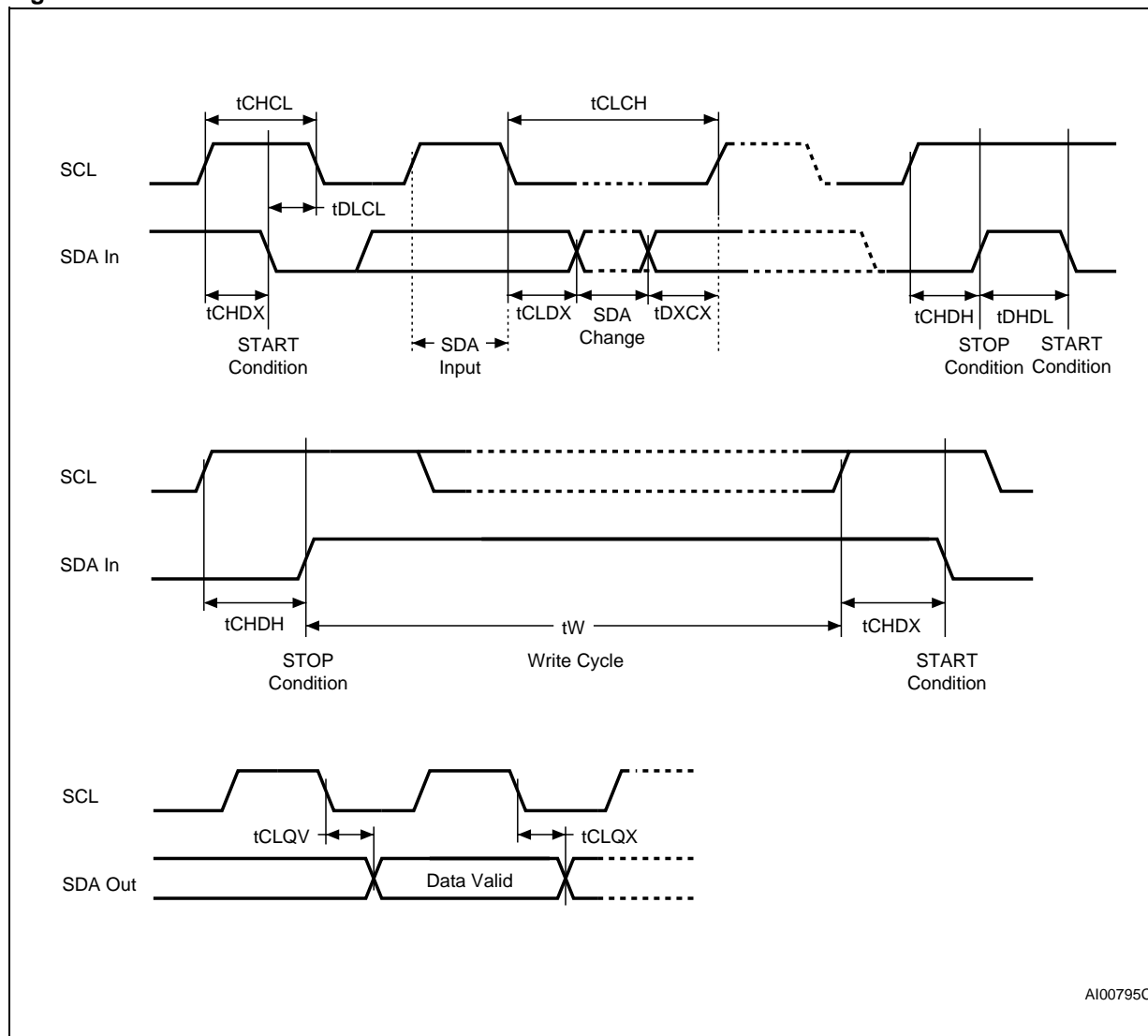
| Test conditions specified in Table 9 and Table 8 | | | | | |
|--|--------------|--|------|------|------|
| Symbol | Alt. | Parameter | Min. | Max. | Unit |
| f_C | f_{SCL} | Clock Frequency | | 400 | kHz |
| t_{CHCL} | t_{HIGH} | Clock Pulse Width High | 600 | | ns |
| t_{CLCH} | t_{LOW} | Clock Pulse Width Low | 1300 | | ns |
| t_{CH1CH2} | t_R | Clock Rise Time | | 300 | ns |
| t_{CL1CL2} | t_F | Clock Fall Time | | 300 | ns |
| t_{DH1DH2}^2 | t_R | SDA Rise Time | 20 | 300 | ns |
| t_{DL1DL2}^2 | t_F | SDA Fall Time | 20 | 300 | ns |
| t_{DXCX} | $t_{SU:DAT}$ | Data In Set Up Time | 100 | | ns |
| t_{CLDX} | $t_{HD:DAT}$ | Data In Hold Time | 0 | | ns |
| t_{CLQX} | t_{DH} | Data Out Hold Time | 200 | | ns |
| t_{CLQV}^3 | t_{AA} | Clock Low to Next Data Valid (Access Time) | 200 | 900 | ns |
| t_{CHDX}^1 | $t_{SU:STA}$ | Start Condition Set Up Time | 600 | | ns |
| t_{DLCL} | $t_{HD:STA}$ | Start Condition Hold Time | 600 | | ns |
| t_{CHDH} | $t_{SU:STO}$ | Stop Condition Set Up Time | 600 | | ns |
| t_{DHDL} | t_{BUF} | Time between Stop Condition and Next Start Condition | 1300 | | ns |
| t_W | t_{WR} | Write Time | | 10 | ms |

Note: 1. For a reSTART condition, or following a Write cycle.

2. Sampled only, not 100% tested.

3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

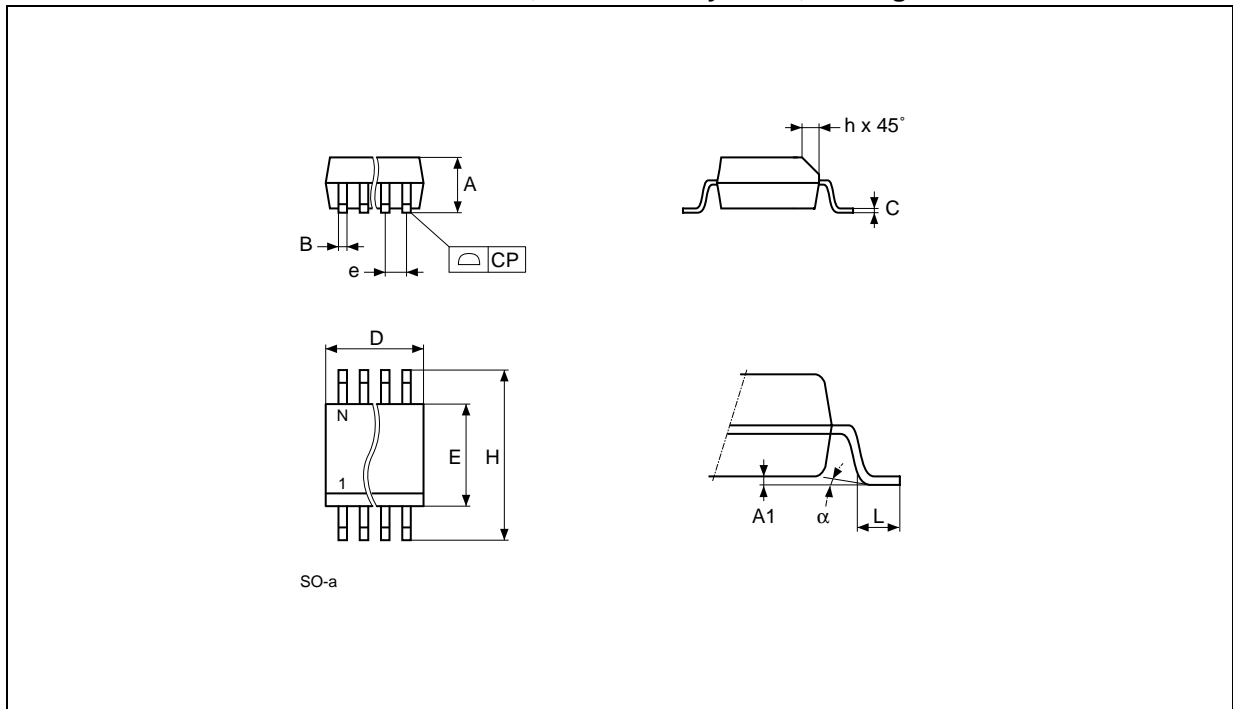
Figure 11. AC Waveforms



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PACKAGE MECHANICAL

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Outline

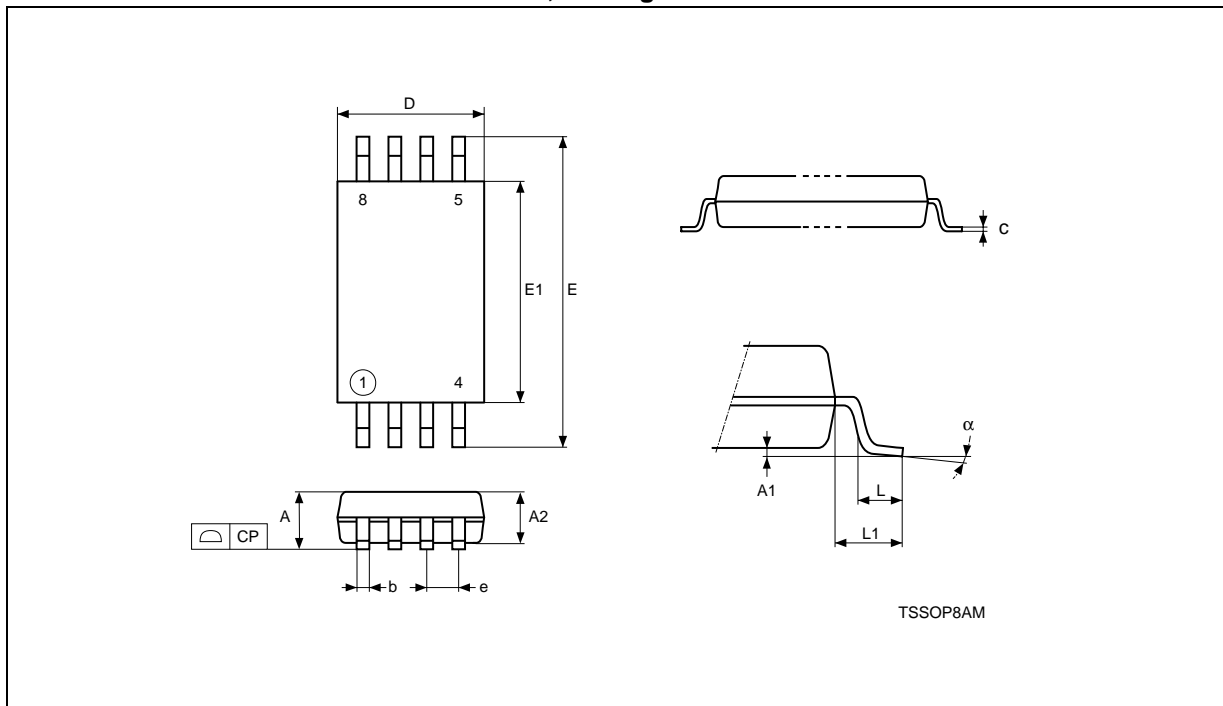


Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

| Symb. | mm | | | inches | | |
|-------|------|------|------|--------|-------|-------|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | 1.35 | 1.75 | | 0.053 | 0.069 |
| A1 | | 0.10 | 0.25 | | 0.004 | 0.010 |
| B | | 0.33 | 0.51 | | 0.013 | 0.020 |
| C | | 0.19 | 0.25 | | 0.007 | 0.010 |
| D | | 4.80 | 5.00 | | 0.189 | 0.197 |
| E | | 3.80 | 4.00 | | 0.150 | 0.157 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | | 5.80 | 6.20 | | 0.228 | 0.244 |
| h | | 0.25 | 0.50 | | 0.010 | 0.020 |
| L | | 0.40 | 0.90 | | 0.016 | 0.035 |
| alpha | | 0° | 8° | | 0° | 8° |
| N | | 8 | | | 8 | |
| CP | | | 0.10 | | | 0.004 |

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Outline



Notes: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline, Package Mechanical Data

| Symbol | mm | | | inches | | |
|--------|-------|-------|-------|--------|--------|--------|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.800 | 1.050 | 0.0394 | 0.0315 | 0.0413 |
| b | | 0.190 | 0.300 | | 0.0075 | 0.0118 |
| c | | 0.090 | 0.200 | | 0.0035 | 0.0079 |
| CP | | | 0.100 | | | 0.0039 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | – | – | 0.0256 | – | – |
| E | 6.400 | 6.200 | 6.600 | 0.2520 | 0.2441 | 0.2598 |
| E1 | 4.400 | 4.300 | 4.500 | 0.1732 | 0.1693 | 0.1772 |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | | | 0.0394 | | |
| α | | 0° | 8° | | 0° | 8° |

PART NUMBERING

Table 15. Ordering Information Scheme

| | | | | | | |
|---|--------|---|---|----|---|---|
| Example: | M34D64 | - | W | MN | 6 | T |
| Device Type | | | | | | |
| M34 = I ² C Application Specific Standard Product serial access EEPROM | | | | | | |
| Device Function | | | | | | |
| 64 = 64 Kbit (8192 x 8) | | | | | | |
| Operating Voltage | | | | | | |
| W = V _{CC} = 2.5 to 5.5V | | | | | | |
| R = V _{CC} = 1.8 to 5.5V | | | | | | |
| Package | | | | | | |
| MN = SO8 (150 mil width) | | | | | | |
| DW = TSSOP8 (169 mil width) | | | | | | |
| Temperature Range | | | | | | |
| 6 = -40 to 85 °C | | | | | | |
| Option | | | | | | |
| T = Tape & Reel Packing | | | | | | |

Devices are shipped from the factory with the memory content set at all 1s (FFh).

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY**Table 16. Document Revision History**

| Date | Rev. | Description of Revision |
|-------------|-------------|--|
| 23-Mar-1999 | 1.0 | Document written |
| 09-Jun-1999 | 1.1 | Memory Map illustration added. Line removed from Tab-2 |
| 16-Nov-2000 | 1.2 | M34D32 removed; PSDIP8 package removed; 4.5 to 5.5V and 1.8 to 3.6V ranges removed; 0 to 70°C and -20 to 85°C ranges removed |
| 13-Sep-2002 | 2.0 | New edition. TSSOP8 package added |

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