



## Dolby Pro Logic II / Virtual Dolby Surround Decoder

### ■ General Description

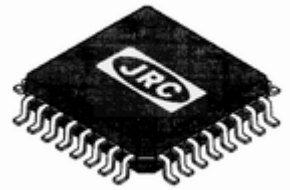
The NJU26106 is a digital audio signal decoder that provides the function of Dolby Pro Logic II and Virtual Dolby Surround.

The NJU26106 processes the stereo matrix-encoded signal into spacious sound of 5.1 channels by Dolby Pro Logic II and Bass Management System. Also not matrix-encoded audio signal can be processed into effective spacious sound by Music mode.

The decoded 5-channel signal can be downmixed into 2-channel virtual surround output by the Dolby Virtual technology.

The applications of the NJU26106 are suitable for multi-channel products such as AV AMP and Car Audio, or ordinary audio products such as small speaker system.

### ■ Package



NJU26106

### ■ FEATURES

- 5.1 Channel signal outputs by Dolby Pro Logic II
- 2 Channel outputs by Virtual Dolby Surround
- Movie mode / Music mode
- Available for center width control, dimension control, panorama mode Music mode and Custom mode
- Two kinds of micro computer interface
  - I<sup>2</sup>C Bus (standard-mode/100Kbps)
  - 4-Wire Serial Bus (4-Wire: clock, enable, input data, output data)

### ■ Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 40MHz
- Digital Audio Interface : 2 Input ports / 3 Output ports
- Power Supply : DSP Core : 2.5V I/O interface: 2.5V(+3.3V tolerant)  
I/O interface: 2.5V(+3.3V tolerant)
- Package : QFP 32pin

\* Note1: The Word "DOLBY", "Pro Logic" and the double D mark are trademarks of Dolby Laboratories.

The NJU26106 can only be delivered to licensees of Dolby Laboratories.

Please refer to the licensing application manual issued by Dolby Laboratories.

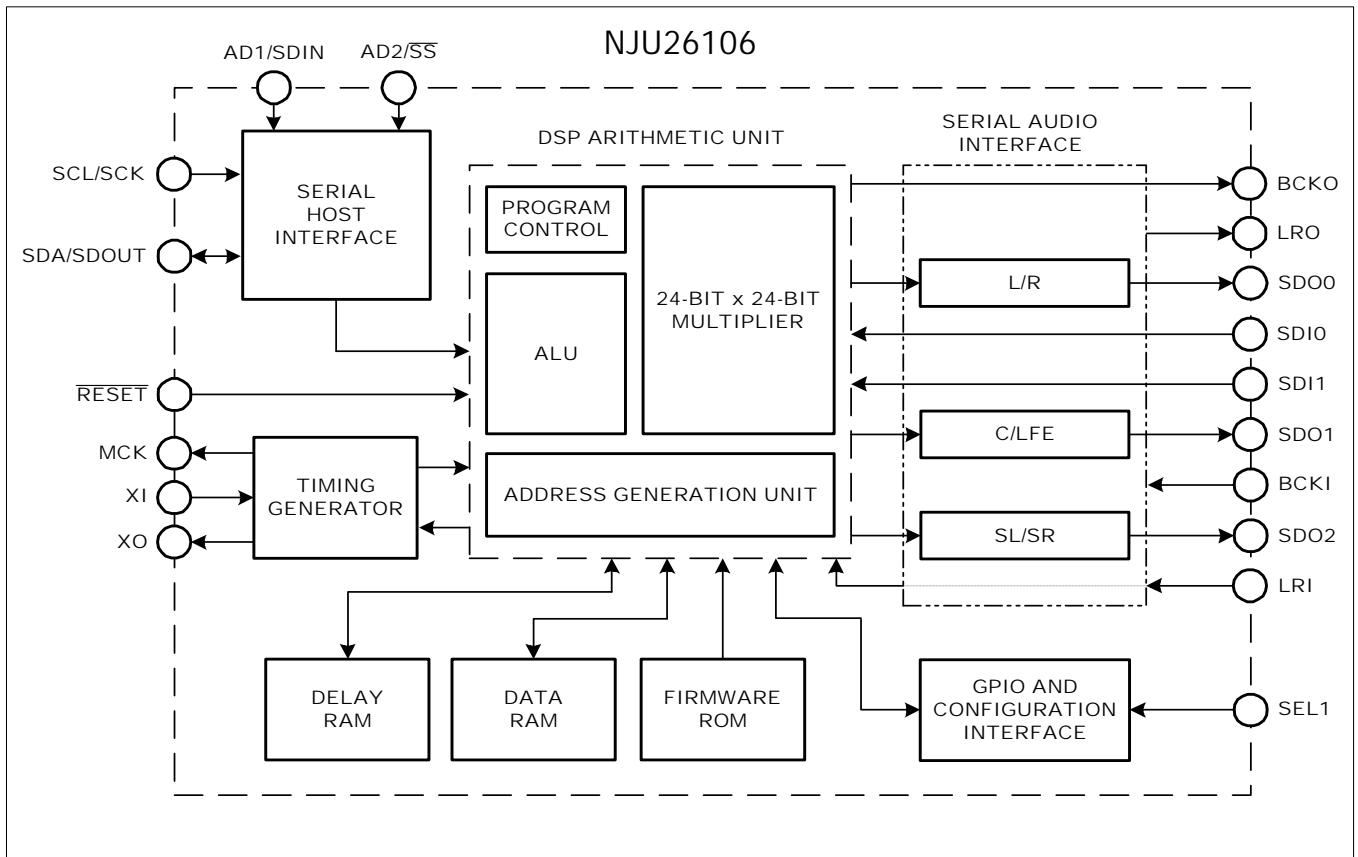
\* Note2: Purchase of I<sup>2</sup>C components of New Japan Radio Co., Ltd or one of sublicensed Associated Companies

conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system,

provided that the system conforms to the I<sup>2</sup>C Standard specification as defined by Philips.

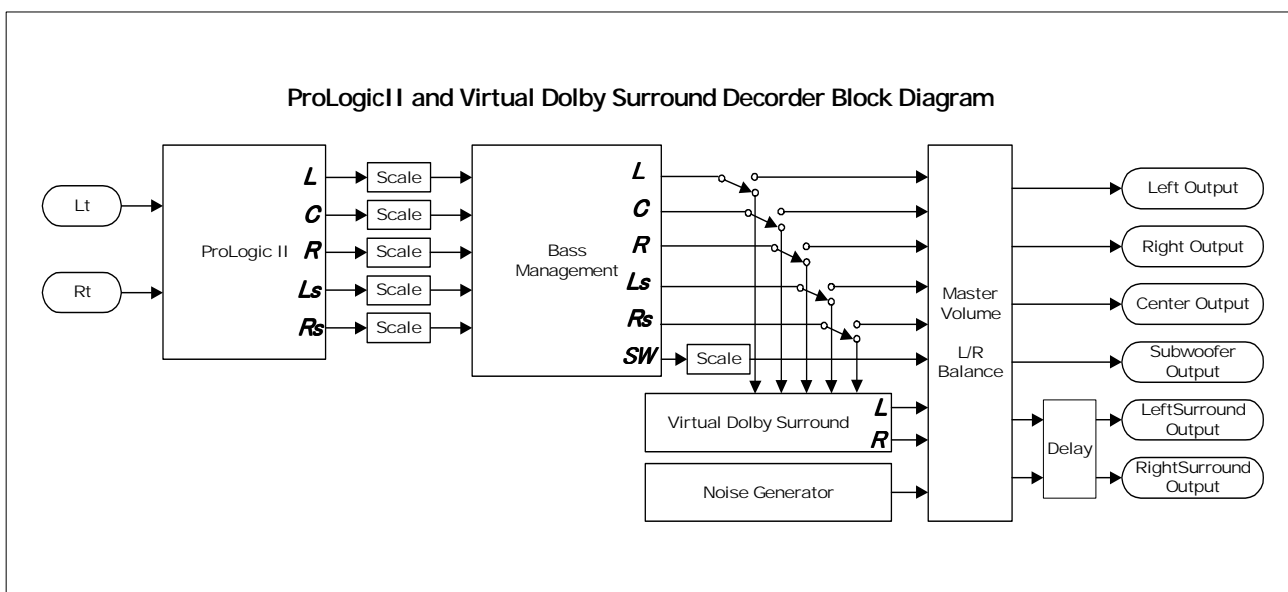
## DSP Block Diagram

Fig.1-1 NJU26106 Block Diagram

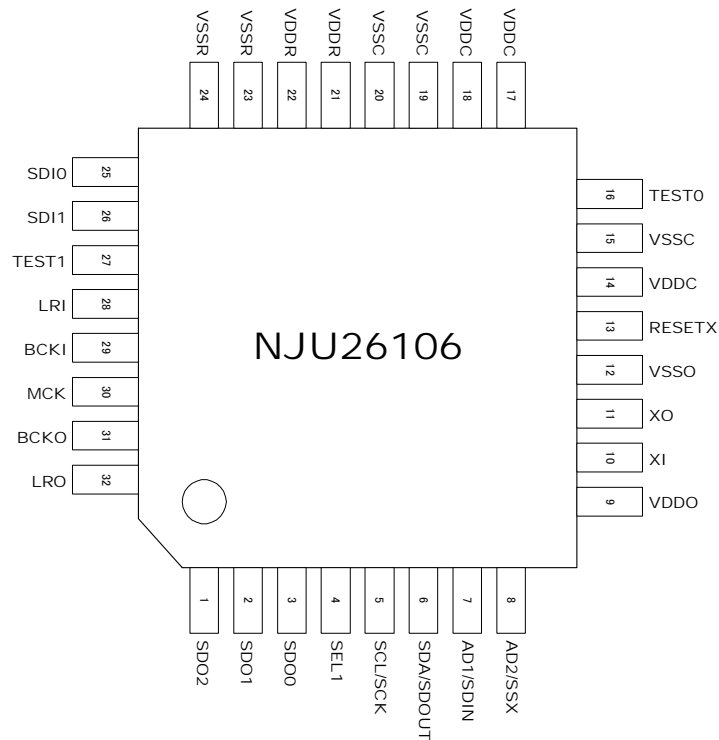


## Pro Logic II & Virtual Dolby Surround Decoder

Fig.1-2 NJU26106 Function Diagram



## Pin Configuration



## Pin Description

**Table1-1 Pin Description**

| No. | Symbol    | I/O | Description                              | No. | Symbol | I/O | Description             |
|-----|-----------|-----|--|-----|--------|-----|-------------------------|
| 1   | SDO2      | O   | Audio Data Output CH2                    | 17  | VDDC   | P   | Core Power Supply +2.5V |
| 2   | SDO1      | O   | Audio Data Output CH1                    | 18  | VDDC   | P   | Core Power Supply +2.5V |
| 3   | SDO0      | O   | Audio Data Output CH0                    | 19  | VSSC   | G   | Core GND                |
| 4   | SEL1      | I   | Select I <sup>2</sup> C or Serial bus    | 20  | VSSC   | G   | Core GND                |
| 5   | SCL/SCK   | I   | I <sup>2</sup> C Clock / Serial Clock    | 21  | VDDR   | P   | I/O Power Supply +2.5V  |
| 6   | SDA/SDOUT | IO  | I <sup>2</sup> C I/O / Serial Output     | 22  | VDDR   | P   | I/O Power Supply +2.5V  |
| 7   | AD1/SDIN  | I   | I <sup>2</sup> C Address / Serial Input  | 23  | VSSR   | G   | I/O GND                 |
| 8   | AD2/SSX   | I   | I <sup>2</sup> C Address / Serial Enable | 24  | VSSR   | G   | I/O GND                 |
| 9   | VDDO      | P   | OSC Power Supply +2.5V                   | 25  | SDI_0  | I   | Audio Data Input CH0    |
| 10  | XI        | I   | X'tal Clock Input                        | 26  | SDI_1  | I   | Audio Data Input CH1    |
| 11  | XO        | O   | X'tal Clock Output                       | 27  | TEST3  | I   | GND                     |
| 12  | VSSO      | G   | OSC GND                                  | 28  | LRI    | I   | LR Clock Input          |
| 13  | RESETX    | I   | RESET                                    | 29  | BCKI   | I   | Bit Clock Input         |
| 14  | VDDC      | P   | Core Power Supply +2.5V                  | 30  | MCK    | O   | Master Clock Output     |
| 15  | VSSC      | G   | Core GND                                 | 31  | BCKO   | O   | Bit Clock Output        |
| 16  | TEST2     | IO  | OPEN                                     | 32  | LRO    | O   | LR Clock Output         |

\* I:In, O:Out, IO:Bidir, P:+Power, G:GND

## ■ Absolute Maximum Ratings

**Table1-2 Absolute Maximum Ratings**

| Parameter                   | Symbol       | Rating    | Units |
|-----------------------------|--------------|-----------|-------|
| Supply Voltage              | $V_{DD}$     | 3.05      | V     |
| Pin No.10(Xi) Input Voltage | $V_{X(OSC)}$ | -0.3~3.05 | V     |
| Input,Output Pin Voltage    | $V_x$        | -0.3~3.6  | V     |
| Power Dissipation           | $P_D$        | 0.3       | W     |
| Operating Temperature *     | $T_{OPR}$    | -20~+75   | °C    |
| Storage Temperature         | $T_{stg}$    | -40~+125  | °C    |

\* For the car application, please ask NJR sale.

## ■ Electric Characteristics

**Table1-3 Electric Characteristics ( $V_{DD}=2.5V, T_a=25^\circ C$ )**

| Parameter                         | Symbol        | Test Condition                | Min.         | Typ. | Max.     | Units   |
|-----------------------------------|---------------|-------------------------------|--------------|------|----------|---------|
| Operating $V_{DD}$ Voltage        | $V_{DD}$      | $V_{DD}$ pins                 | 2.25         | 2.5  | 2.75     | V       |
| Operating Current                 | $I_{DD}$      | $f_{OSC}=36.864MHz$           | -            | 60   | -        | mA      |
| Recommended Operating Temperature | $T_{OPRR}$    | $V_{DD}=2.5V$                 | 0            | 25   | 70       | °C      |
| High Level Input Voltage(Xi)      | $V_{IH(OSC)}$ | No.10pin(Xi) Only             | 2.0          | -    | $V_{DD}$ | V       |
| High Level Input Voltage          | $V_{IH}$      |                               | 2.0          | -    | 3.3      | V       |
| Low Level Input Voltage           | $V_{IL}$      |                               | $V_{SS}$     | -    | 0.5      | V       |
| High Level Input Current          | $I_{IH}$      | $V_{IN}=3.3V$                 | -10          | -    | +10      | $\mu A$ |
| High Level Input Current          | $I_{IH(pd)}$  | $V_{IN}=3.3V$                 | 100          | -    | 300      | $\mu A$ |
| Low Level Input Current           | $I_{IL}$      | $V_{IN}=V_{SS}$               | -10          | -    | +10      | $\mu A$ |
| High Level Output Voltage         | $V_{OH}$      | $I_{OH}=-2mA$                 | $V_{DD}-0.4$ | -    | -        | V       |
| Low Level Output Voltage          | $V_{OL}$      | $I_{OL}=2mA$                  | -            | -    | 0.4      | V       |
| Input Capacitance                 | $C_{IN}$      |                               | -            | 5    | -        | pF      |
| Input Rise/Fall transition Time   | $t_r / t_f$   | except for No.5, 6, 7, 8pin * | -            | -    | 100      | ns      |
| Clock Frequency                   | $f_{OSC}$     | No.10pin(Xi)                  | -            | -    | 38.0     | MHz     |
| Ext.System Clock Duty Cycle       | $r_{EC}$      | No.10pin(Xi)                  | 47.5         | 50   | 52.5     | %       |

\* The  $t_r / t_f$  of these terminals is specified separately.

\* All input / input-and-output terminals serve as the Schmidt trigger input except for No.10pin(Xi).

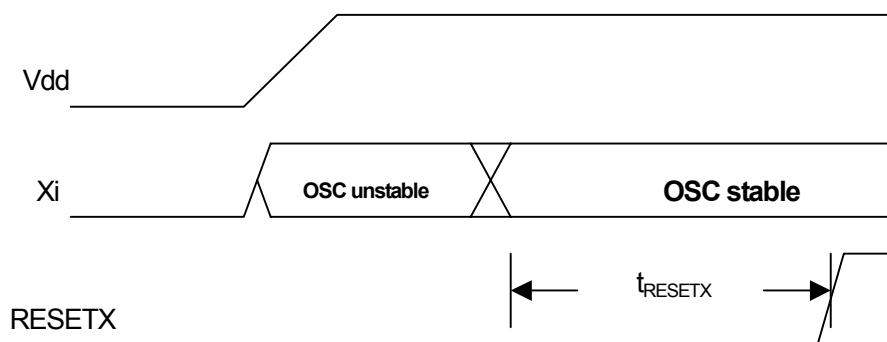
## 1. Clock and Reset

The NJU26106 Xi pin requires the system clock that should be related to the sample frequency  $f_s$ . The Xi/Xo pins can generate the system clock by connecting the crystal oscillator or the ceramic resonator. Refer to the application circuit diagram about the circuit parameters.

When the external oscillator is connected to Xi/Xo pins, check the voltage level of the pins. Because the maximum input voltage level of Xi pin is different from the other input or bi-directional pins. The maximum voltage-level of Xi pin equals to VDD.

To initialize the NJU26106, RESET pin should be set low level during some period. After some period of Low level, RESET pin should be High level. This procedure starts the initialization of the NJU26106. To finalize the initialization procedure takes 1 m sec. After 1 m sec, the NJU26106 can accept a command from Host controller. The detail status of the initialized NJU26106 is referred to the each command that describes the initial status.

To select I<sup>2</sup>C bus or 4-Wire serial bus, some level should be supplied to SEL1 pin. When SEL1="L", I<sup>2</sup>C bus is selected. When SEL1="H", 4-Wire serial bus is selected. The level of SEL1 is checked by the NJU26106 in 1 m sec after RESET-pin level goes to "H". After the power supply and the oscillation of the NJU26106 becomes stable, RESET pin should be kept Low-level at least  $t_{RESETX}$  period.



**Fig. 1-3 Reset Timing**

**Table 1-4 Reset Time**

| Symbol       | Time          |
|--------------|---------------|
| $t_{RESETX}$ | $\geq 1\mu s$ |

## 2 System Clock

Audio data samples must be transferred in synchronism between all components of the digital audio system. That is, for each audio sample originated by an audio source there must be one and only one audio sample processed by the NJU26106 and delivered to the D/A converters. To accomplish this, one device in the system is selected to generate the audio sample rate; the remaining devices are designated to follow this sample rate. The device that generates the audio sample rate is called the MASTER device; all devices following this sample rate are called SLAVE(s)

LR, BCK and MCK should be synchronized. This is described in next section 2.1. When the NJU26106 is in MASTER mode, the NJU26106 system clock should be 768 multiples of the sampling frequency (Table2-1). When the NJU26106 is in SLAVE mode, NJU26106 system clock should be from 768 multiples of the sampling frequency to the maximum operating frequency.

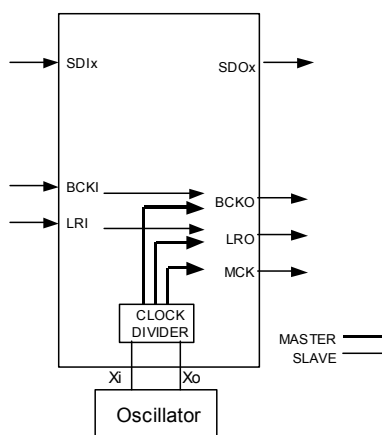
### 2.1 Audio Clock

Three types of clock signals are included in the serial audio interface. Two of the clock signals LR (LRI and LRO) and BCK (BCKI and BCKO) establish data transfer on the serial data lines. The third clock, MCK, is not associated with serial data transfer but is required by delta-sigma A/D and D/A converters.

The frequency of the LR clock is, by definition, equal to the digital audio sample rate,  $F_s$ . BCK and MCK operate at multiples of the LR clock rate. Therefore the signals LR, BCK and MCK must be locked, that is, they must be generated or derived from a single frequency reference. In SLAVE mode, the NJU26106 dose not generate MCK clock.

**Table2-1 Sampling Frequency and BCK, MCK, Xi**

| Clock Signal | Multiple Frequency | 32Khz     | 44.1kHz    | 48kHz     |
|--------------|--------------------|-----------|------------|-----------|
| LR           | 1Fs                | 32kHz     | 44.1kHz    | 48kHz     |
| BCK(32fs)    | 32Fs               | 1.024MHz  | 1.4112MHz  | 1.536MHz  |
| BCK(64fs)    | 64Fs               | 2.048MHz  | 2.822MHz   | 3.072MHz  |
| MCK(256fs)   | 256Fs              | 8.192MHz  | 11.289MHz  | 12.288MHz |
| MCK(384fs)   | 384Fs              | 12.288MHz | 16.934MHz  | 18.432MHz |
| Xi           | 768Fs              | 24.576MHz | 33.8688MHz | 36.864MHz |



**Fig. 2-1 MASTER / SLAVE Mode**

### 3. Audio Interface

The serial audio interface carries audio data to and from the NJU26106. Industry standard serial data formats of I<sup>2</sup>S, MSB-first left-justified or MSB-first right-justified are supported. These serial audio formats define a pair of digital audio signals (stereo audio) on each data line. Two clock lines, BCK (bit clock) and LR (left/right word clock) establish timing for serial data transfers.

The NJU26106 serial audio interface includes two data input lines; SDI0 and SDI1 and three data output lines, SDO1, SDO2, SDO3 as shown in the figure below. The input serial data is selected by the firmware command.

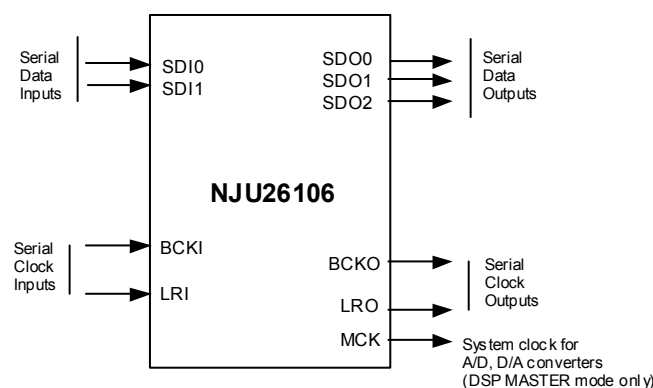
**Table 3-1 Serial Audio Output Pin Description**

| Symbol | Pin No. | Description              |
|--------|---------|--------------------------|
| SDO0   | 3       | Front Lch/Rch Output(*)  |
| SDO1   | 2       | Center/Sub Woofer Output |
| SDO2   | 1       | Rear Lch/Rch Output      |

(\*) In Virtual Dolby Surround mode, only front Lch/Rch output signal. The other channels are muted.

The NJU26106 has a pair of left/right clock lines (LRI and LRO) and a pair of bit clock lines (BCKI and BCKO). Clock inputs BCKI and LRI are used to accept timing signals from an external device when the NJU26106 is operating in SLAVE clock mode.

The BCKO,LRO and system clock output MCK, is provided for delta-sigma A/D and D/A converters when the NJU26106 operates in MASTER mode. In SLAVE mode, the output of BCKO and LRO are the buffered output of BCKI and LRI. The output of MCK is fixed to low level in SLAVE mode.



**Fig. 3-1 Serial Audio Interface**

## 3.1 Audio Data Format

The NJU26106 can exchange data using any of three industry-standard digital audio data formats: I<sup>2</sup>S, MSB-first Left-justified, or MSB-first Right-justified.

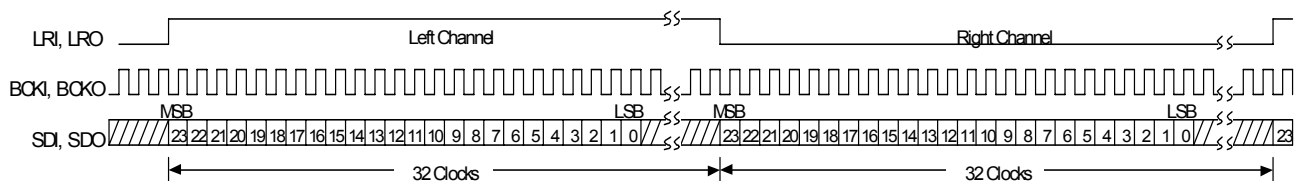
The three serial formats differ primarily in the placement of the audio data word relative to the LR clock. Left-justified format places the most-significant data bit (MSB) as the first bit after an LR transition. I<sup>2</sup>S format places the most-significant data bit (MSB) as the second bit after an LR transition (one bit delay relative to left-justified format). Right-justified format places the least-significant data bit (LSB) as the last bit before an LR transition.

Clock LR (LRI, LRO) marks data word boundaries and clock BCK (BCKI, BCKO) clocks the transfer of serial data bits. One period of LR defines a complete stereo audio sample and thus the rate of LR equals the audio sample rate (Fs). All formats transmit the stereo sample left channel first. Note that polarity of LR is opposite in I<sup>2</sup>S format (LR:LOW = Left channel data) compared to Left-Justified or Right-Justified formats.

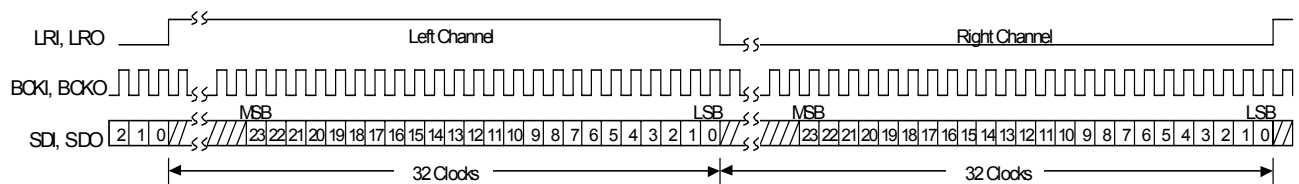
The number of BCK clock must follow the serial data format. If the BCK clock is not enough, the right sound are not produced. Set serial data format for the adequate mode that A/Ds, D/As or Codecs require.

The NJU26106 supports serial data format which includes 32(32fs) or 64(64fs) BCK clocks. This serial data format is applied to both MASTER and SLAVE mode.

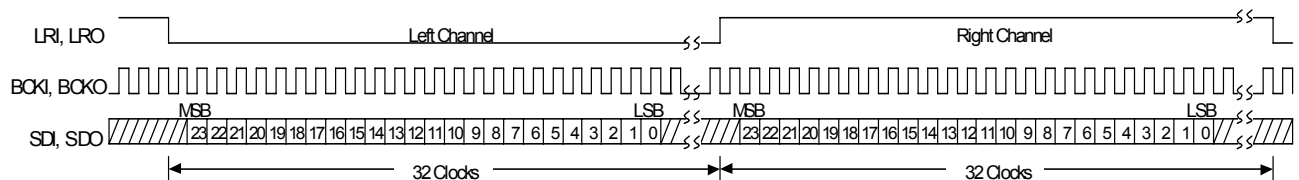
## 3.2 Serial Audio Data Transmitting Diagram



**Fig. 3-2 Left-Justified Data Format 64Fs, 24bit Data**

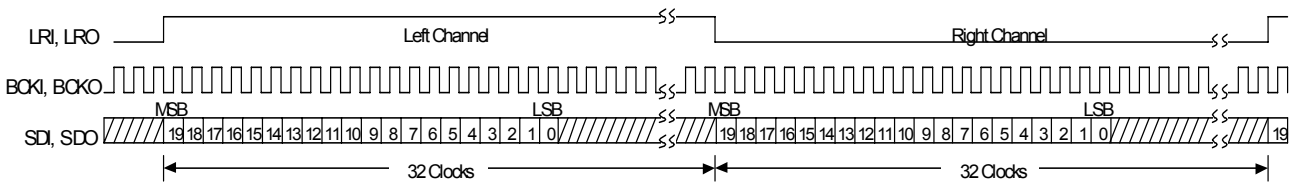


**Fig. 3-3 Right-Justified Data Format 64Fs, 24bit Data**

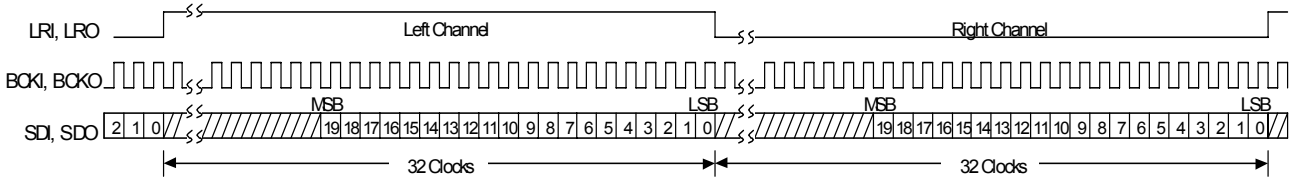


**Fig. 3-4 I<sup>2</sup>S Data Format 64Fs, 24bit Data**

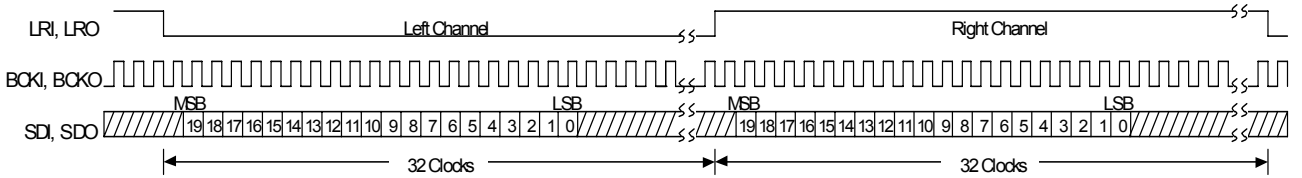




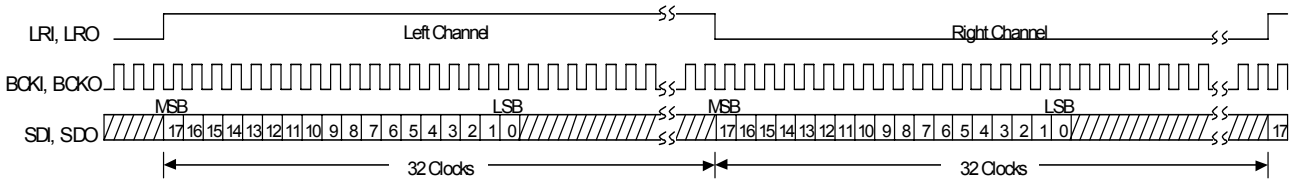
**Fig. 3-5 Left-Justified Data Format 64Fs, 20bit Data**



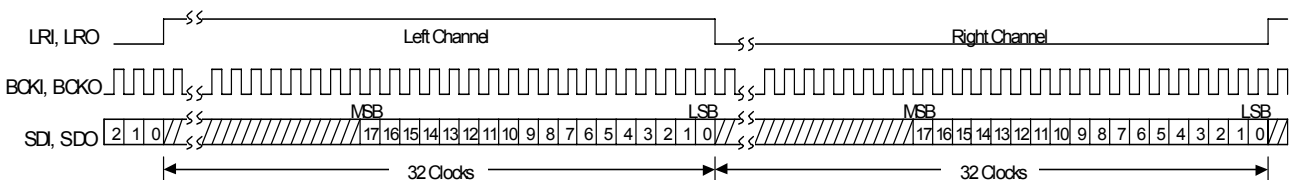
**Fig. 3-6 Right-Justified Data Format 64Fs, 20bit Data**



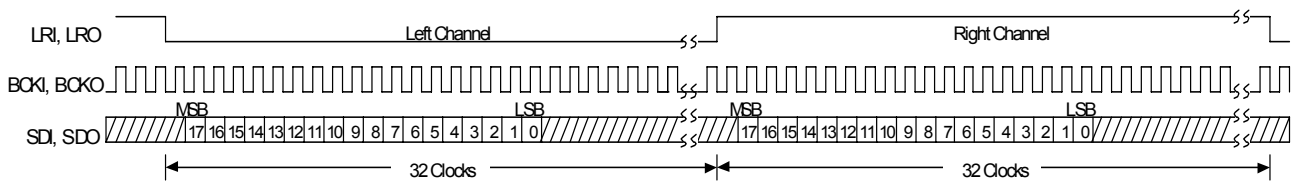
**Fig. 3-7 I²S Data Format 64Fs, 20bit Data**



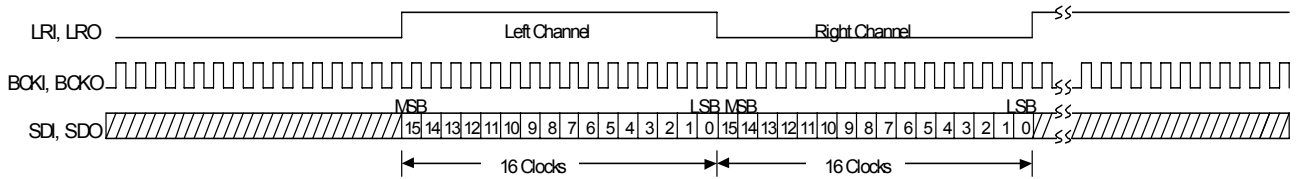
**Fig. 3-8 Left-Justified Data Format 64Fs, 18bit Data**



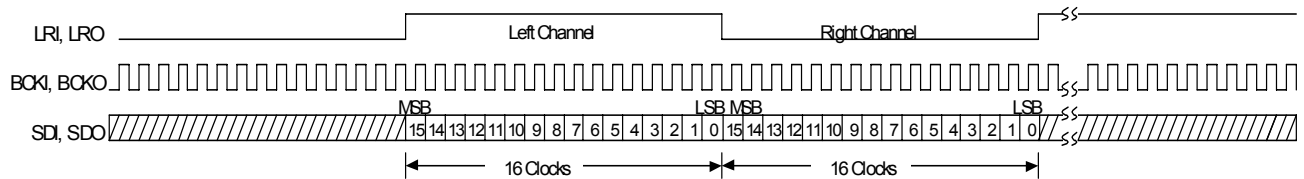
**Fig. 3-9 Right-Justified Data Format 64Fs, 18bit Data**



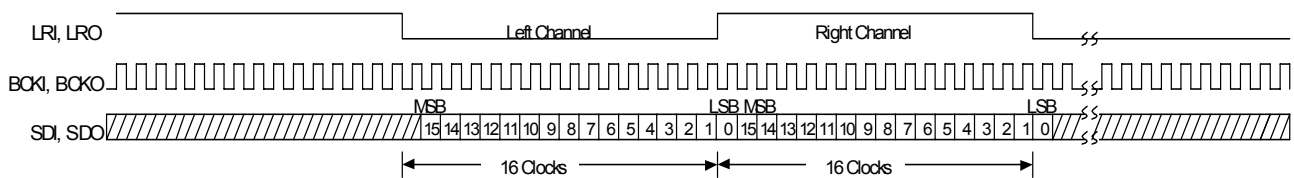
**Fig. 3-10 I²S Data Format 64Fs, 18bit Data**



**Fig. 3-11 Left-Justified Data Format 32Fs, 16bit Data**



**Fig. 3-12 Right-Justified Data Format 32Fs, 16bit Data**



**Fig. 3-13 I²S Data Format 32Fs, 16bit Data**

3.3 Serial Audio Timing

Table 3-2 Serial Audio Input Timing Parameters

| Parameter        | Symbol    | Test Condition | Min | Typ. | Max | Units |
|------------------|-----------|----------------|-----|------|-----|-------|
| BCKI Frequency   |           |                | 0.9 | -    | 4.0 | MHz   |
| BCKI Period      |           |                |     |      |     |       |
| L Pulse Width    | $t_{SIL}$ |                | 85  | -    | -   | ns    |
| H Pulse Width    | $t_{SIH}$ |                | 85  | -    | -   | ns    |
| BCKI to LRI Time | $T_{SLI}$ |                | 40  | -    | -   | ns    |
| LRI to BCKI Time | $t_{LSI}$ |                | 40  | -    | -   | ns    |
| Data Setup Time  | $t_{DS}$  |                | 40  | -    | -   | ns    |
| Data Hold Time   | $t_{DH}$  |                | 40  | -    | -   | ns    |

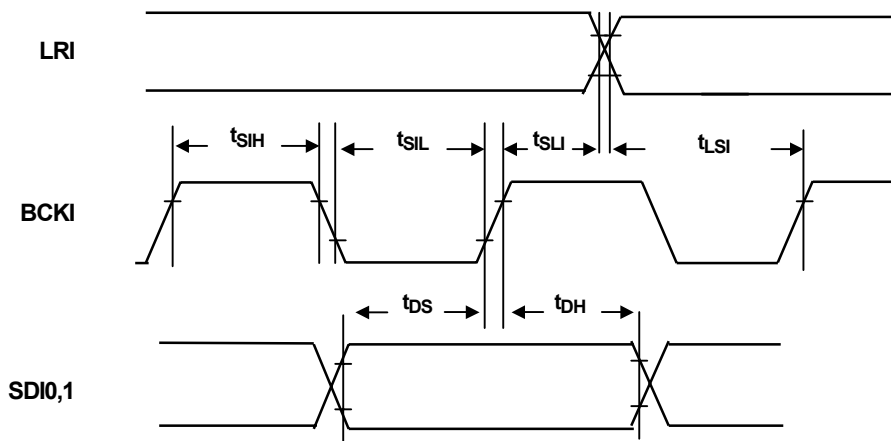
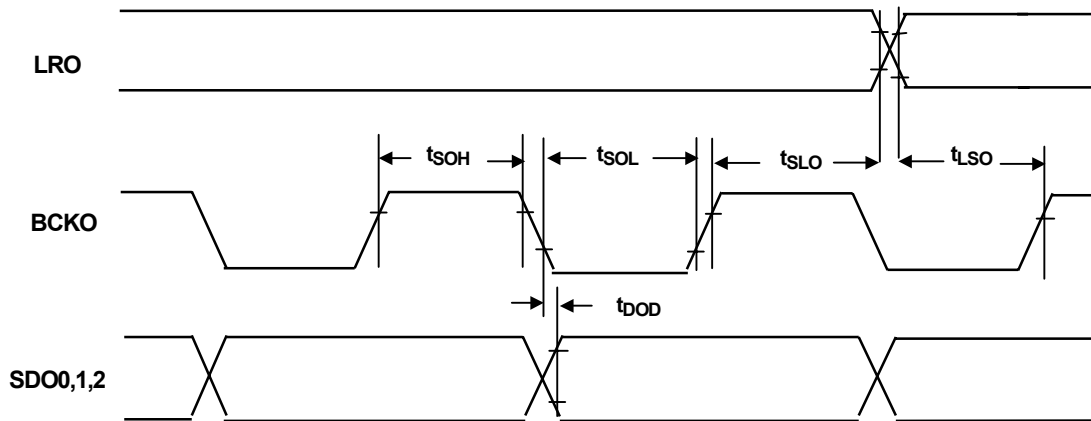


Fig. 3-14 Serial Audio Input Timing

**Table 3-3 Serial Audio Output Timing Parameters**

| Parameter                                     | Symbol                 | Test Condition                | Min                          | Typ. | Max                          | Units |
|---|------------------------|-------------------------------|------------------------------|------|------------------------------|-------|
| BCKO Period<br>L Pulse Width<br>H Pulse Width | $t_{SOL}$<br>$t_{SOH}$ | $C_L$ :LRO, BCKO,<br>SDO=25pF | $t_{SIL-40}$<br>$t_{SIH-40}$ | -    | $t_{SIL+40}$<br>$t_{SIH+40}$ | ns    |
| BCKO to LRO Time                              | $t_{SLO}$              |                               | 20                           | -    | -                            | ns    |
| LRO to BCKO Time                              | $t_{LSO}$              |                               | 20                           | -    | -                            | ns    |
| Data Output Delay                             | $t_{DOD}$              |                               | -                            | -    | 20                           | ns    |



**Fig. 3-15 Serial Audio Output Timing**

## 4. Host Interface

The NJU26106 can be controlled via Serial Host Interface (SHI) using either of two serial bus format : 4-Wire serial bus or I<sup>2</sup>C bus. Data transfers are in 8 bit packets (1 byte) when using either format. The SHI operates only in a SLAVE fashion. A host controller connected to the interface always drives the clock (SCL / SCK) line and initiates data transfers, regardless of the chosen communication protocol.

The SEL1 pin controls the serial bus mode. When the SEL1 is low during the NJU26106 initialization, 4-Wire serial bus is available. When the SEL1 is high during the NJU26106 initialization, I<sup>2</sup>C bus is available.

**Table 4-1 Serial Host Interface Pin Description**

| Symbol<br>(I <sup>2</sup> C / Serial) | Pin No. | 4-Wire Serial bus Format | I <sup>2</sup> C bus Format       |
|---------------------------------------|---------|--------------------------|-----------------------------------|
| SCL/SCK                               | 5       | Serial Clock             | Serial Clock                      |
| SDA/SDOUT                             | 6       | Serial Data Output       | Serial Data<br>(Bi-directional)   |
| AD1/SDIN                              | 7       | Serial Data Input        | I <sup>2</sup> C bus address Bit1 |
| AD2/SSx                               | 8       | SLAVE Select             | I <sup>2</sup> C bus address Bit2 |

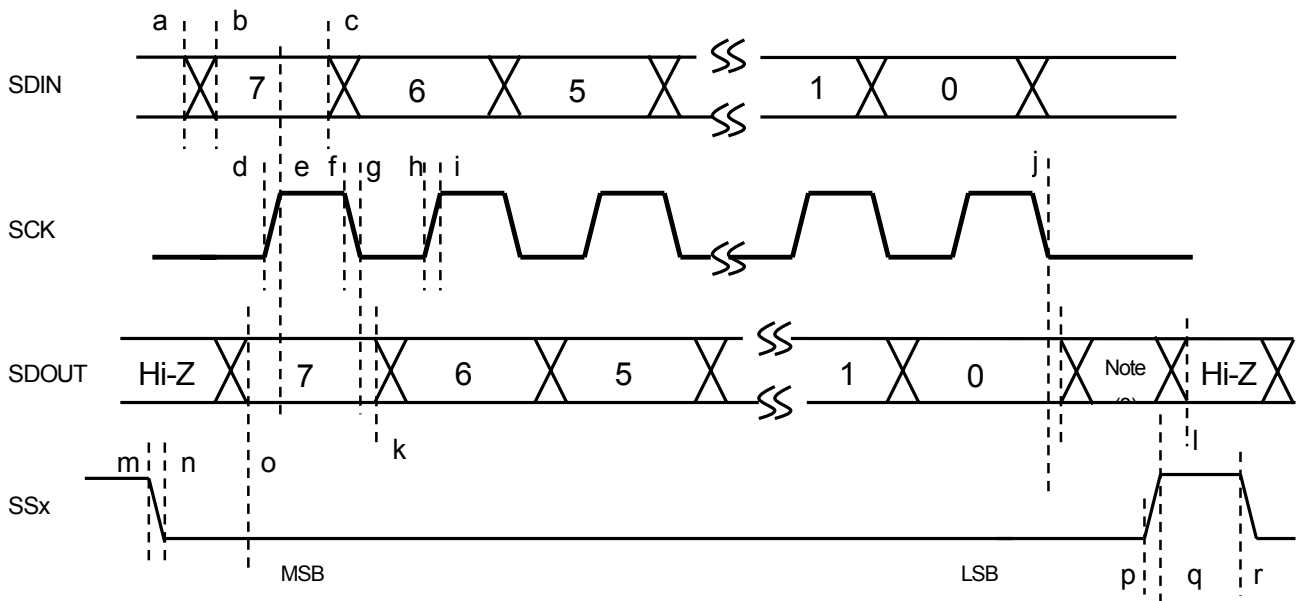
Note : SDA /SDOUT pin is a bi-directional open drain. When 4-Wire Serial bus is selected, and SSX is effective, and a CMOS output and SSX are invalid, it will be in a Hi-Z state. This pin, which is assigned for 4-Wire serial bus format or for I<sup>2</sup>C, requires a 4.7k pull-up resistor.

### 4.1 4-Wire Serial Interface

The serial host interface can be configured for 4-Wire Serial bus communication by setting SEL1="H" during the Reset Sequence initialization. SHI bus communication is full-duplex; a write byte is shifted into the SDIN pin at the same time that a read byte is shifted out of the SDOUT pin. Data transfers are MSB first and are enabled by setting the Slave Select pin LOW (SSX = 0). Data is clocked into SDIN on rising transitions of SCK. Data is latched at SDOUT on falling transitions of SCK except for the first byte (MSB) which is latched on the falling transitions of SSX. SDOUT is Hi-Z in case of SSX = "H". SDOUT is CMOS output in case of SSX = "L". SDOUT needs a pull-up resistor when SDOUT is Hi-Z.

**Table 4-2 4-Wire Serial Interface Timing Parameters**

| Parameter                        | Symbol      | Timelines            | Min. | Typ. | Max. | Units   |
|----------------------------------|-------------|----------------------|------|------|------|---------|
| Input Data Rising Time           | $t_{MSDr}$  | a-b                  | -    | -    | 100  | ns      |
| Input Data Falling Time          | $t_{MSDf}$  | a-b                  | -    | -    | 100  | ns      |
| Serial Clock Rising Time         | $t_{MSCr}$  | d-e                  | -    | -    | 100  | ns      |
| Serial Clock Falling Time        | $t_{MSCf}$  | f-g                  | -    | -    | 100  | ns      |
| Serial Strobe Rising Time        | $t_{MSSr}$  | p-q                  | -    | -    | 100  | ns      |
| Serial Strobe Falling Time       | $t_{MSSf}$  | m-n                  | -    | -    | 100  | ns      |
| Serial Clock H Duration          | $t_{MSCa}$  | e-f                  | 50   | -    | -    | ns      |
| Serial Clock L Duration          | $t_{MSCn}$  | g-h                  | 50   | -    | -    | ns      |
| Serial Clock Period              | $t_{MSCc}$  | e-i                  | 250  | -    | -    | ns      |
| Serial Strobe Setup Time         | $t_{MSSs}$  | n-e                  | 100  | -    | -    | ns      |
| Serial Strobe Hold Time          | $t_{MSSH}$  | j-q                  | 30   | -    | -    | ns      |
| Serial Strobe L Duration         | $t_{MSSa}$  | n-p                  | -    | 1.0  | -    | $\mu$ s |
| Serial Strobe H Duration         | $t_{MSSn}$  | q-r                  | 40   | -    | -    | ns      |
| Input Data Setup Time            | $t_{MSDis}$ | b-e                  | 20   | -    | -    | ns      |
| Input Data Hold Time             | $t_{MSDih}$ | e-c                  | 20   | -    | -    | ns      |
| Output Data Delay (From SSx)     | $t_{MSDos}$ | n-o, CL=25pF         | -    | -    | 50   | ns      |
| Output Data Delay (From SCLK)    | $t_{MSDo}$  | g-k(data-6), CL=25pF | -    | -    | 50   | ns      |
| Output Data Hold Time            | $t_{MSDoh}$ | g-k(data-7)          | 0    | -    | -    | ns      |
| Output Data Turn off Time (Hi-Z) | $t_{MSDov}$ | q-l                  | -    | -    | 40   | ns      |



**Fig. 4-1 4-Wire Serial Interface Timing**

- Note :
- \*1 When the data-clock is less than 8 clocks, the input data is shifted to LSB side and is sent to the DSP core at the transition of SSX="H".
  - \*2 When the data-clock is more than 8 clocks, the last 8 bit data becomes valid.
  - \*3 After sending LSB data, SDOUT transmits the MSB data which is received via SDIN until SSX becomes "H".
  - \*4 SDOUT is Hi-Z in case of SSX = "H". SDOUT is CMOS output in case of SSX = "L". SDOUT needs a pull-up resistor to prevent SDOUT from becoming floating level.

## 4.2 I<sup>2</sup>C Bus

When the NJU26106 is configured for I<sup>2</sup>C bus communication in SEL1="L", the serial host interface transfers data on the SDA pin and clocks data on the SCL pin. SDA is an open drain pin requiring an external 4.7k pull-up resistor. Pins AD1 and AD2 are used to configure the seven-bit SLAVE address of the serial host interface. This offers additional flexibility in a system design by offering two different possible SLAVE addresses for which the NJU26106 will respond to. An address can be arbitrarily set up with an internal setup and this AD1 terminal. In the NJU26106, AD2 pin should be connected to "H". Any I<sup>2</sup>C address could be chosen for AD1. The I<sup>2</sup>C address of AD1 is decided by connection of AD1-pin. The I<sup>2</sup>C address should be the same level of AD1-pin

**Table 4-3 I<sup>2</sup>C Bus SLAVE Address**

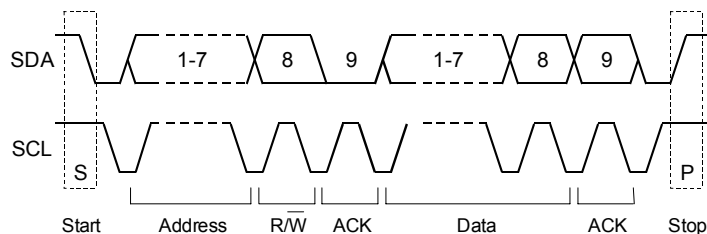
| bit7 | bit6 | bit5 | bit4 | Bit3 | bit2              | bit1              | bit0 |
|------|------|------|------|------|-------------------|-------------------|------|
| 0    | 0    | 1    | 1    | 1    | AD2* <sup>1</sup> | AD1* <sup>2</sup> | R/W  |

\*1 AD2 pin should be connected to high. The I<sup>2</sup>C address of AD2 should be 1.

\*2 SLAVE address is 0 when AD1 is L. SLAVE address is 1 when AD1 is H.

The figure on the following page shows the basic timing relationships for transfers. A transfer is initiated with a START condition, followed by the SLAVE address byte. The SLAVE address consists of the seven-bit SLAVE address followed by a read/write (R/W) bit. When an address with an effective serial host interface is detected, the acknowledgement bit which sets a SDA line to LOW in the ninth bit clock cycle is returned.

The R/W bit in the SLAVE address byte sets the direction of data transmission until a STOP condition terminates the transfer. R/W = 0 indicates the host will send to the NJU26106 while R/W = 1 indicates the host will receive data from the NJU26106.



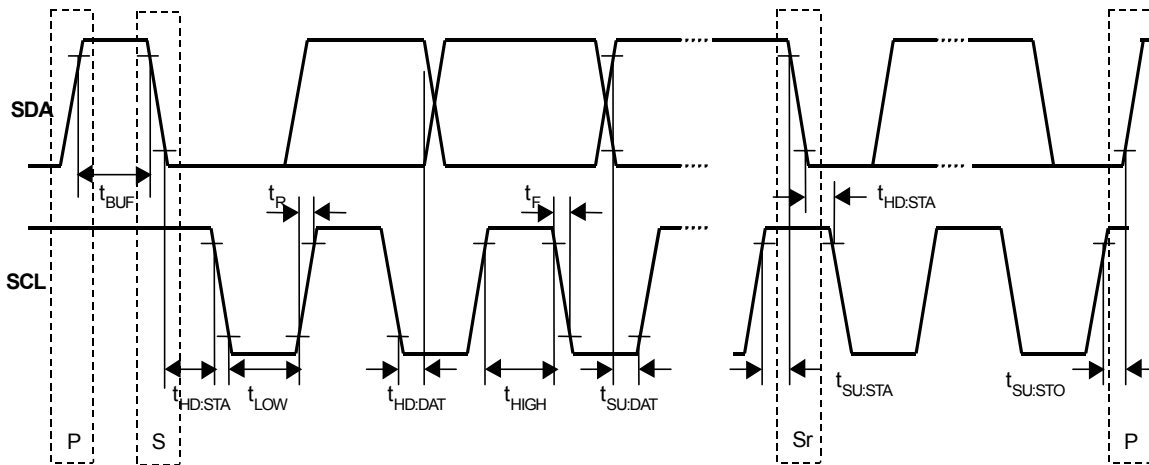
**Fig. 4-2 I<sup>2</sup>C Bus Format**

In case of the NJU26106, only single-byte transmission is available.

The serial host interface supports "Standard-Mode (100kbps)" I<sup>2</sup>C bus data transfer.

**Table 4-4 I<sup>2</sup>C Bus Interface Timing Parameters**

| Parameter                  | Symbol       | Standard Mode |      | Units   |
|----------------------------|--------------|---------------|------|---------|
|                            |              | Min           | Max  |         |
| SCL Clock Frequency        | $f_{SCL}$    | 0             | 100  | kHz     |
| Start Condition Hold Time  | $t_{HD:STA}$ | 4.0           | -    | $\mu$ s |
| SCL "L" Duration           | $t_{LOW}$    | 4.7           | -    | $\mu$ s |
| SCL "H" Duration           | $t_{HIGH}$   | 4.0           | -    | $\mu$ s |
| Start Condition Setup Time | $t_{SU:STA}$ | 4.7           | -    | $\mu$ s |
| Data Hole Time             | $t_{HD:DAT}$ | 0             | 3.45 | $\mu$ s |
| Data Setup Time            | $t_{SU:DAT}$ | 250           | -    | ns      |
| Rising Time                | $t_R$        | -             | 1000 | ns      |
| Falling Time               | $t_F$        | -             | 300  | ns      |
| Stop Condition Setup Time  | $t_{SU:STO}$ | 4.0           | -    | $\mu$ s |
| Bus Release Time           | $t_{BUF}$    | 4.7           | -    | $\mu$ s |



**Fig. 4-3 I<sup>2</sup>C Bus Timing**



## 5. Firmware Command Table

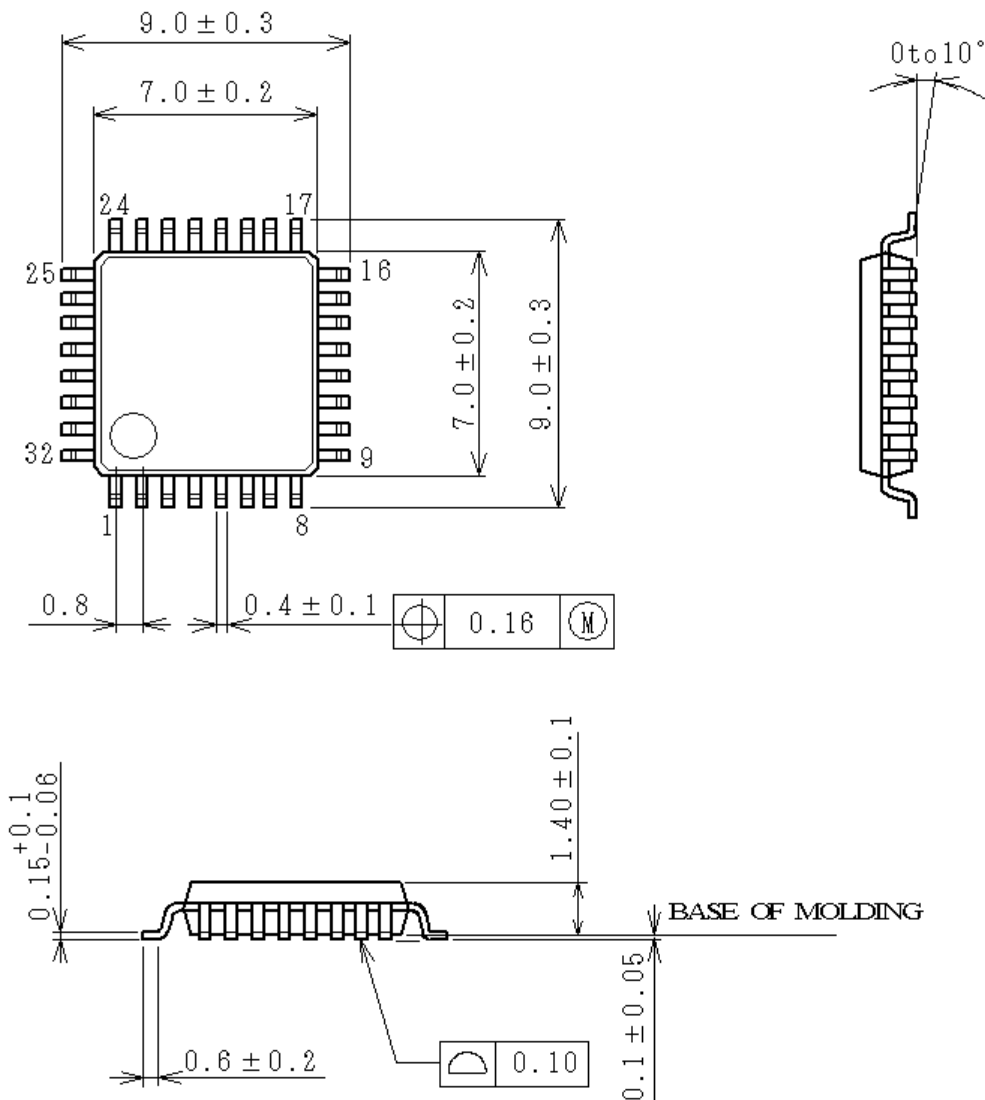
The NJU26106 allows for user configuration of the decoder with micro controller commands entered via Host interface (I<sup>2</sup>C bus or serial interface). The following table summarizes the available user commands.

**Table5-1 NJU26106 Command**

| No. | Command System     | Command Description  |
|-----|--------------------|--|
| 1   | SET_TASK_CMD       | Set decoding mode: Pro Logic II, Virtual Dolby Surround, Pink Noise Generator                      |
| 2   | VDS_ANG_CMD        | Set Virtual Dolby Surround Speaker separation angle  |
| 3   | DPL_SUR_CMD        | Set Pro Logic II Decode Mode (Movie,Music,etc) and Panorama mode                                   |
| 4   | CWIDTH_DIM_CMD     | Set Pro Logic II Center Width and Dimension configuration  |
| 5   | DPL_MOD_CMD        | Set Pro Logic II Variable Setting, Auto input Balance and Shelf Filter, Rs Polarity Inversion, etc |
| 6   | BASS_MGNT_CMD      | Set Bass Management Configuration, LFE Cutoff Frequency Configuration                              |
| 7   | FS_CMD             | Set sampling rate  |
| 8   | NOISE_CMD          | Set Output Speaker Configuration for Pink Noise Generator  |
| 9   | DLY_CMD            | Set Surround Channel Delay Time  |
| 10  | LR_BAL_CMD         | Set L/R Volume Balance   |
| 11  | MST_VOL_CMD        | Set MASTER Volume  |
| 12  | LCH_VOL_CMD        | Set L Channel Volume   |
| 13  | RCH_VOL_CMD        | Set R Channel Volume   |
| 14  | CENT_VOL_CMD       | Set Center Channel Volume  |
| 15  | SURR_LEFT_VOL_CMD  | Set Surround Left Channel Volume   |
| 16  | SURR_RIGHT_VOL_CMD | Set Surround Right Channel Volume  |
| 17  | SW_VOL_CMD         | Set Subwoofer Channel Volume   |
| 18  | SYS_SET_CMD        | Configure serial audio interface format, LR & BCK MASTER/SLAVE, etc.                               |

# NJU26106

## ■ Package Dimensions (EIAJ : QFP032-P-0707-1)



UNIT : mm

LEADS MATERIAL : 42ALLOY

LEADS FINISH : SOLDER PLATING

MOLD MATERIAL : EPOXY RESIN

Ver. 2.1

**[CAUTION]**

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