19-6338; Rev 0; 5/12

MAX14840PMB1 Peripheral Module

General Description

The MAX14840PMB1 peripheral module provides the necessary hardware to interface the MAX14840E RS-485 transceiver to any system that utilizes Pmod™-compatible expansion ports configurable for a UART interface. The IC is a +3.3V ESD-protected transceiver intended for half-duplex RS-485 communication up to 40Mbps*. These transceivers are optimized for high speeds over extended cable runs, while maximizing tolerance to noise.

The IC features symmetrical fail-safe and larger receiver hysteresis, providing improved noise rejection and improved recovered signals in high-speed and long-cable applications.

**The maximum communication speed of this module is generally less than 10Mbps due to the presence of current-limiting resistors on the data lines of this module and possibly also the host board.*

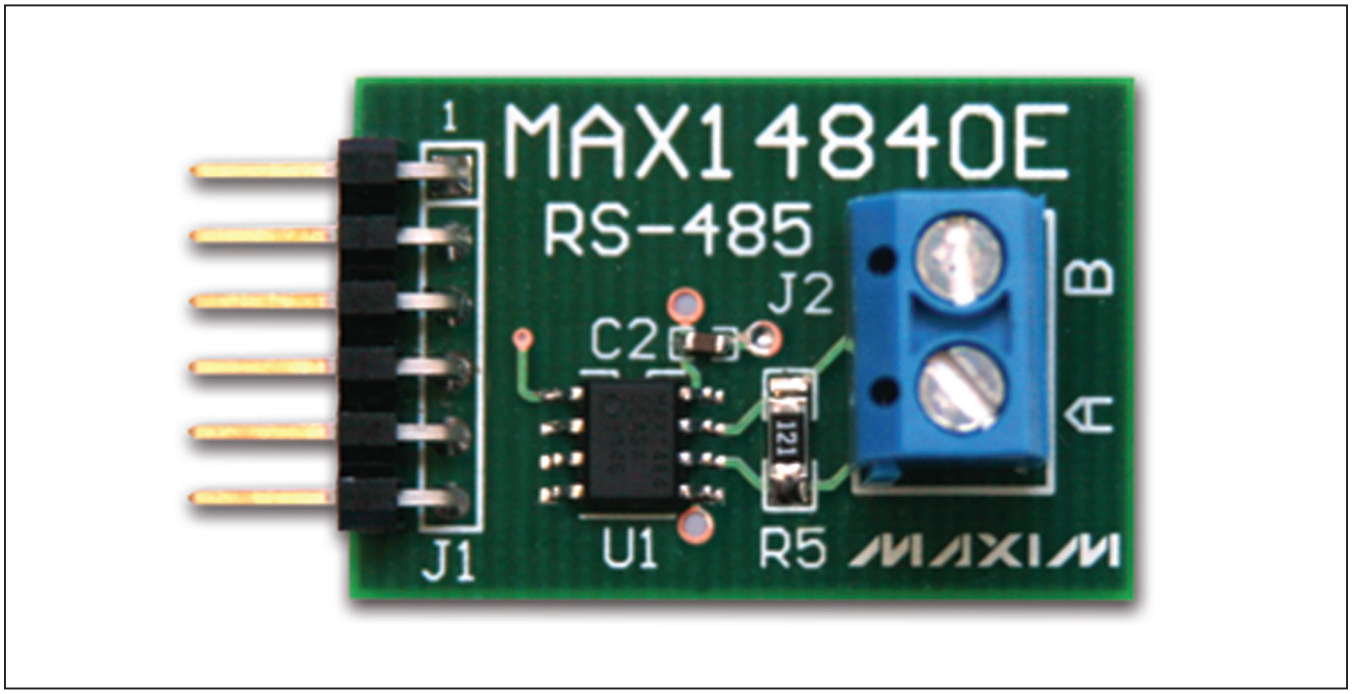
Refer to the MAX14840E IC data sheet for detailed information regarding operation of the IC.

Features

- **Half-Duplex RS-485 Transceivers**
- **40Mbps Maximum Data Rate**
- **Large (170mV) Receiver Hysteresis**
- **Symmetrical Fail-Safe Receiver Input**
- **Hot-Swap Capability**
- **Short-Circuit-Protected Outputs**
- **Thermal Self-Protection**
- **Extended ESD Protection for RS-485 I/O Pins**
- **6-Pin Pmod-Compatible Connector (Pmod Interface Type 4 UART)**
- **Example Software Written in C for Portability**
- **RoHS Compliant**
- **Proven PCB Layout**
- **Fully Assembled and Tested**

***Ordering Information** appears at end of data sheet.*

MAX14840PMB1 Peripheral Module



Pmod is a trademark of Digilent Inc.

Component List

DESIGNATION	QTY	DESCRIPTION
C1	1	1µF ±10%, 10V X7R ceramic capacitor (0603) TDK C1608X7R1A105K
C2	1	0.1µF ±10%, 16V X7R ceramic capacitor (0603) Murata GRM188R71C104KA01D
J1	1	6-pin right-angle male header
J2	1	2-position terminal block On-Shore Technology ED500/2DS

DESIGNATION	QTY	DESCRIPTION
JP1	1	2-pin straight male header
R1–R4	4	150Ω ±5% resistors (0603)
R5	1	120Ω ±5% resistor (1206)
U1	1	40Mbps, +3.3V, RS-485 half-duplex transceiver (8 SO) Maxim MAX14840EASA+
—	1	Shorting jumper
—	1	PCB: EPCB14840EPM1

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
On-Shore Technology, Inc.	480-921-3000	www.on-shore.com
TDK Corp.	847-803-6100	www.component.tdk.com

Note: *Indicate that you are using the MAX14840PMB1 when contacting these component suppliers.*

Detailed Description

UART Interface

The MAX14840PMB1 peripheral module can interface to the host by plugging directly into a Pmod-compatible port (configured for UART) through connector J1.

Connector J1 provides connection of the module to the Pmod host through an interface **similar** to the Pmod UART Type 4 standard recommended by Digilent. The transmit driver and receive pin assignment are the same as the standard. However, the CTS and RTS signals are replaced by half-duplex driver- and receiver-enable signals. See Table 1.

Connector J2 provides the RS-485 positive and negative signal pair. See Table 2.

Table 1. Connector J1 (UART Communication)

PIN	SIGNAL	DESCRIPTION
1	$\overline{RE}$	Receiver-enable input. This active-low pin enables the half-duplex receiver.
2	DI	Driver input. This pin carries the transmit data from the Pmod system's UART transmitter to a connected receiver.
3	RO	Receiver output. This pin carries the half-duplex receive data to the Pmod system's UART receiver.
4	DE	Driver-output-enable input. This active-high pin enables the half-duplex transmitter.
5	GND	Ground
6	VCC	Power supply

Table 2. Connector J2

PIN	SIGNAL	DESCRIPTION
1	RS485-A	Noninverting RS-485 signal
2	RS485-B	Inverting RS-485 signal

Connector JP1 (Termination Select)

This jumper port optionally inserts a 120Ω termination resistor across the transmit-positive and negative nets. The JP1 jumper should be installed at the endpoints of the RS-485 network, and not at the midpoints.

Software and FPGA Code

Example software and drivers are available that execute directly without modification on several FPGA development boards that support an integrated or synthesized microprocessor. These boards include the Digilent Nexys 3, Avnet LX9, and Avnet ZEDBoard, although other platforms can be added over time. Maxim provides complete Xilinx ISE projects containing HDL, Platform Studio, and SDK projects. In addition, a synthesized bit stream, ready for FPGA download, is provided for the demonstration application.

The software project (for the SDK) contains several source files intended to accelerate customer evaluation and design. These include a base application (maximModules.c) that demonstrates module functionality, and which uses an API interface (maximDeviceSpecific Utilities.c) to set and access Maxim device functions within a specific module.

The source code is written in standard ANSI C format, and all API documentation including theory/operation, register description, and function prototypes are documented in the API interface file (maximDeviceSpecificUtilities.h & .c).

The complete software kit is available for download at **www.maxim-ic.com**. Quick start instructions are also available as a separate document.

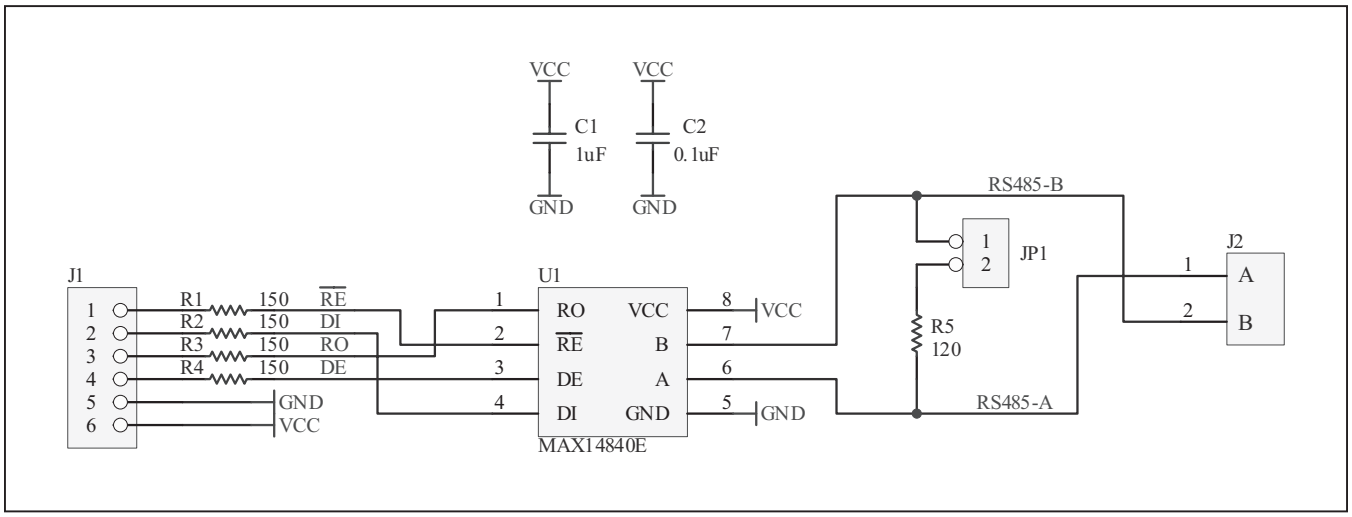


Figure 1. MAX14840PMB1 Peripheral Module Schematic

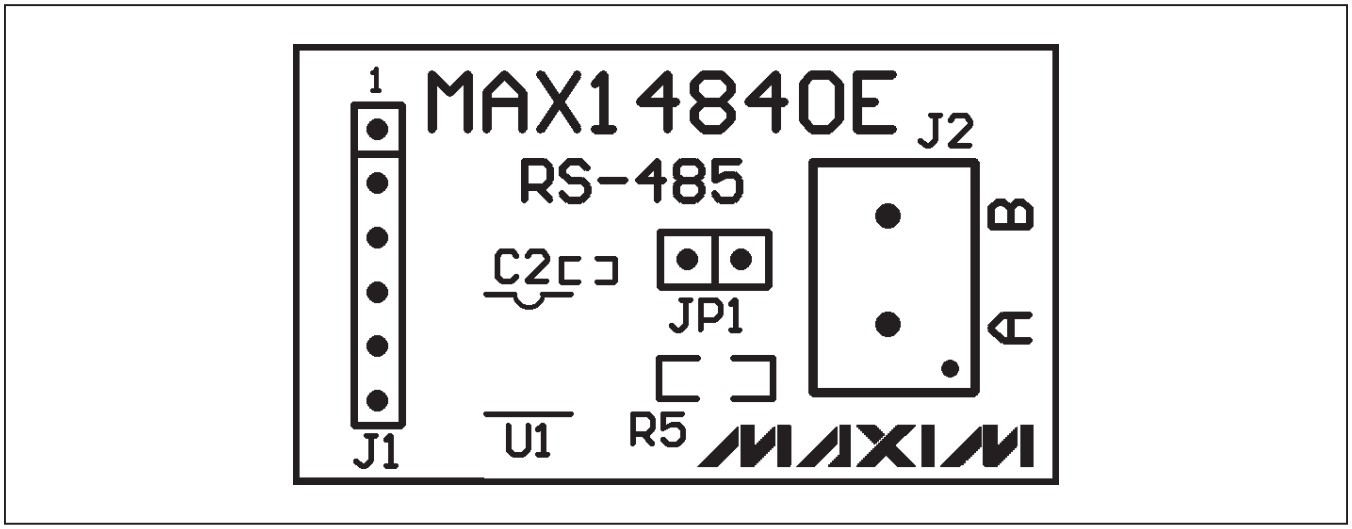


Figure 2. MAX14840PMB1 Peripheral Module Component Placement Guide—Component Side

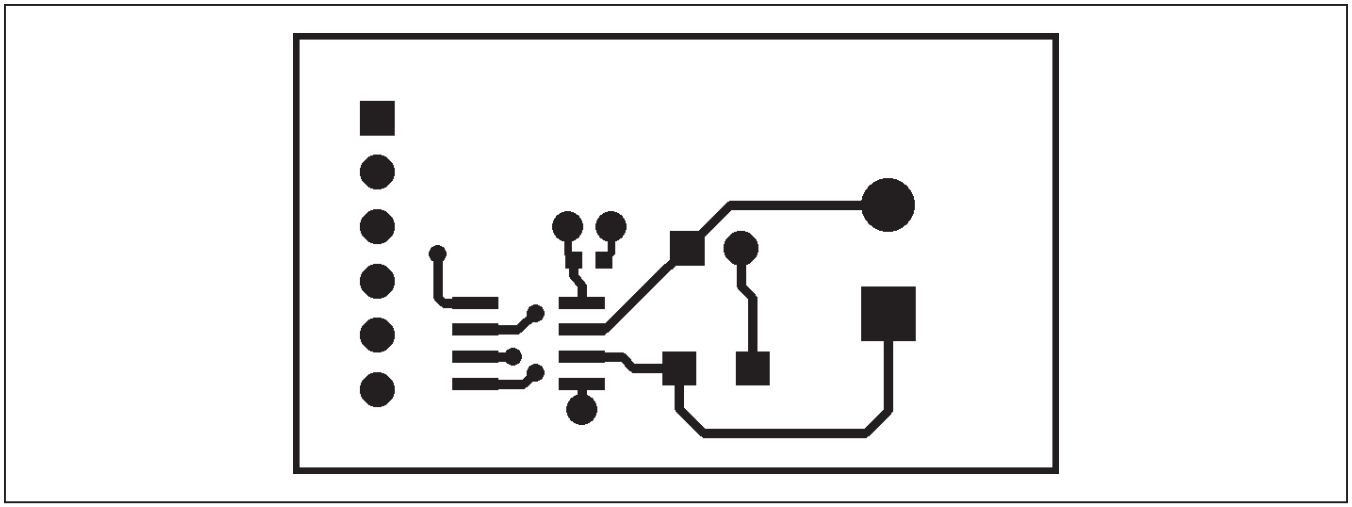


Figure 3. MAX14840PMB1 Peripheral Module PCB Layout—Component Side

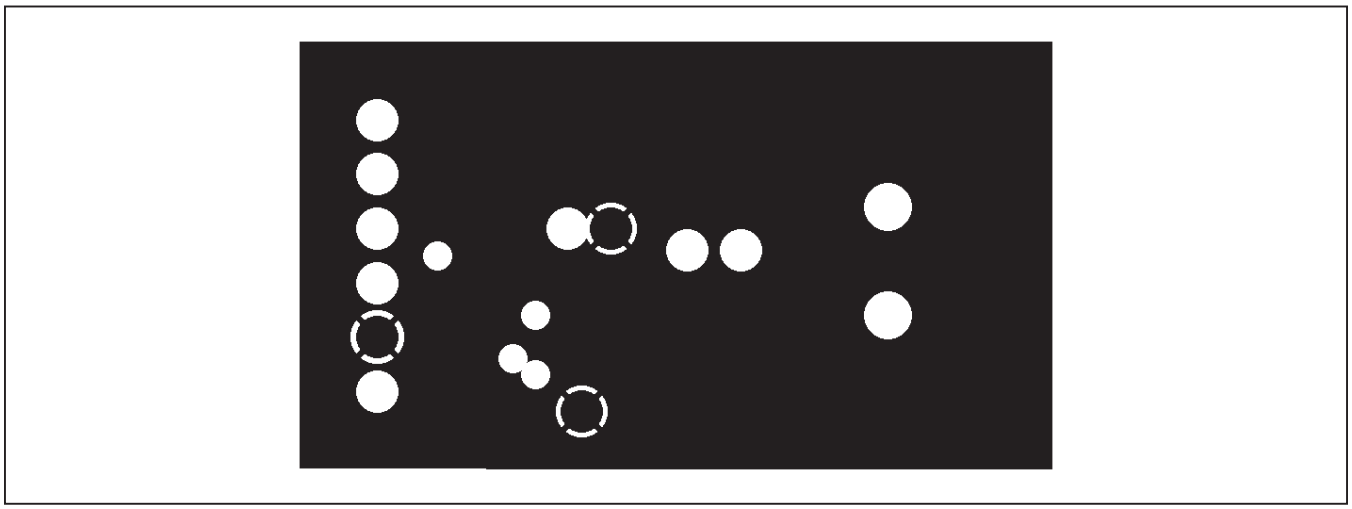


Figure 4. MAX14840PMB1 Peripheral Module PCB Layout—Inner Layer 1 (Ground)

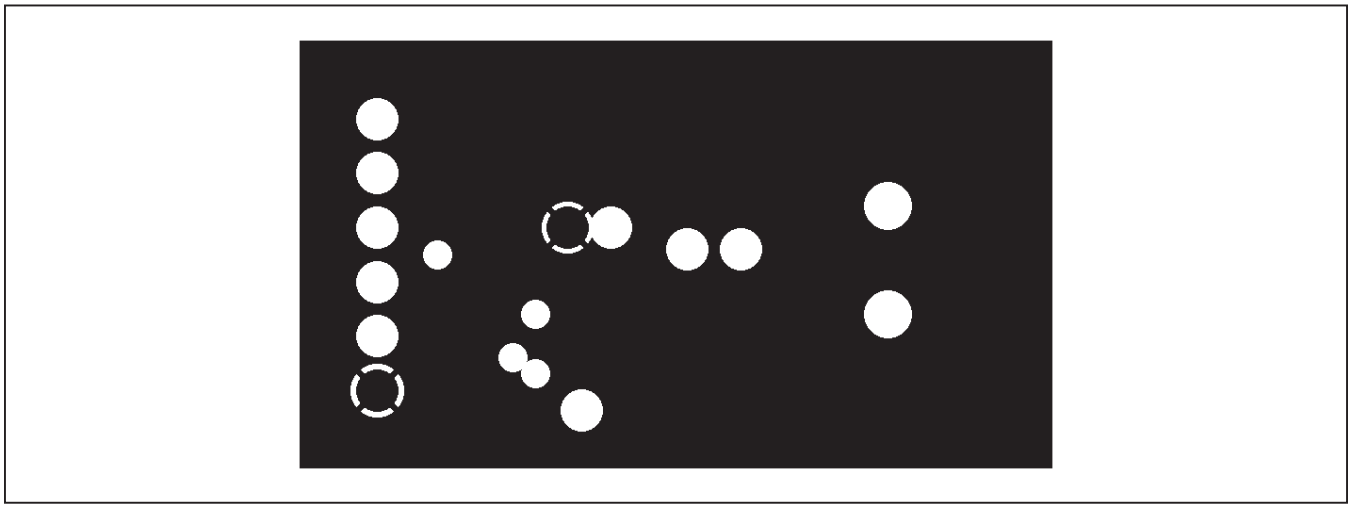


Figure 5. MAX14840PMB1 Peripheral Module PCB Layout—Inner Layer 2 (Power)

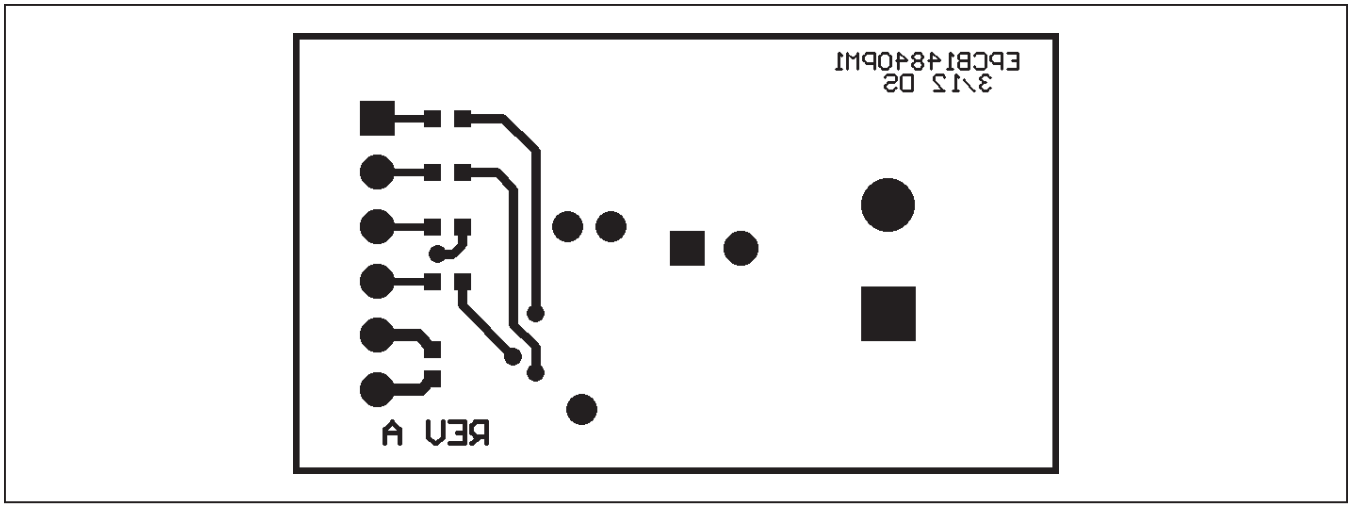


Figure 6. MAX14840PMB1 Peripheral Module PCB Layout—Solder Side

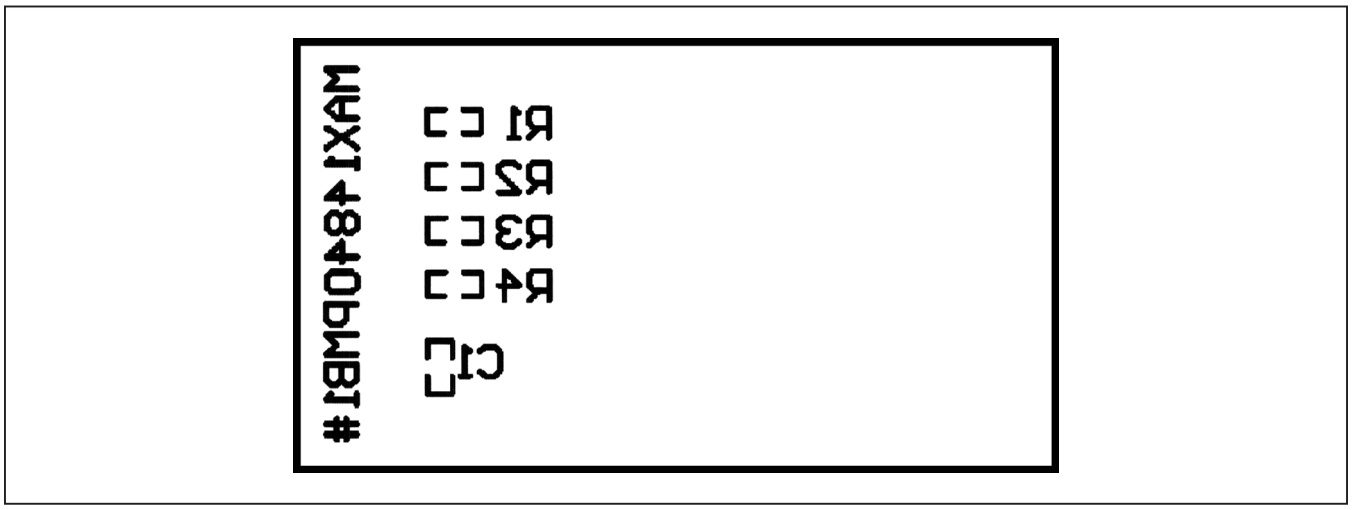


Figure 7. MAX14840PMB1 Peripheral Module Component Placement Guide—Solder Side

Ordering Information

PART	TYPE
MAX14840PMB1#	Peripheral Module

#Denotes RoHS compliant.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—