LIBERTY CHIP™ IC

Am8159

Three-Gun Graphics Color Palette

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Monolithic three-channel video DAC with color look-up table
- 64 x 13 color map
- 83 MHz maximum pixel data rate
- On-chip Address Multiplexer supports system addressing and graphics pixel data addressing
- Compatible with both 8- and 16-bit systems
- Overlay, blank, and composite sync capabilities
- Connects directly to 50- or 75-Ω monitors
- TTL-compatible inputs

GENERAL DESCRIPTION

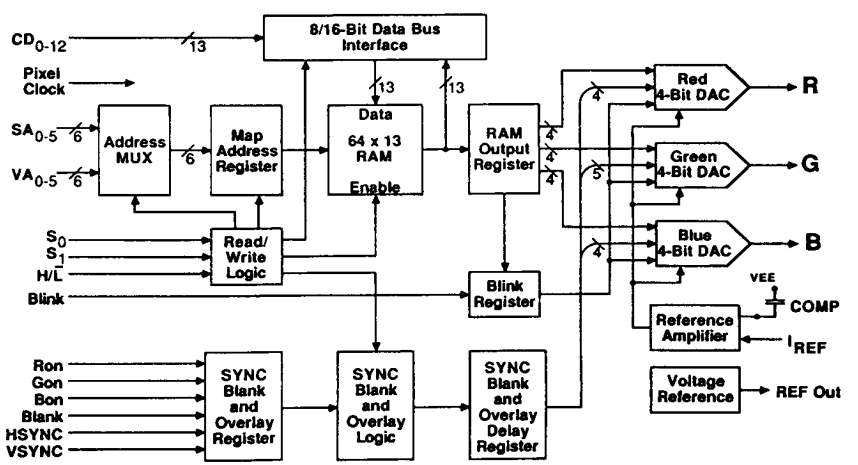
The Am8159 Three-Gun Graphics Color Palette provides a color look-up table and three video DACs on a single chip for use in medium-resolution graphics systems. The palette contains all the necessary logic for sync, blank, and text overlay.

A 64 x 13 RAM acts as a look-up table and supplies color information to be decoded for the three 4-bit DACs. Blink capability is supported by the thirteenth bit in the RAM and a Blink clock input. The Am8159 provides Red, Green, and Blue outputs and allows simultaneous display of 64 colors from a palette of 4096.

An on-chip Address Multiplexer selects either the Video Address pins for the graphics mode, or the System Address pins for loading into or reading from the look-up table. Reading from and writing to the table is handled by two control pins, S_0 and S_1, and thirteen TTL bus-compatible bidirectional Color Data pins.

The video DACs are RS-343-compatible with sync on the Green channel, and connect directly to 50- or 75-Ω monitors.

BLOCK DIAGRAM



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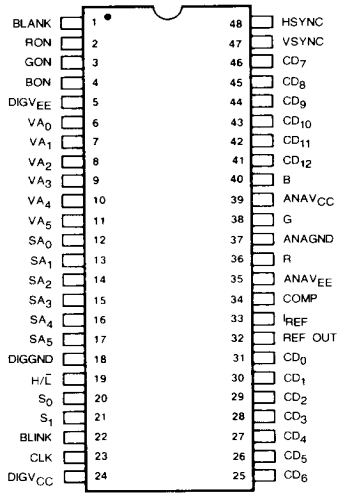
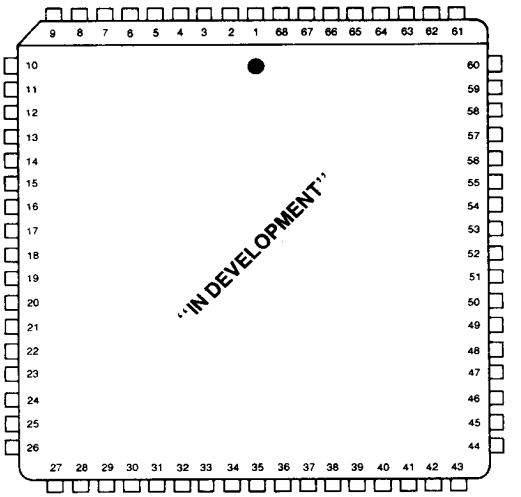
CONNECTION DIAGRAMS
Top View



CD009080



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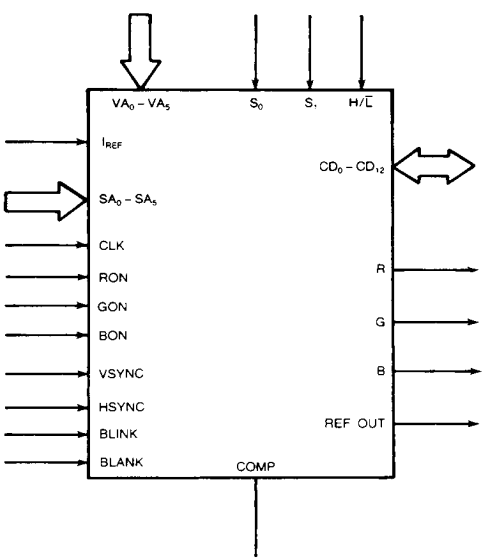
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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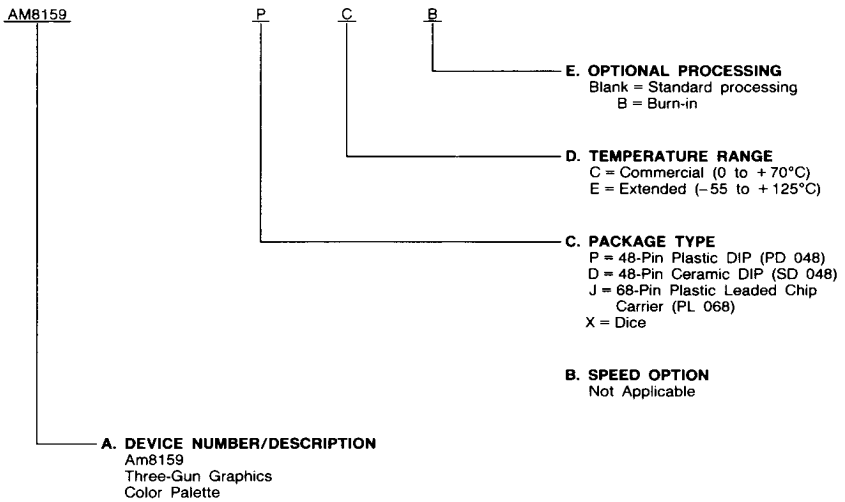
ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



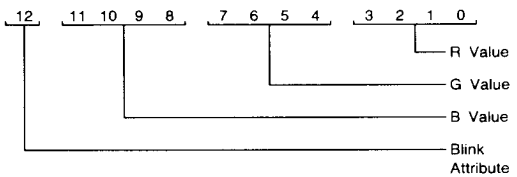
Valid Combinations	
AM8159	PC, PCB, DC, DCB, DE, DEB, JC, XC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$CD_0 - CD_{12}$ Color Data (I/O, TTL, Three-State)
Color Data pins are used to write into or read back color information from the color map. The data is composed of four fields: three 4-bit, and one single-bit field. Data from each of the 4-bit fields is decoded and sent to the video DACs. The MSBs are CD_3, CD_7, and CD_{11} for the Red, Green, and Blue DACs, respectively. The single-bit field, CD_{12}, is the Blink Attribute bit. A value of 1 on CD_{12}, along with the BLINK input being HIGH, results in the Color Data being inverted. The color data bits are assigned as shown:



S_0, S_1 State Control (Inputs, TTL)
These pins control the operational state of the Am8159. S_1 enables the part for read/write functions and selects which set of address pins is active. S_0 controls the direction of the Color Data pins and is used for text overlay.

H/$\overline{L}$ High/$\overline{\text{Low}}$ Byte Control (Input, TTL)
The Am8159 supports both 8- and 16-bit systems. In 8-bit systems, this input maps the high-order color data bits onto the low-order data pins. With H/$\overline{L}$ LOW, the eight low-order bits are on pins $CD_0 - CD_7$. With H/$\overline{L}$ HIGH, the five high-order bits are mapped onto pins $CD_0 - CD_4$. With H/$\overline{L}$ HIGH, pins $CD_5 - CD_7$ are driven LOW during read operations, and ignored while writing. While writing in 8-bit systems, the eight low-order bits must be written before the five high-order bits. In 16-bit systems, H/$\overline{L}$ should be tied LOW. Note that the table below is used for both Update and Readback operations.

H/$\overline{L}$ = 0	RAM Data	12 11 10 9 8 7 6 5 4 3 2 1 0
	CD Pins	12 11 10 9 8 7 6 5 4 3 2 1 0
H/$\overline{L}$ = 1	RAM Data	12 11 10 9 8
	CD Pins	4 3 2 1 0

$VA_0 - VA_5$ Video Address (Input, TTL)
$VA_0 - VA_5$ are the registered Video Address inputs for the color map in the Display mode. These pins are selected when S_1 is HIGH.

$SA_0 - SA_5$ System Address (Input, TTL)
$SA_0 - SA_5$ pins are the non-registered System Address inputs for the color map during Update and Readback operations. They may be directly connected to the System Address bus, and are selected when S_1 is LOW.

CLK Clock (Input, TTL)
CLK is the pixel clock input which is used for all internal timing.

RON Red On (Input, TTL)
GON Green On (Input, TTL)
BON Blue On (Input, TTL)
These pins control the level of the Red, Green, and Blue outputs in the Overlay mode. When HIGH, the appropriate video DAC is driven to peak white (10% overbright). When LOW, the output is forced to reference black. These pins enable the user to overlay text onto graphics in up to eight colors.

VSYNC Vertical Sync (Input, TTL)
HSYNC Horizontal Sync (Input, TTL)
The sync pins are internally XORed and connected to the DACs to generate a composite sync signal. Sync inputs override all other inputs and drive the Green output to 40 IRE units (286 mV) below the blanking level, and the Red and Blue outputs to the blanking level. When HSYNC and VSYNC are both active (HIGH), all outputs are driven to the blank level.

BLANK Blank (Input, TTL)
BLANK input is connected to the DAC Decoders to blank the screen during retrace intervals. A HIGH BLANK signal overrides the color data and overlay information and drives all DAC outputs to 10 IRE units (71 mV) below the reference black level.

BLINK Blink (Input, TTL)
This input controls the blinking of the video outputs. When BLINK and the displayed color's Blink Attribute bit, CD_{12}, are both active (HIGH), the color data bits will be inverted.

R Red Output (Output, Analog)
G Green Output (Output, Analog)
B Blue Output (Output, Analog)
R, G, and B are the three video DAC outputs, one for each color gun. These outputs will directly drive 50- or 75-Ω monitor inputs. 75-Ω lines may be doubly terminated with a 75-Ω resistor at the monitor and another 75-Ω resistor at the device output pin. The output voltages may range from ground to −1.4 V or from +1.4 V to ground.

REF OUT Reference Output (Output, Analog)
REF OUT is the output from the on-chip precision Voltage Reference. Typical output value is 2.286 V.

I_{REF} Reference Input (Input, Analog)
I_{REF} is the reference current input for the DACs. A reference resistor is connected from REF OUT to I_{REF} in order to set the full-scale output current of the DACs. A 1-kΩ resistor will result in a 1.071-V peak video signal across a doubly terminated 75-Ω line. Other full-scale currents can be found by the relationship:

$$I_{FS} = \frac{28.56\ V}{R_{REF}}$$

Typical R_{REF} values are shown in the following table.

Load Resistance (Ω)	Full-Scale Current (mA)	R_{REF} (kΩ)	Nearest 5% Standard Value (kΩ)
100.0	10.71	2.67	2.7
75.0	14.28	2.00	2.0
50.0	21.42	1.33	1.3
37.5	28.56	1.00	1.0

COMP Reference Compensation
A compensation capacitor for the Reference Amplifier must be connected to this pin. The suggested value is a 0.1 μF paralleled by a 100-pF capacitor to the $ANAV_{EE}$ pin.

$DIGV_{CC}$ Digital Positive Power Supply
Digital, TTL, +5-V power supply.

$ANAV_{CC}$ Analog Positive Power Supply
Analog +5-V power supply for the Voltage Reference and Reference Amplifier.

$DIGV_{EE}$ Digital Negative Power Supply
Digital, ECL, −5.0-V or −5.2-V power supply.

$ANAV_{EE}$ Analog Negative Power Supply
Analog −5.0-V or −5.2-V power supply for the DACs and Reference Amplifier.

DIGGND Digital Ground
Ground for the digital portions of the chip.

ANAGND Analog Ground
Ground for the analog portions of the chip.

FUNCTIONAL DESCRIPTION

The Am8159 Three-Gun Graphics Color Palette has four modes of operation as selected by the State Control pins. These modes are Display, Overlay, Update, and Readback.

TABLE 1. MODES OF OPERATION

Inputs		Description	
S_1	S_0	Operational Mode	Active Address
0	0	Update (Write)	$SA_0 - SA_5$
0	1	Readback (Read)	$SA_0 - SA_5$
1	0	Overlay	N.A.
1	1	Display (Run)	$VA_0 - VA_5$

In Display or Overlay modes, the Am8159 has three levels of pipeline to allow a high pixel rate and ease system timing requirements. Address and associated sync, blank, and overlay information are latched into registers on one CLK rising edge, with the corresponding video information exiting three CLK cycles later.

In Update and Readback modes, the color look-up table may be loaded, and the stored information read back and verified.

Address Multiplexer and Decoder

The on-chip Address Multiplexer allows interfacing with both the System Address, as well as the Video Address bus. With S_1 HIGH, data on the Video Address pins ($VA_0 - VA_5$) is latched in the Map Address Register on the first rising edge of CLK . The Map Address Registers drive the RAM Decoders and select one of the 64 13-bit words stored in the color map. In Update or Readback mode S_1 LOW), System Address pins ($SA_0 - SA_5$) are active and the Map Address Registers are transparent.

Color Map and Registers

The color map consists of a 64 x 13 RAM, and is organized as 64 13-bit words. Each word is made up of four fields: three 4-bit fields for each of the decoders (Red, Green, and Blue), and one single-bit field for the Blink Attribute bit. In the Display and Overlay modes, color data from the RAM is latched into the RAM Output Registers on the second rising edge of the CLK . In Readback mode, RAM Output Registers are transparent, and outputs of the RAM connect to the Color Data pins ($CD_0 - CD_{12}$).

Sync, Blank, and Overlay

To ease system timing, HSYNC, VSYNC, BLANK, S_0, S_1, RON, GON, and BON signals are delayed the same number of CLK cycles as the corresponding video address. In the Overlay mode, the RON, GON, and BON pins are used to override the color data in the RAM, forcing the DAC outputs to peak white when HIGH, or reference black when LOW. Peak white is 10% brighter than reference white, such that light colored text may still be visible over a light background. The RON, GON, and BON pins allow text to be displayed over graphics in eight colors. The BLANK signal overrides all color and overlay information and forces all video outputs to a blank level of 10 IRE units (71 mV) below reference black. The HSYNC and VSYNC inputs are internally XORed to create a composite sync signal. A HIGH composite sync signal overrides all color, overlay and blank signals, and forces the Green DAC to a sync level of 40 IRE units (286 mV) below blank. The Red and Blue DACs are forced to the blank level. When HSYNC and VSYNC are both active (HIGH), all video outputs are at the blank level.

DAC Decoder and DAC

Each of the DAC decoders (Red, Green, and Blue) receives one 4-bit word from the color data registers. Additionally, the Blink Attribute bit is ANDed with the Blink clock signal. When the result is active (HIGH), the 4-bit word from the color data registers is inverted in each of the decoders. The 4-bit word is fully decoded to drive fifteen gray-scale current switches. The DACs are fully decoded to ensure that all color transitions consist purely of current switches turning either off or on. This architecture leads to a DAC with less glitch energy than a standard R-2R construction, where transitions commonly have current switches turning off while others are turning on simultaneously. Additional input signals come from the Sync, Blank, and Overlay output registers. These signals override the color data information to switch the gray-scale as well as the larger current sources needed to force the DACs to the appropriate sync or blank output levels. All decoded signals are registered before driving the DAC switches to minimize timing skew that would result in the glitching of the output waveform. The Red and Blue DACs consist of fifteen gray-scale current sources, as well as current sources for 10% overbright and blanking. The Green DAC is similar, with the addition of a current source switch for sync level capabilities.

Voltage Reference

An on-chip precision Voltage Reference is included for setting the full-scale output current. A reference current is generated by placing a reference resistor between the REF OUT and I_{REF} pins. The relationship between the reference resistor and the full-scale current is:

$$I_{FS} = \frac{28.56\ V}{R_{REF}}$$

The Voltage Reference output has a typical value of 2.286 V.

Color Data Input/Output

The Am8159 supports both 8- and 16-bit systems. The Color Data pins are bidirectional and TTL bus-compatible where CD_{12} is the MSB. In 8-bit systems the $H/\overline{L}$ input maps the high-order color data bits onto the low-order data pins. With $H/\overline{L}$ LOW, the eight low-order bits are placed on pins $CD_0 - CD_7$. With $H/\overline{L}$ HIGH, the five high-order bits are mapped onto pins $CD_0 - CD_4$. When $H/\overline{L}$ is HIGH, pins $CD_5 - CD_7$ are driven LOW during a Readback, and are ignored while writing. In 8-bit systems the eight low-order bits must be written into the RAM before the five high-order bits. In 16-bit systems, $H/\overline{L}$ should be tied LOW.

TABLE 2. FUNCTION TABLE

Inputs									Outputs		
R, G, BON	S_1	S_0	BLANK	HSYNC	VSYNC	BLINK	CD_{12}	Color Data	Current	Voltage into 37.5 Ω	Description
H	H	L	L	L	L	X	X	X	0 mA	0 mV	Peak White
X	H	H	L	L	L	L	X	15	1.892 mA	−71 mV	Reference White
X	H	H	L	L	L	X	L	15	1.892 mA	−71 mV	Reference White
								.	.	.	
								.	.	.	15 Equal Steps
								.	.	.	
X	H	H	L	L	L	X	L	0	19.040 mA	−714 mV	Reference Black
X	H	H	L	L	L	L	X	0	19.040 mA	−714 mV	Reference Black
X	H	H	L	L	L	H	H	0	1.892 mA	−71 mV	Reference White
								.	.	.	
								.	.	.	15 Equal Inverse Steps
								.	.	.	
X	H	H	L	L	L	H	H	15	19.040 mA	−714 mV	Reference Black
L	H	L	L	L	L	X	X	X	19.040 mA	−714 mV	Reference Black
X	X	X	H	L	L	X	X	X	20.932 mA	−785 mV	Blanking
X	X	X	X	H	H	X	X	X	20.932 mA	−785 mV	Blanking
X	X	X	X	H	L	X	X	X	28.560 mA	−1071 mV	Composite Sync*
X	X	X	X	L	H	X	X	X	28.560 mA	−1071 mV	Composite Sync*

H = HIGH L = LOW X = Don't Care

*Green Only. Red and Blue are at Blanking Level.

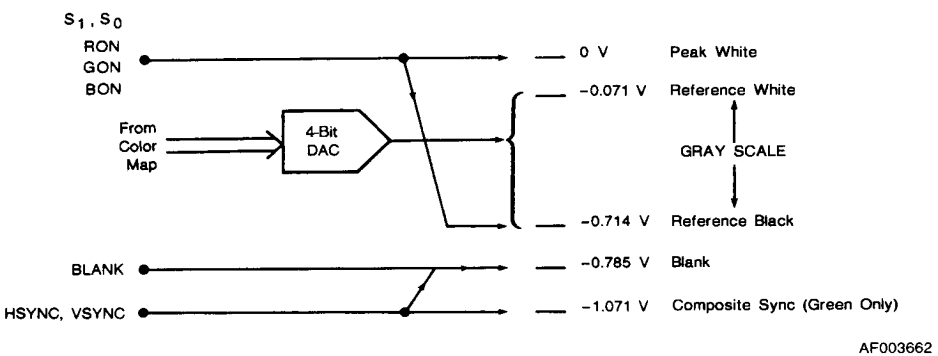


Figure 1. Am8159 DAC Output Levels

APPLICATIONS

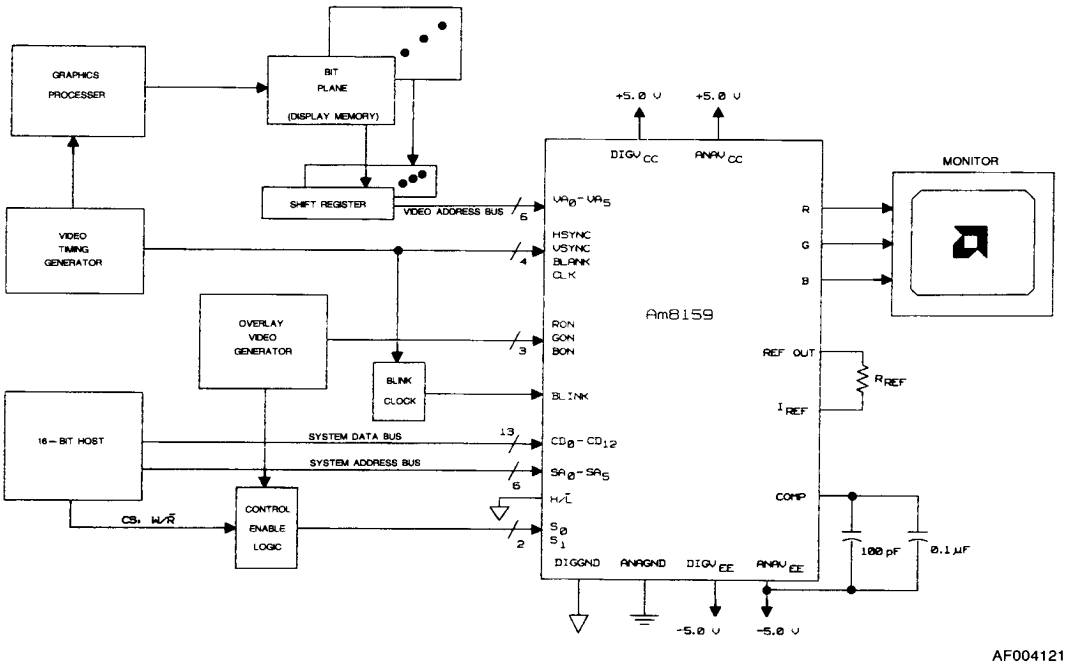


Figure 2. Typical Application Diagram

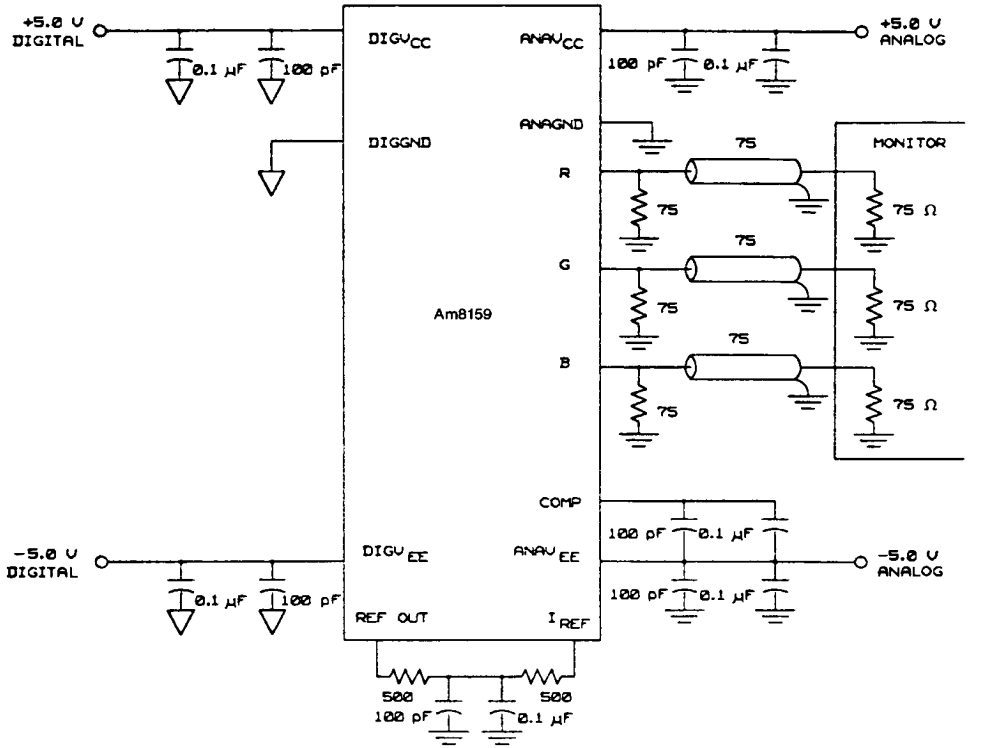


Figure 3. Typical Connection Diagram

Key: = Digital Ground

= Analog Ground

TB000210

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Positive Supply Voltage ..... −0.7 to +7.0 V
Negative Supply Voltage ..... +0.7 to −7.0 V
DC Input Voltage (TTL) ..... −0.5 to +7.0 V
DC Input Current (TTL) ..... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Positive Supply Voltages
Digital ($DIGV_{CC}$) and Analog ($ANAV_{CC}$) ... +5 V ±5%
Negative Supply Voltages
Digital ($DIGV_{EE}$) and Analog ($ANAV_{EE}$) ... −5 V +5%, −5 V −9.2%

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Positive Supply Voltages
Digital ($DIGV_{CC}$) and Analog ($ANAV_{CC}$) ..... (to come)
Negative Supply Voltages
Digital ($DIGV_{EE}$) and Analog ($ANAV_{EE}$) ..... (to come)

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over Commercial Operating Range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Typ. (Note 3)	Max.	Units
V_{IH}	Input HIGH level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			40	μA
I_I	Input HIGH Current	V_{IN} = V_{CC} = 5.25 V			0.1	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = −400 μA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA			0.5	Volts
I_{SC}	Output Short-Circuit Current (Note 4)	V_{CC} = Max.	10		50	mA
$DIGI_{CC}$	Power Supply Current	$DIGV_{CC}$ = Max.		45	70	mA
$ANAI_{CC}$	Power Supply Current	$ANAV_{CC}$ = Max.		5	12.5	mA
$DIGI_{EE}$	Power Supply Current	$DIGV_{EE}$ = Max.		180	300	mA
$ANAI_{EE}$	Power Supply Current (Note 7)	$ANAV_{EE}$ = Max.		75	100	mA

Notes: See notes following Reference Voltage Specifications table.

DAC SPECIFICATIONS over Commercial Operating Range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Notes 1 & 5)	Min.	Typ.	Max.	Units
	Resolution	Gray Scale	4	4	4	Bits
	Nonlinearity	Gray Scale			±0.125	LSB
	Differential Nonlinearity	Gray Scale (Note 6)			±0.125	LSB
V_{OC}	Output Voltage Compliance			±1.4		Volts
I_{ZS}	Zero-Scale Current				10	μA
I_{MAX}	Maximum Output Current				28.56	mA
	Full-Scale Tracking				3	% Gray Scale
	Full-Scale Tempco			50		ppm/°C
PSSI	Power Supply Sensitivity	(Note 6)			0.4	% Gray Scale
I_{REF}	Reference Current				2.3	mA
C_{OUT}	Output Capacitance	(Note 6)		10		pF
	Glitch Energy	(Note 6)		50		pV-sec
t_R	Rise Time: 10 to 90%	(Note 8)				ns
t_F	Fall Time: 90 to 10%	(Note 8)				ns
t_S	Settling Time	±0.5 LSB (Note 6)		5		ns
f_{CLK}	Clock Frequency	(Note 8)	DC		83	MHz

Notes: See notes following Reference Voltage Specifications table.

REFERENCE VOLTAGE SPECIFICATIONS over Commercial Operating Range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Typ.	Max.	Units
V_{REF}	Reference Voltage	I_{REF} = 1 to 2.3 mA	2.263	2.286	2.309	Volts
	Line Regulation				0.4	$\%V_{REF}$
	Reference Voltage Tempco	T_A = 0 to +70°C (Note 6)		50		ppm/°C

Notes*: 1. For conditions shown as Min. or Max., use the appropriate values specified under recommended operating ranges.
2. V_{IH}, V_{IL} are tested for each input at least once. Thereafter, hard HIGH and LOW levels are used for all other tests.
3. All typical values are at V_{CC} = 5.0 V, V_{EE} = −5.0 V, and T_A = 25°C. The device may be operated with a V_{EE} of −5.2 V with no effect on performance.
4. Not more than one output should be shorted at a time. Duration of short not to exceed one second.
5. Gray Scale is defined as output levels between reference white and reference black. DAC nonlinearity and differential nonlinearity are measured at a frequency less than or equal to 10 MHz in production over operating temperature range at nominal supply voltages. DAC output terminated into 37.5-Ω load, with a full scale current of 28.56 mA.
6. This typical value is provided for design reference and will not be tested in production.
7. Power supply currents include load current through a 37.5-Ω load to ground on all three outputs. Reference equals 1.0 kΩ.
8. Not all tests are being performed in manufacturing. Tests are guaranteed by engineering characterization with periodic manufacturing sampling.

*Notes listed correspond to respective references made in DC Characteristics, DAC Specifications, and Reference Voltage Specification tables.

Explanation of DAC Specifications

Resolution

Resolution refers to the number of discrete steps or levels which the DAC can provide, and is expressed as a number of bits. A DAC having n bits of resolution provides 2^n discrete analog steps. Each of these analog steps is referred to as a least significant bit, or LSB.

Nonlinearity

Nonlinearity is the maximum deviation of an actual DAC output from an ideal output defined by a straight line drawn through the end points of the transfer function. A DAC must be linear to within 1/2 a step to be accurate to its full resolution.

Differential Nonlinearity

Differential Nonlinearity (DNL), is the maximum deviation of any actual output step from an ideal step size. If the DNL is specified as 1/2 LSB, or step, the step size from one step to the next may be from 1/2 to 3/2 of an ideal step.

Output Voltage Compliance

The Output Voltage Compliance is that voltage which may be impressed on the output current pins without degrading the specified accuracy of the DACs.

Zero-Scale Current

Zero-Scale Current is the current produced at the peak white output level.

Maximum Output Current

The Maximum Output Current is the maximum current at the sync level that the outputs may operate at without degrading the specified accuracy of the DACs.

Full-Scale Tracking

The Full-Scale Tracking is the maximum deviation in output current levels between the three DAC outputs when all DACs are at Reference Black.

Full-Scale Tempco

The Full-Scale Temperature Coefficient (Tempco) is the effect of temperature change, within the operating range, on the DAC output current. This is specified as the change in current per degree centigrade.

Power Supply Sensitivity

The effect of a power supply voltage change on the DAC current output is referred to as power supply sensitivity (PSSI). For the Am8159 the PSSI is expressed as a percentage change in any output current level while the supply voltage varies over the recommended operating range. This specification assumes the internal voltage reference is used.

Reference Current

Reference Current is the range of acceptable reference current at the I_{REF} pin.

Output Capacitance

Output Capacitance is the capacitance seen at any of the DAC output pins.

Glitch Energy

Glitch Energy is the product of voltage and time for any transient ringing around a final DAC transition output level.

Rise Time, Fall Time

The Rise or Fall Time is the time that any DAC transition takes to change from 10 to 90, or 90 to 10 percent of the transition voltage.

Settling Time

Settling Time is the time from when the output first changes until the output remains within a certain error band around the final output voltage level.

Clock Frequency

The Clock Frequency is that range of clock frequencies for which the device outputs remain 4-bit accurate.

Explanation of Reference Voltage Specifications

Reference Voltage

The Reference Voltage is the output voltage provided by the reference voltage source.

Line Regulation

The effect of a change in supply voltage on the reference voltage output is the Line Regulation. For the Am8159 this is given as a percent change of the reference voltage caused by supply voltage changes within the operating range.

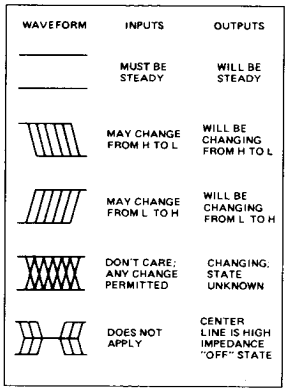
Load Regulation

The change in the reference voltage caused by a change in the current sourced by the reference current output is the Load Regulation. For the Am8159 this is given as a percent change in reference voltage for changes in current as specified.

Reference Voltage Temperature Coefficient

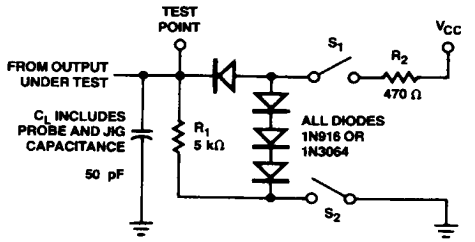
The Reference Voltage Temperature Coefficient is the effect of temperature change on the reference voltage. This is shown as the change in voltage per degree centigrade.

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING TEST CIRCUIT



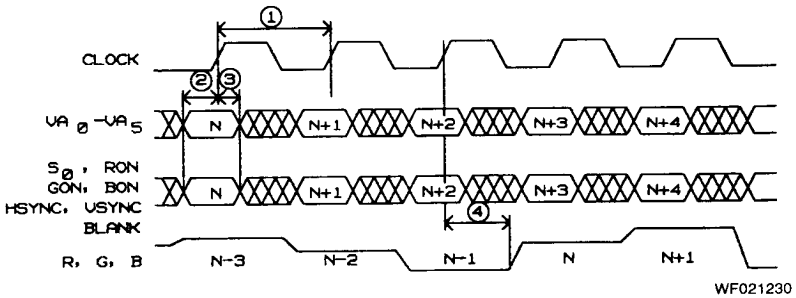
TC002871

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

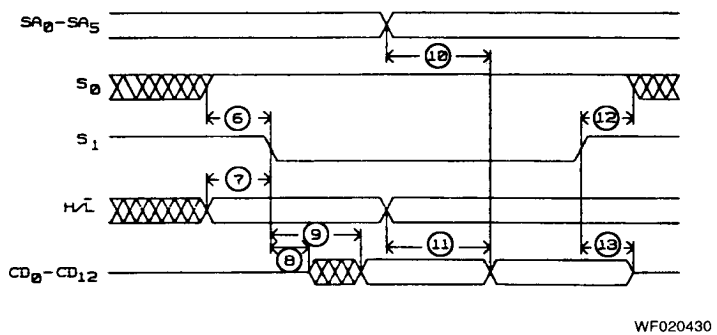
No.	Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
1	t_{CLK}	Clock Period (Note 8)	12			ns
2	t_S	$VA_0 - VA_5$, S_0, RON, GON, BON, HSYNC, VSYNC, BLANK Setup Before CLK ↑ (Note 8)	5			ns
3	t_H	$VA_0 - VA_5$, S_0, RON, GON, BON, HSYNC, VSYNC, BLANK Hold After CLK ↑ (Note 8)	2			ns
4	t_{PD}	CLK ↑ to 10% R, G, B Change			12	ns
5	Δt_{PD}	Skew in CLK ↑ to 10% Change Between R, G, and B Outputs (Note 8)			1.2	ns
6	t_S	S_0 Setup Before S_1 ↓	0			ns
7	t_S	H/$\overline{L}$ Setup Before S_1 ↓	0			ns
8	t_{PD}	S_1 ↓ to Data Active	10			ns
9	t_{PD}	S_1 ↓ to Data Valid			30	ns
10	t_{PD}	Address Change to Data Change	10		30	ns
11	t_{PD}	H/$\overline{L}$ Change to Data Change	10		30	ns
12	t_H	S_0 Hold After S_1 ↑ (Note 8)	5			ns
13	t_{PD}	S_1 ↑ to High Z			30	ns
14	t_W	Write Pulse Width	70			ns
15	t_S	Address Setup Before S_1 ↓	0			ns
16	t_H	Address Hold After S_1 ↑ (Note 8)	5			ns
17	t_H	H/$\overline{L}$ Hold After S_1 ↑	5			ns
18	t_S	Data Setup Before S_1 ↑	30			ns
19	t_H	Data Hold After S_1 ↑	7			ns

Notes: See notes following Reference Voltage Specifications table.

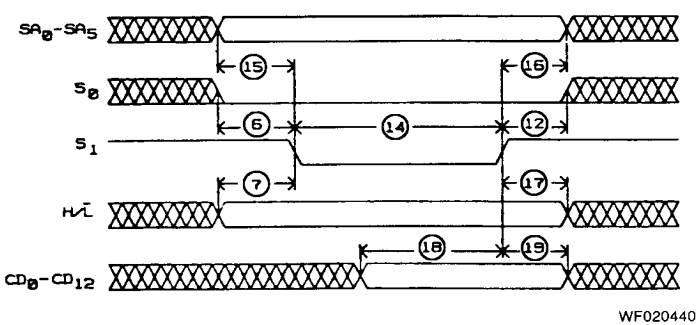
SWITCHING WAVEFORMS



Run and Overlay Timing

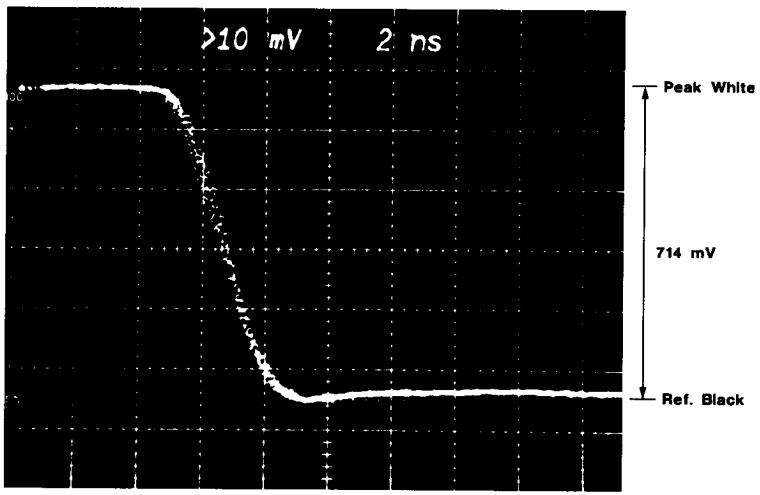


Read Timing



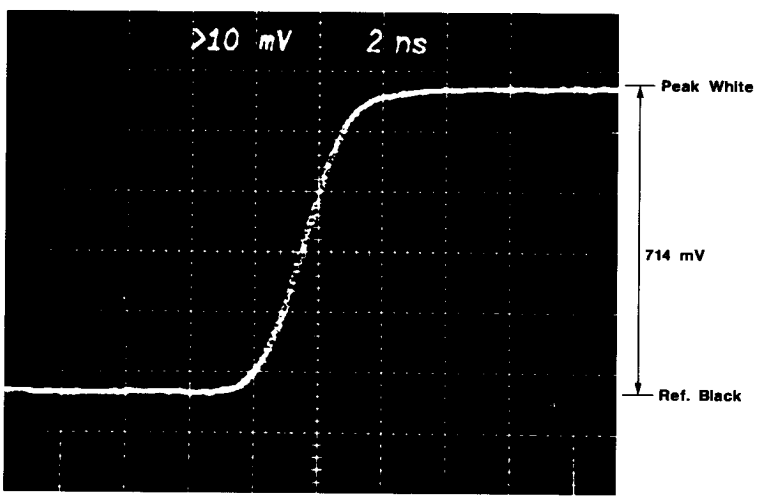
Write Timing

TYPICAL PERFORMANCE CURVES



OP002200

G Output Falling Edge

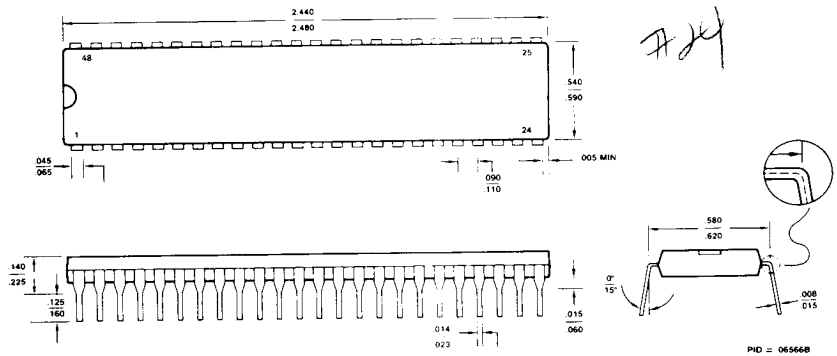


OP002190

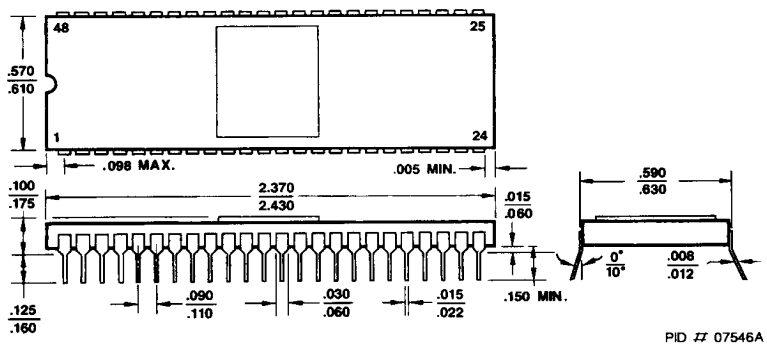
G Output Rising Edge

PHYSICAL DIMENSIONS

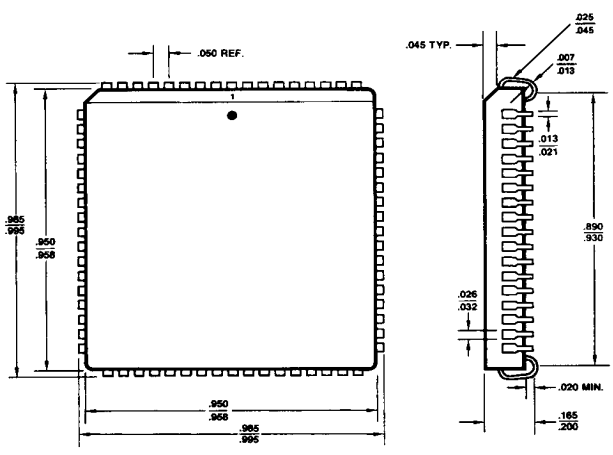
PD 048



SD 048



PL 068



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