To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

HD74SSTV16857A

1:1 14-bit SSTL_2 Registered Buffer

ADE-205-695 (Z)

Rev.0
Jun. 2002

Description

The HD74SSTV16857A is a 14-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

Features

- Supports LVCMOS reset ($\overline{\text{RESET}}$) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Package type

Package type	Package code	Package suffix	Taping code
TSSOP-48 pin	TTP-48DBV	T	EL (1,000 pcs / Reel)
TVSOP-48 pin	TTP-48DEV	N	EL (1,000 pcs / Reel)

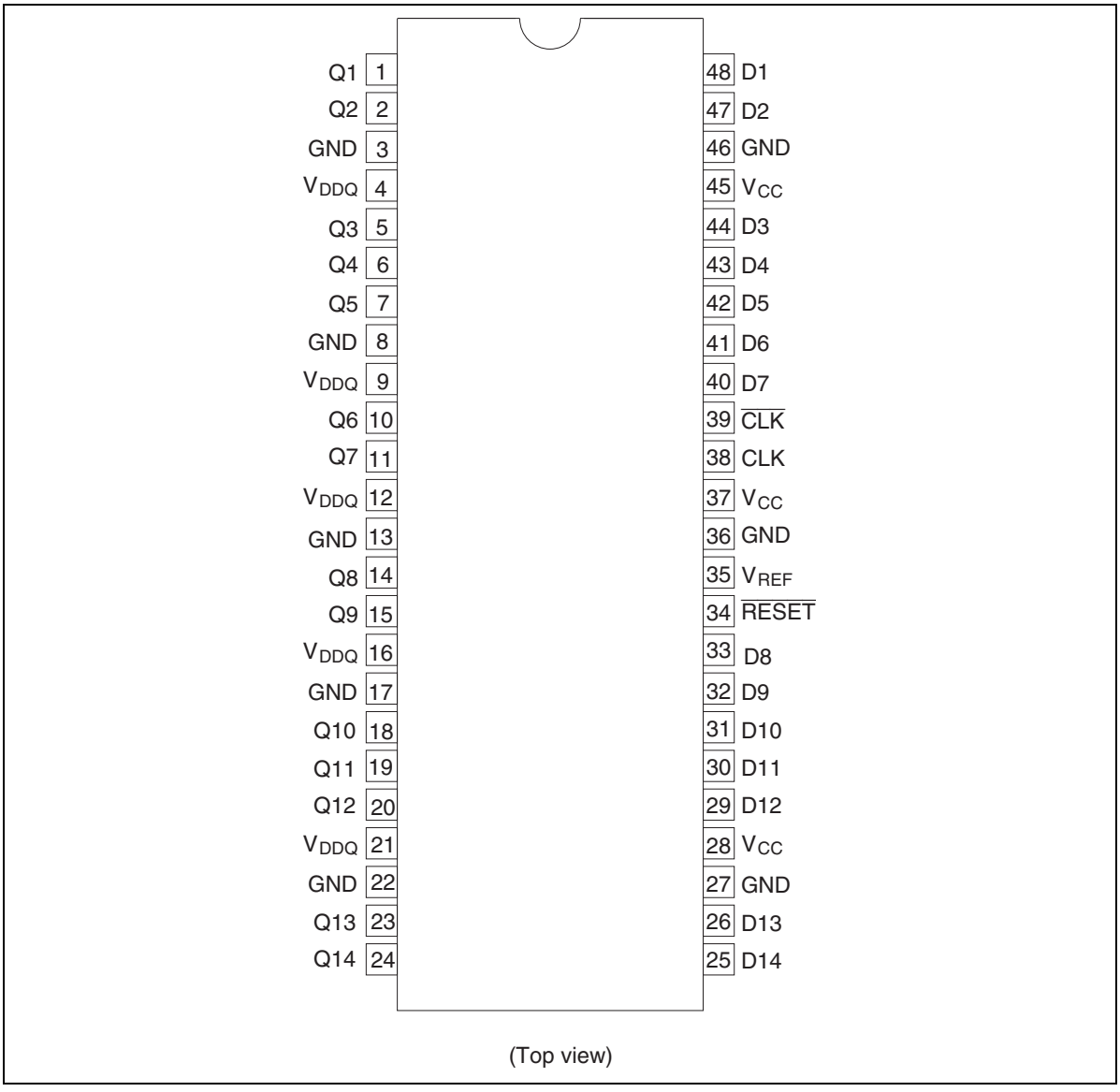
Function Table

Inputs				Output Q
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	H or L	X	Q_0 [*1]

H : High level
L : Low level
X : Immaterial
↑ : Low to high transition
↓ : High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC} or V_{DDQ}	–0.5 to 3.6	V	
Input voltage [*1]	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1, 2]	V_O	–0.5 to V_{DDQ}+0.5	V	
Input clamp current	I_{IK}	±50	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
V_{CC}, V_{DDQ} or GND current / pin	I_{CC}, I_{DDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)	P_T	115	°C / W	TSSOP
Storage temperature	Tstg	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.

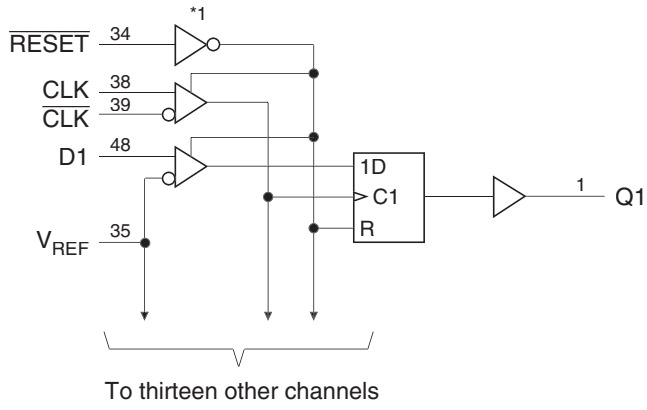
RENESAS

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage		V_{CC}	V_{DDQ}	2.5	2.7	V	
Output supply voltage		V_{DDQ}	2.3	2.5	2.7	V	
Reference voltage		V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination voltage		V_{TT}	V_{REF}–40 mV	V_{REF}	V_{REF}+40 mV	V	
Input voltage		V_I	0	—	V_{CC}	V	
AC high level input voltage		V_{IH}	V_{REF}+310 mV	—	—	V	D
AC low level input voltage		V_{IL}	—	—	V_{REF}–310 mV	V	D
DC high level input voltage		V_{IH}	V_{REF}+150 mV	—	—	V	D
DC low level input voltage		V_{IL}	—	—	V_{REF}–150 mV	V	D
High level input voltage		V_{IH}	1.7	—	V_{DDQ}+0.3	V	$\overline{\text{RESET}}$
Low level input voltage		V_{IL}	–0.3	—	0.7	V	$\overline{\text{RESET}}$
Differential input voltage	(Common mode range)	V_{CMR}	0.97	—	1.53	V	CLK, $\overline{\text{CLK}}$
	(Minimum peak to peak input)	V_{PP}	360	—	—	mV	CLK, $\overline{\text{CLK}}$
High level output current		I_{OH}	—	—	–20	mA	
Low level output current		I_{OL}	—	—	20	mA	
Operating temperature		Ta	0	—	70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

Logic Diagram



Note: 1. $\overline{\text{RESET}}$ input gate is connected to V_{DDQ}.

Electrical Characteristics

Item		Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input diode voltage		V_{IK}	2.3	—	—	–1.2	V	I_{IN} = –18 mA
Output voltage		V_{OH}	2.3 to 2.7	V_{CC}–0.2	—	—	V	I_{OH} = –100 µA
			2.3	1.95	—	V_{DDQ}		I_{OH} = –16 mA
		V_{OL}	2.3 to 2.7	—	—	0.2		I_{OL} = 100 µA
			2.3	0	—	0.35		I_{OL} = 16 mA
Input current	(All inputs)	I_{IN}	2.7	—	—	±5	µA	V_{IN} = 2.7 V or 0
Quiescent supply current		I_{CC} [*2]	2.7	—	25	45	mA	V_{IN} = $V_{IH(AC)}$ or $V_{IL(AC)}$, I_O = 0
Standby current		$I_{CC\ (stdy)}$	2.7	—	—	10	µA	$\overline{RESET}$ = GND
Dynamic operating clock only		I_{CCD} [*2]	2.7	—	38	45	µA/ clock MHz	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle
Dynamic operating per each data input		I_{CCD} [*2]	2.7	—	11	15	µA/ clock MHz / data input	$\overline{RESET}$ = V_{CC}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.
Output high [*3]		r_{OH}	2.3 to 2.7	7	—	20 [*4]	Ω	I_{OH} = –20 mA
Output low [*3]		r_{OL}	2.3 to 2.7	7	—	20 [*4]	Ω	I_{OL} = 20 mA
$\lvert r_{OH} - r_{OL} \rvert$ each separate bit [*3]		$r_{O(\Delta)}$	2.5	—	—	4	Ω	I_O = 20 mA, Ta = 25°C
Input capacitance	Data inputs	C_{IN}	2.5 [*1]	2.5	—	3.5	pF	V_I = V_{REF}±310 mV
	CLK and $\overline{CLK}$			2.5	—	3.5		V_{CMR} = 1.25 V, V_{PP} = 360 mV
	$\overline{RESET}$			—	3.0	—		V_I = V_{CC} or GND

Notes: 1. All typical values are at V_{CC} = 2.5 V, Ta = 25°C.

2. Total I_{CC} (max) = I_{CC} + {I_{CCD} (clock)×f(clock)} + {I_{CCD} (Data)×1/2f(clock)×14}
3. This is effective in the case that it did terminate by resistance.
4. See figure. 1, 2.

RENESAS

Switching Characteristics

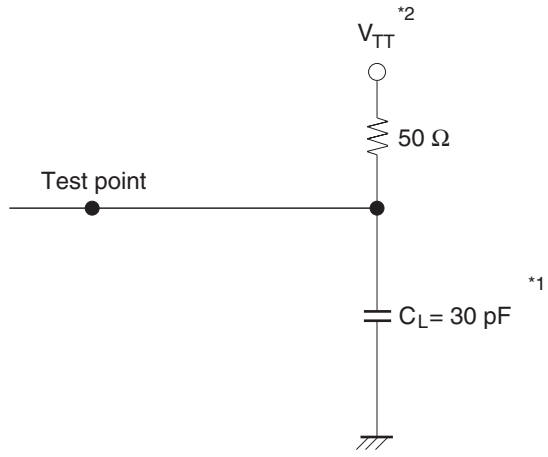
Item		Symbol	V_{cc} = 2.5 ± 0.2 V		Unit	Test Condition
			Min	Max		
Clock frequency [*1]		f_{clock}	—	200	MHz	
Setup time	Fast slew rate [*4, 6]	t_{su}	0.75	—	ns	Data before CLK↑, $\overline{CLK}$↓
	Slow slew rate [*5, 6]		0.9	—		
Hold time	Fast slew rate [*4, 6]	t_h	0.75	—	ns	Data after CLK↑, $\overline{CLK}$↓
	Slow slew rate [*5, 6]		0.9	—		
Differential inputs active time		t_{act}	22	—	ns	Data inputs must be low after $\overline{RESET}$ high.
Differential inputs inactive time		t_{inact}	22	—	ns	Data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ low.
Pulse width		t_w	2.5	—	ns	CLK, $\overline{CLK}$ "H" or "L"
Output slew [*3]		t_{SL}	1	4	volt/ns	

(C_L = 30 pF, R_L = 50 Ω, $V_{REF} = V_{TT} = V_{DDQ} \times 0.5$)

Item	Symbol	V_{cc} = 2.5±0.2 V			Unit	FROM (Input)	TO (Output)
		Min	Typ	Max			
Maximum clock frequency	f_{max}	200	—	—	MHz		
Propagation delay time [*2]	t_{PLH}, t_{PHL}	1.1	—	2.8	ns	CLK, $\overline{CLK}$	Q
	t_{PHL}	—	—	5.0		$\overline{RESET}$	Q

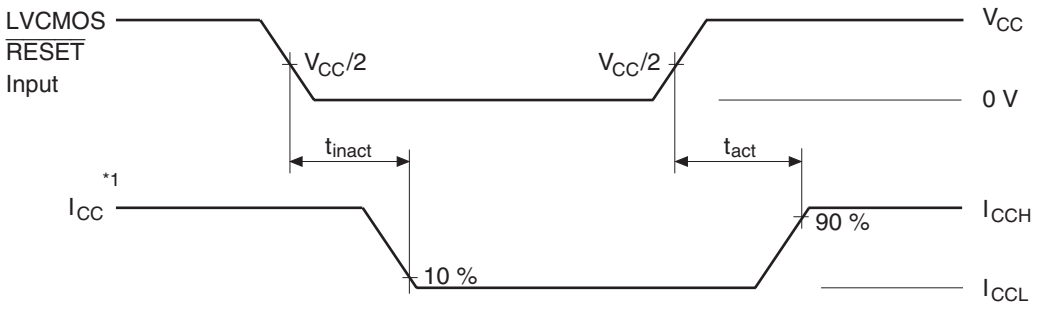
Notes: 1. Although the clock is differential, all timing is relative to CLK going high and $\overline{CLK}$ going low.
2. This timing relationship is specified into test load (see waveforms – 3, 4) with all of the outputs switching.
3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
6. CLK, $\overline{CLK}$ signals input slew rates are ≥ 1 V/ns.

Test Circuit

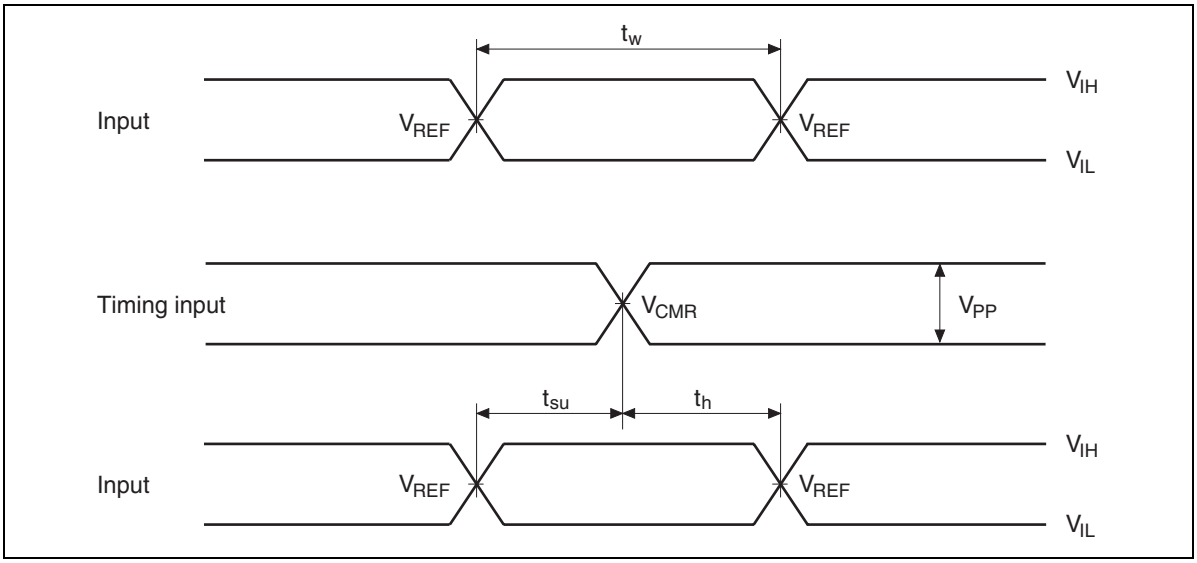


Notes: 1. C_L includes probe and jig capacitance.
2. $V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

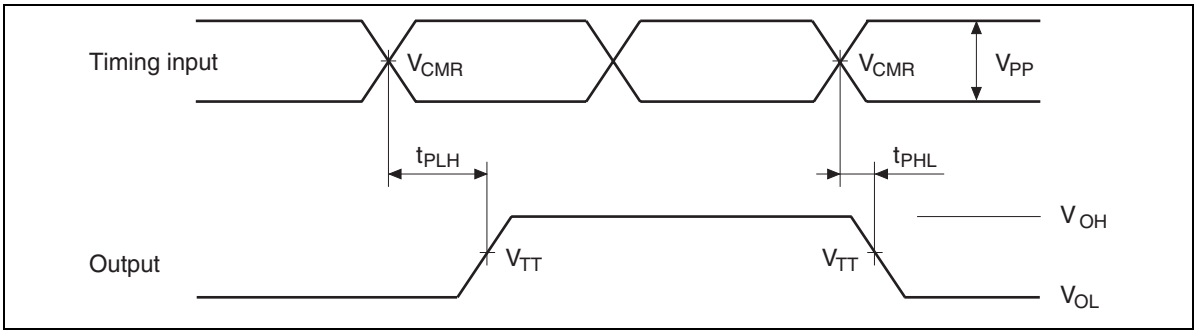
Waveforms – 1



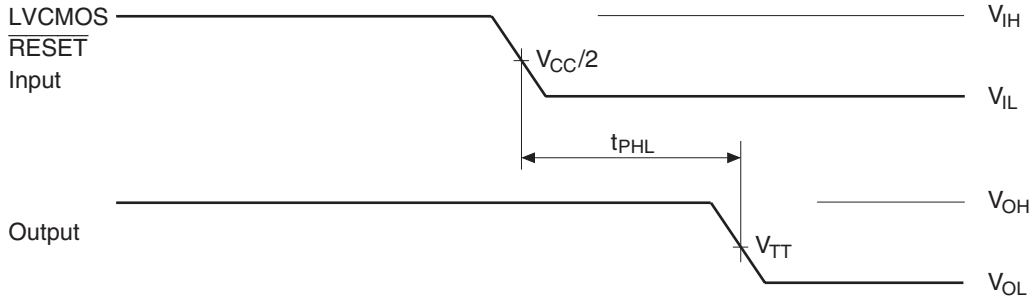
Waveforms – 2



Waveforms – 3



Waveforms – 4



Notes:
1. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and I_O = 0 mA.
2. All input pulses are supplied by generators having the following characteristics : PRR ≤ 10 MHz, Zo = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
3. The outputs are measured one at a time with one transition per measurement.
4. $V_{TT} = V_{REF} = V_{DDQ}/2$
5. $V_{IH} = V_{REF}$+310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{CC}$ for LVCMOS input.
6. $V_{IL} = V_{REF}$–310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
7. t_{PLH} and t_{PHL} are the same as t_{pd}

Application Data

• Pull-down

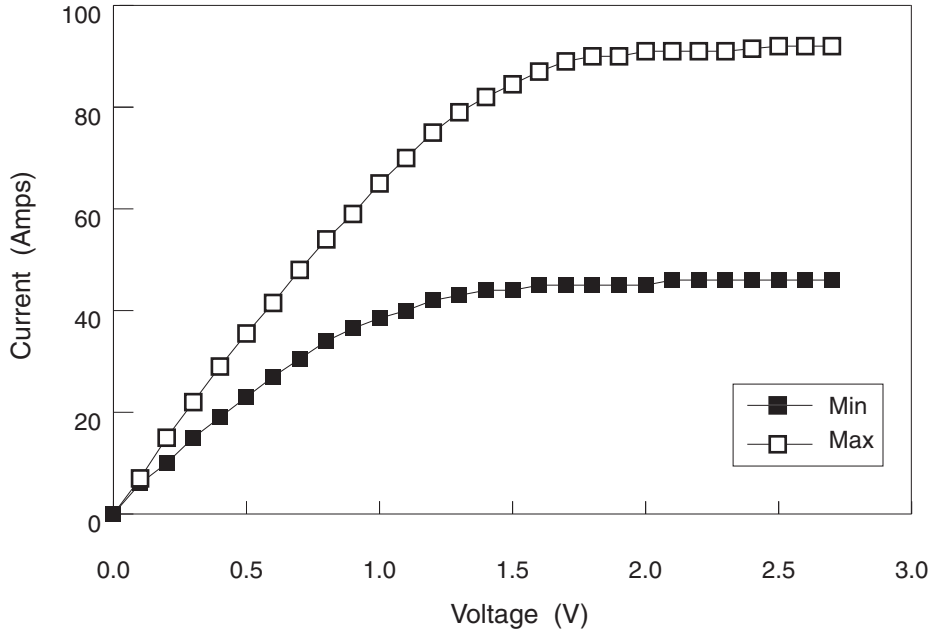


Figure. 1

• Pull-up

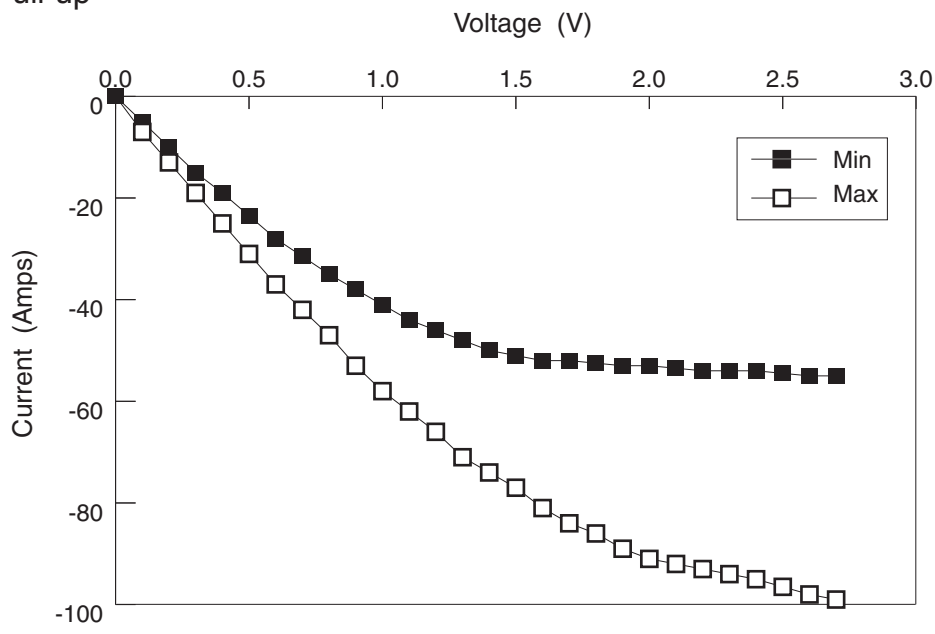


Figure. 2

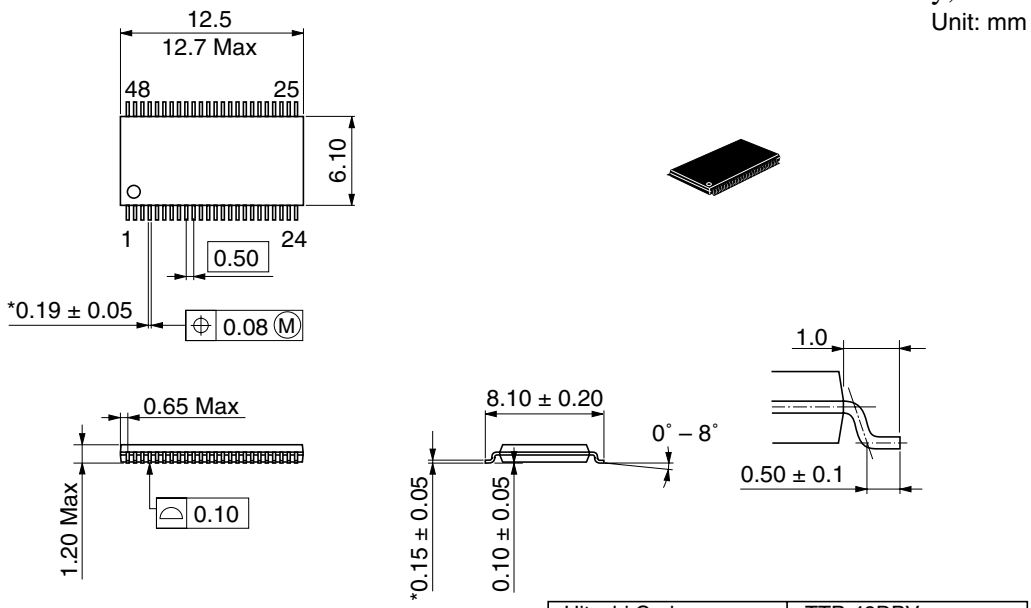
Curve Data

Voltage (V)	Pull-down		Pull-up	
	I (mA)	I (mA)	I (mA)	I (mA)
	Min	Max	Min	Max
0.0	0	0	0	0
0.1	6	7	–6	–7
0.2	11.5	15	–11.5	–13
0.3	16	22	–16	–19
0.4	20	29	–20	–25
0.5	23	35.5	–23.5	–31
0.6	27	41.5	–28	–37
0.7	30.5	48	–31.5	–42
0.8	34	54	–35	–47
0.9	36.5	59	–38	–53
1.0	38.5	65	–41	–58
1.1	40	70	–44	–62
1.2	42	75	–46	–66
1.3	43	79	–48	–71
1.4	44	82	–50	–74
1.5	44	84.5	–51	–77
1.6	45	87	–52	–81
1.7	45	89	–52	–84
1.8	45	90	–52.5	–86
1.9	45	90	–53	–89
2.0	45	91	–53	–91
2.1	46	91	–53.5	–92
2.2	46	91	–54	–93
2.3	46	91	–54	–94
2.4	46	91.5	–54	–95
2.5	46	92	–54.5	–96.5
2.6	46	92	–55	–98
2.7	46	92	–55	–99

Package Dimensions

As of January, 2002

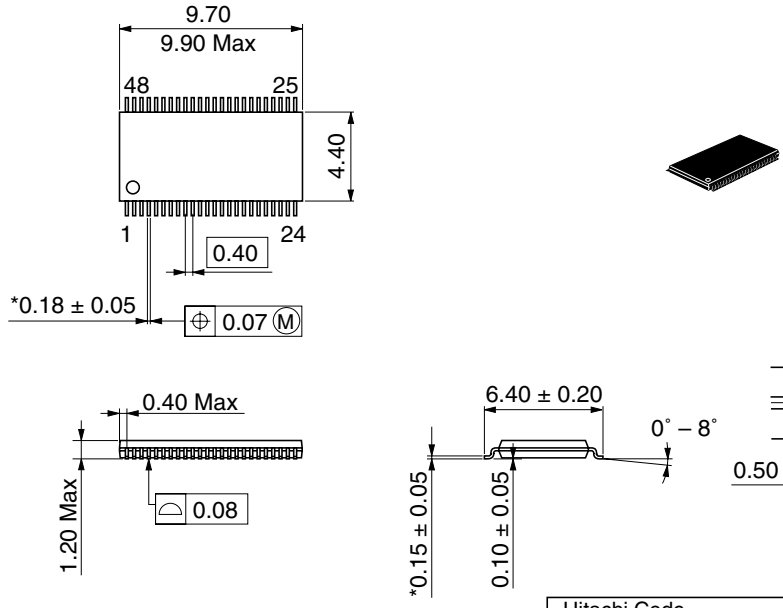
Unit: mm



Hitachi Code	TTP-48DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.20 g

*Pd plating

Unit: mm



*Pd plating

Hitachi Code	TTP-48DEV
JEDEC	—
JEITA	—
Mass (reference value)	—

Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

Sales Offices

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL http://www.hitachisemiconductor.com/

For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel : <65>-6538-6533/6538-8577
Fax : <65>-6538-6933/6538-3877
URL : http://semiconductor.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel : <852>-2735-9218
Fax : <852>-2730-0281
URL : http://semiconductor.hitachi.com.hk

Copyright © Hitachi, Ltd., 2002. All rights reserved. Printed in Japan.

Colophon 6.0

RENESAS