

Features

- CMOS logic output
- Ceramic package (No bump or with bump)
- Space savings
- Available on 24 mm Tape & Reel
- Enable/Disable feature
- Tight symmetry (45 to 55%) "R" version available

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O	-0.5 to $V_{CC} + 0.5$	V
Input current	I_{IN}	± 10	mA
Output current	I_O	± 25	mA
Storage temperature	T_{stg}	-55 to +125	$^{\circ}C$
Soldering condition	T_{sol} T	260/230 20/180	$^{\circ}C$ sec

Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency range	F_O	1.5	—	70	MHz	
Frequency stability	$\Delta F/F_O$	-100	—	100	ppm	*1
Operating temperature	T_{opr}	0	25	70	$^{\circ}C$	
Operating voltage	V_{CC}	4.5	5.0	5.5	V	DC
Operating current	I_{CC}	—	—	*3	mA	$V_{CC} = 5.5V$
Input voltage	V_{IH} V_{IL}	3.5 —	— —	— 1.5	V V	#1: V_{IH} or OPEN \rightarrow Enable #1: V_{IL} or GND \rightarrow Disable
Output voltage	V_{OH} V_{OL}	$V_{CC} - 0.4$ —	— —	— 0.4	V V	$I_{OH} = -4$ mA $I_{OL} = 4$ mA
Symmetry	SYM	40	50	60	%	at 50% V_{CC}
Rise/Fall time	t_r, t_f	—	—	*3	ns	at 10% V_{CC} to 90% V_{CC} / at 90% V_{CC} to 10% V_{CC}
Load capacitance	C_L	—	15	50	pF	1.5 to 26 MHz
		—	15	30	pF	26+ to 46 MHz
		—	—	15	pF	46+ to 70 MHz
Start-up time	t_{st}	—	—	4	ms	1.5 to 26 MHz *2
		—	—	10	ms	26+ to 70 MHz *2

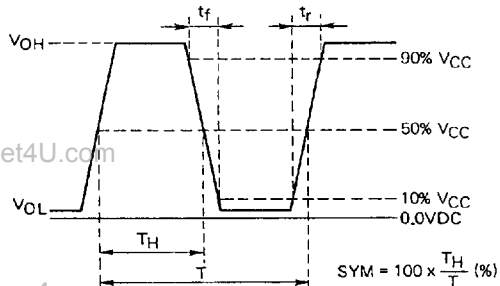
*1 Inclusive of calibration tolerance at 25 $^{\circ}C$, operating temperature, operating voltage range, load change, aging, shock and vibration.

*2 Rise time (0 to 4.5V) of $V_{CC} > 150 \mu s$

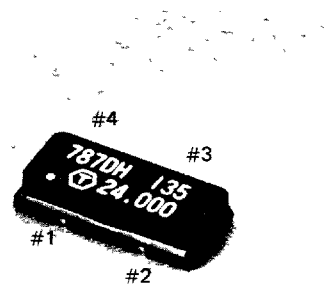
*3

Freq.	1.5 to 10	10+ to 26	26+ to 46	46+ to 70	MHz
I_{CC}	10	15	35	50	mA
t_r, t_f	12	12	10	5	ns

Output waveform



Model TCO-787DH TCO-787DHB



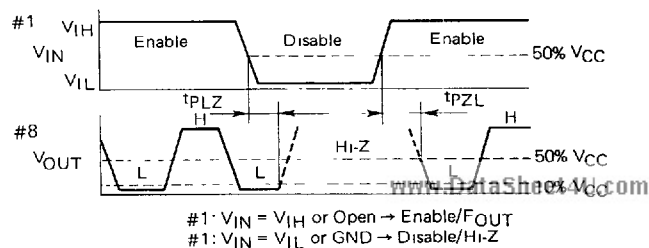
SMO-LN

Dimensions

12.1x5.8x2.5 max. [LN] or 2.7 max. [LB] (mm)
.476x.228x.098 max. [LN] or .106 max. [LB] (inch)

Pin Connections

#4 V_{CC} #3 OUTPUT
#1 E/D #2 GND

Enable/Disable ($t_{PLZ}, t_{PZL} \leq 100$ ns)

#1: $V_{IN} = V_{IH}$ or Open \rightarrow Enable/ F_{OUT}
#1: $V_{IN} = V_{IL}$ or GND \rightarrow Disable/ H_i-Z

Test circuit
See page 11 [4] TEST-4