



STP100NH02L

N-CHANNEL 24V - 0.0052 Ω - 60A TO-220
STripFET™ III POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP100NH02L	24 V	< 0.006 Ω	60 A (2)

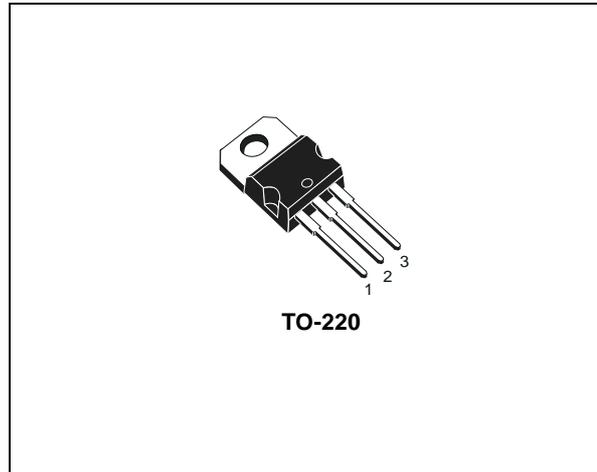
- TYPICAL R_{DS(on)} = 0.0052 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.007 Ω @ 5 V
- R_{DS(ON)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE

DESCRIPTION

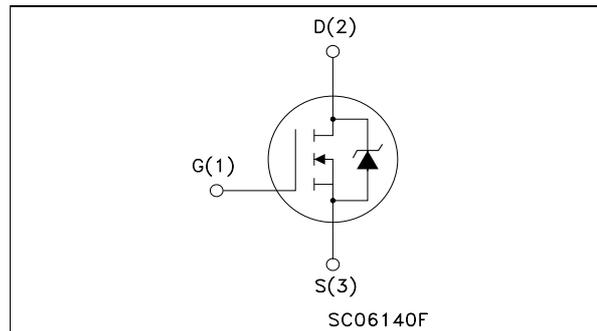
The STP100NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter applications where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP100NH02L	P100NH02L	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{spike(1)}	Drain-source Voltage Rating	30	V
V _{DS}	Drain-source Voltage (V _{GS} = 0)	24	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	24	V
V _{GS}	Gate- source Voltage	\pm 20	V
I _{D(2)}	Drain Current (continuous) at T _C = 25°C	60	A
I _{D(2)}	Drain Current (continuous) at T _C = 100°C	60	A
I _{DM(3)}	Drain Current (pulsed)	240	A
P _{tot}	Total Dissipation at T _C = 25°C	100	W
	Derating Factor	0.67	W/°C
E _{AS(4)}	Single Pulse Avalanche Energy	600	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

STP100NH02L

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 25 mA, V _{GS} = 0	24			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 20 V V _{DS} = 20 V T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (5)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.8		V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 30 A V _{GS} = 5 V I _D = 15 A		0.0052 0.007	0.006 0.011	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (5)	Forward Transconductance	V _{DS} = 10 V I _D = 30 A		40		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 15V f = 1 MHz V _{GS} = 0		2850 800 120		pF pF pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level =20 mV Open Drain		1		Ω

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		13 75		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=10\text{ V}$ $I_D=60\text{ A}$ $V_{GS}=10\text{ V}$		47.5 10 7	64	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		50 18	24.3	ns ns

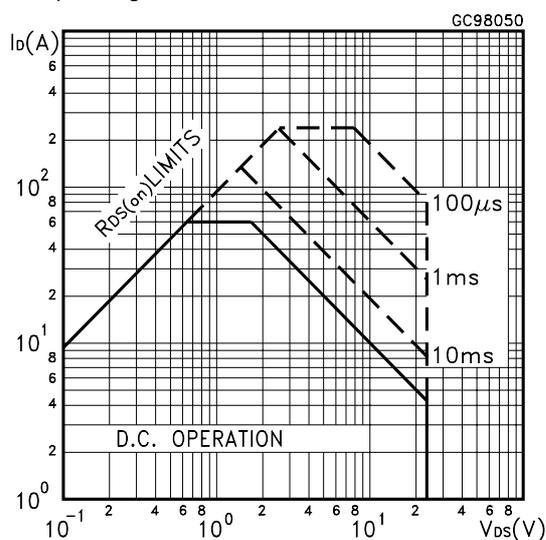
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				60 240	A A
$V_{SD}^{(5)}$	Forward On Voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 16\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		35 35 2		ns nC A

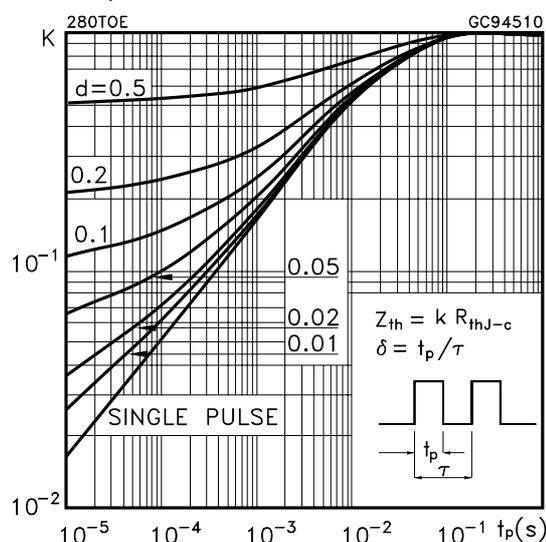
(1) Guaranteed when external $R_g=4.7\ \Omega$ and $t_f < t_{fmax}$.
 (2) Value limited by wire bonding
 (3) Pulse width limited by safe operating area.
 (4) Starting $T_j = 25\ ^\circ\text{C}$, $I_D = 30\text{ A}$, $V_{DD} = 15\text{ V}$

(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (6) $Q_{OSS} = C_{OSS} \cdot \Delta V_{in}$, $C_{OSS} = C_{gd} + C_{ds}$. See Appendix A
 (7) Gate charge for synchronous operation

Safe Operating Area

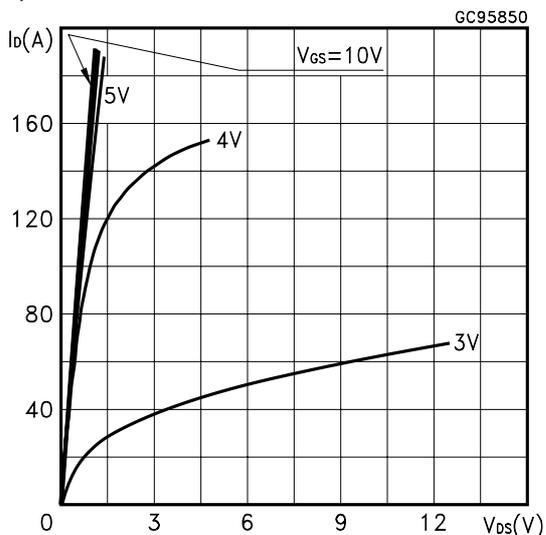


Thermal Impedance

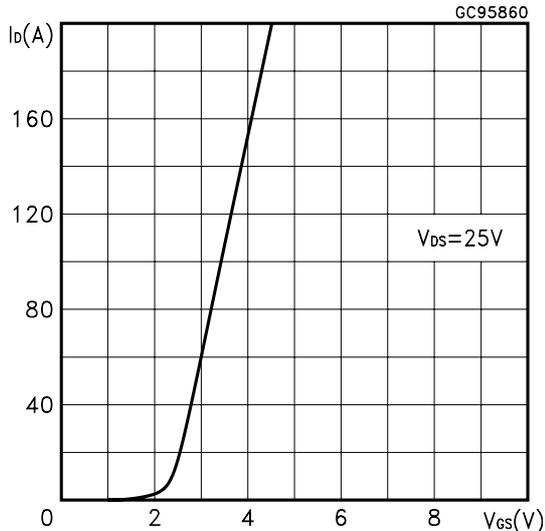


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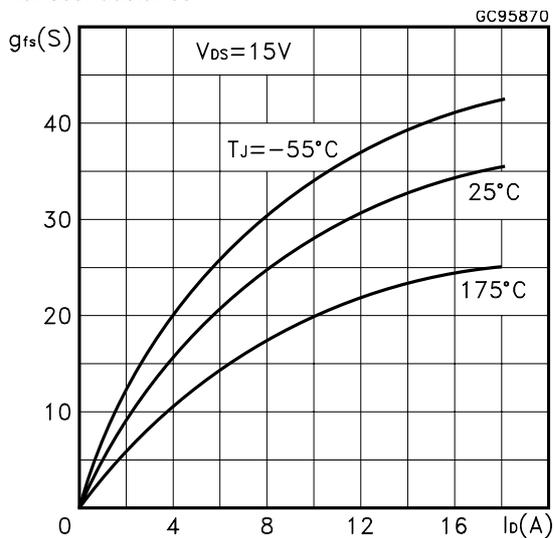
Output Characteristics



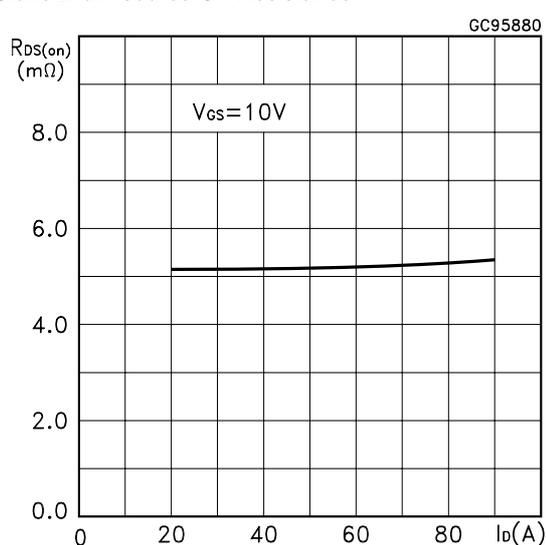
Transfer Characteristics



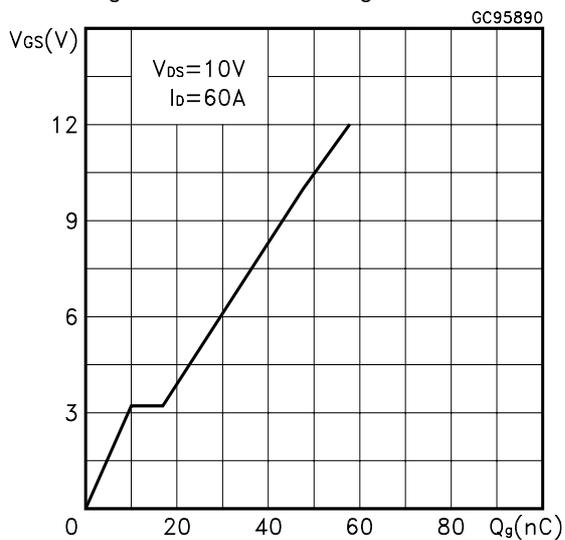
Transconductance



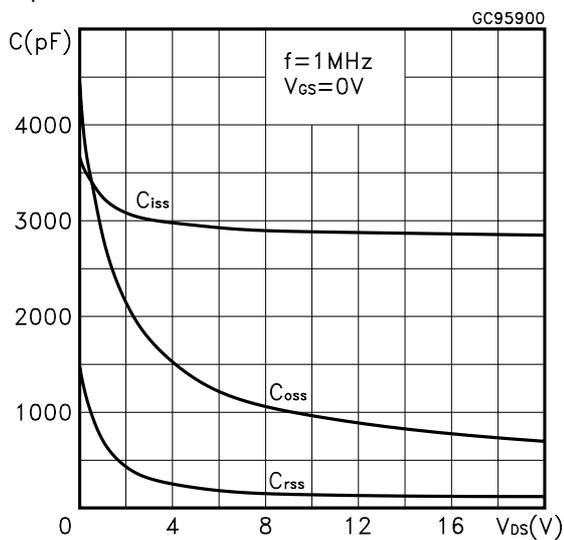
Static Drain-source On Resistance



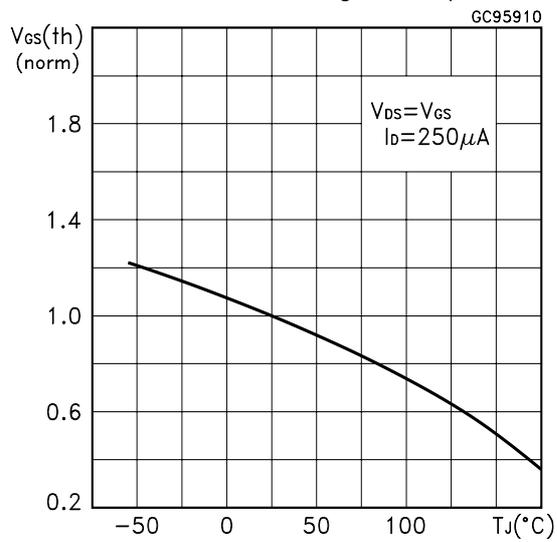
Gate Charge vs Gate-source Voltage



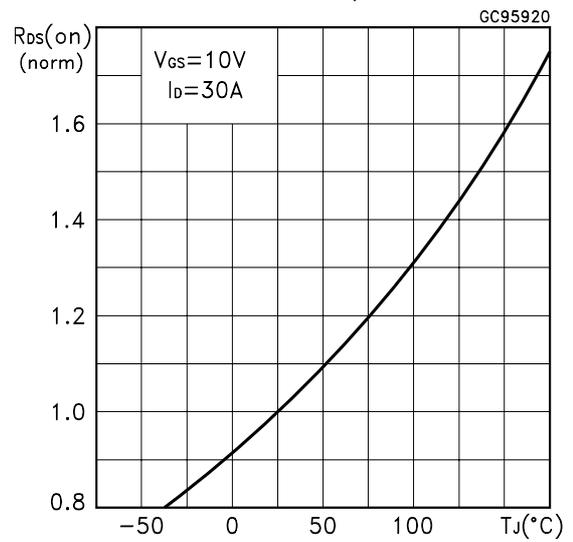
Capacitance Variations



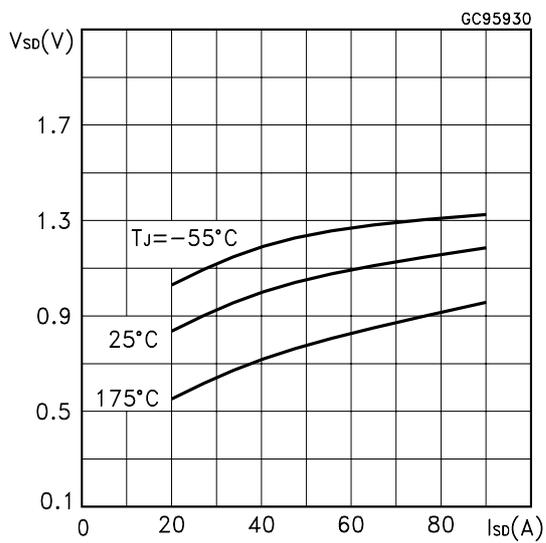
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

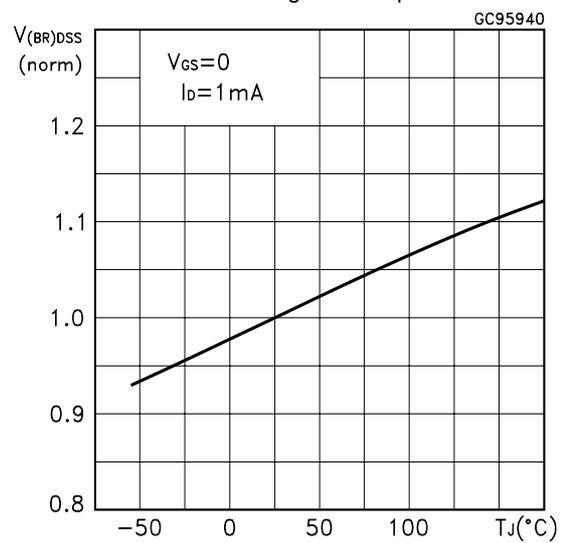


Fig. 1: Unclamped Inductive Load Test Circuit

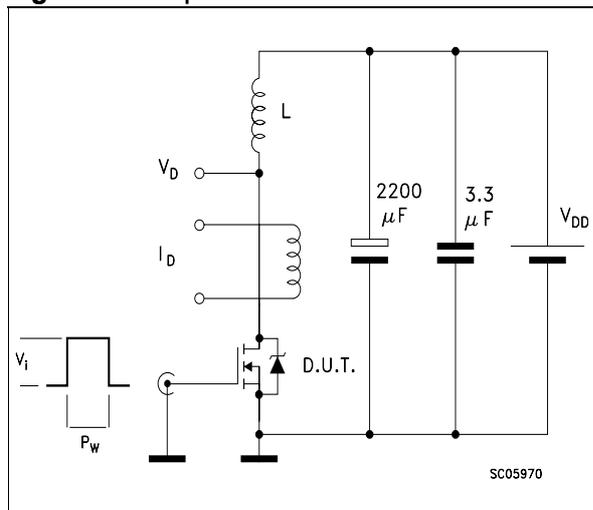


Fig. 2: Unclamped Inductive Waveform

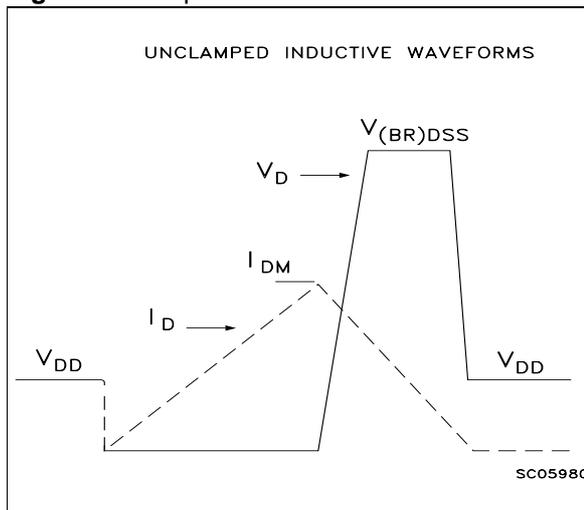


Fig. 3: Switching Times Test Circuits For Resistive Load

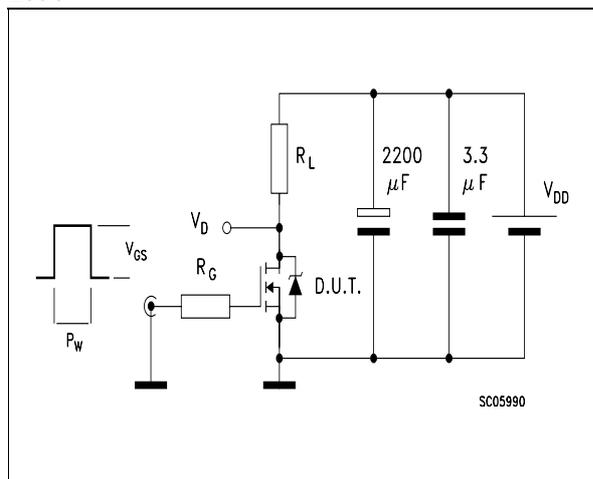


Fig. 4: Gate Charge test Circuit

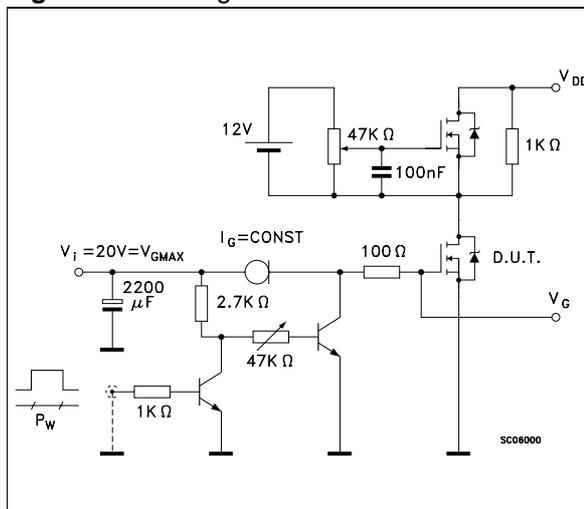
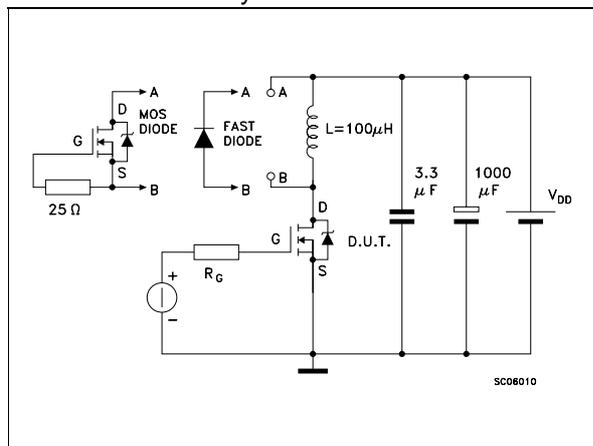
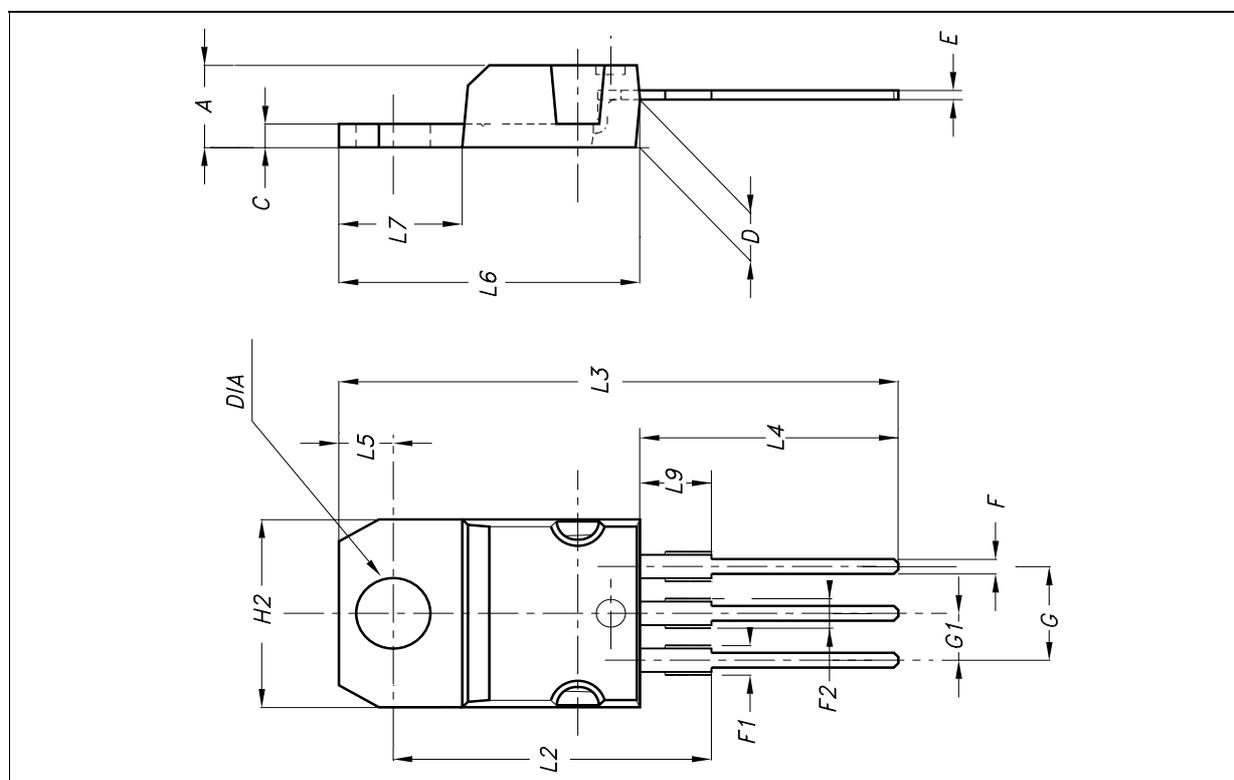


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



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