



LC4132C

Dot Matrix STN LCD Segment Driver

Overview

The LC4132C is a segment driver for large-scale dot matrix LCDs. The LC4132C latches 240 bits of display data sent from the controller (in 4- or 8-bit parallel units) and generates the LCD drive signals. The LC4132C and the LC4102C common driver form a chip set that can drive a large-screen LCD panel.

Features

- CMOS (p-substrate) high voltage process
- LCD drive voltage: 36 V
- Logic system supply voltage: 2.7 to 5.5 V
- fcp max: 12 MHz ($V_{DD} = 5\text{ V} \pm 10\%$), 10 MHz ($V_{DD} = 2.7\text{ to }4.5\text{ V}$)
- Slim chip
- Can be switched between 4-bit and 8-bit parallel input.
- Output direction switching
- Display off function that holds the LCD drive voltages at fixed levels.
- Display duty: 1/160 to 1/480
- Supports COG (chip on glass) mounting. (Gold bump pads are used.)

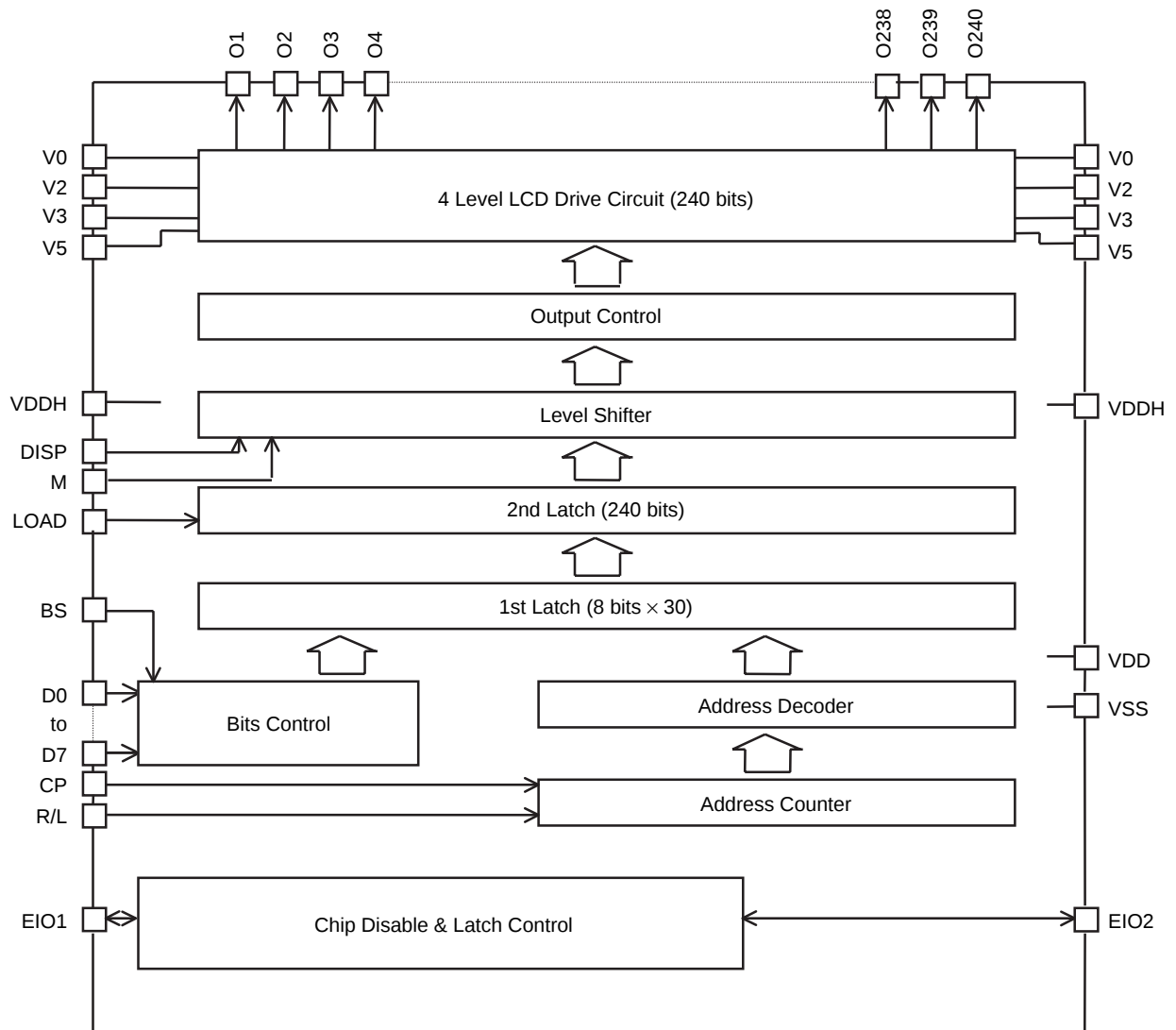
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Block Diagram



LC4132C

The electrical characteristics listed below apply when packaged in the Sanyo PGA-208 package.

Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum supply voltage	$V_{DD\text{ max}}$	V_{DD}	-0.3		7.0	V
	$V_{DDH\text{ max}}$	V_{DDH}	-0.3		40.0	V
	$V_{SS\text{ max}}$	V_{SS}	-0.3		0.3	V
Input voltage	V_{IN}	*1	-0.3		$V_{DD} + 0.3$	V
	V_0, V_2	V_0, V_2 *2	$V_{DDH} - 7.0$		$V_{DDH} + 0.3$	V
	V_3	V_3 *2	-0.3		$V_{SS} + 7.0$	V
	V_5	V_5 *2	-0.3		0.3	V
Operating temperature	T_{opr}		-20		+75	°C
Storage temperature	T_{stg}		-55		+125	°C

Notes: 1. D0 to D7, LOAD, CP, R/L, DISP, M, EIO1, EIO2, BS

2. The following relationships must hold for V_0, V_2, V_3 , and V_5 : $V_{DDH} \geq V_0 \geq V_2 \geq V_{DDH} - 7\text{ V}$, and $7\text{ V} \geq V_3 \geq V_5 \geq V_{SS}$.

Allowable Operating Ranges at $T_a = -20\text{ to }+75^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		5.5	V
	V_{DDH}	V_{DDH}	20		36	V
	V_{SS}	V_{SS}		0		V
Input high-level voltage	V_{IH}	*3	$0.8 V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL}	*3	0		$0.2 V_{DD}$	V
Input voltage	V_0, V_2	V_0, V_2 *4	$V_{DDH} - 7.0$		V_{DDH}	V
	V_3	V_3 *4	0		$V_{SSH} + 7.0$	V
	V_5	V_5 *1		0		V

Notes: 3. D0 to D7, LOAD, CP, R/L, M, DISP, BS, EIO1, EIO2

4. The following relationships must hold for V_0, V_2, V_3 , and V_5 : $V_{DDH} \geq V_0 \geq V_2 \geq V_{DDH} - 7\text{ V}$, and $7\text{ V} \geq V_3 \geq V_5 \geq V_{SS}$.

At power on: The logic system power supply must be applied before the high-voltage system power supply. (Or they must both be applied at the same time.)

At power off: The high-voltage system power supply must be turned off before the logic system power supply. (Or they must both be turned off at the same time.)

$V_{DD} = 5\text{ V} \pm 10\%$, $T_a = -20\text{ to }+75^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	f_{cp}	CP			12	MHz
High-level load pulse width	$t_w(\text{ldH})$	LOAD	50			ns
High-level clock pulse width	$t_w(\text{cpH})$	CP	20			ns
Low-level clock pulse width	$t_w(\text{cpL})$	CP	20			ns
LOAD/CP setup time	$t_{su}(\text{ld})$	LOAD, CP	100			ns
LOAD/CP hold time	$t_{ho}(\text{ld})$	LOAD, CP	200			ns
DATA/CP setup time	$t_{su}(\text{cp})$	CP, D0 to D7	10			ns
DATA/CP hold time	$t_{ho}(\text{cp})$	CP, D0 to D7	10			ns
EIO input setup time	$t_{su}(\text{ei})$	CP, EIO1, EIO2	24			ns
Clock rise time	t_r	LOAD, CP *5			50	ns
Clock fall time	t_f	LOAD, CP *5			50	ns

Note: 5. The clock rise time (t_r) and the clock fall time (t_f) must meet the conditions (1) and (2) shown below.

$$(1) t_r, t_f < \frac{\frac{1}{f_{cp}} - t_w(\text{cpH}) - t_w(\text{cpL})}{2} \quad (2) t_r, t_f \leq 50\text{ ns}$$

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V_{DD} = 2.7 to 4.5 V, T_a = –20 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	f _{cp}	CP			10	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	37			ns
Low-level clock pulse width	tw (cpL)	CP	37			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	350			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	35			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	35			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	30			ns
Clock rise time	tr	LOAD, CP *6			50	ns
Clock fall time	tf	LOAD, CP *6			50	ns

Note: 6. The clock rise time (tr) and the clock fall time (tf) must meet the conditions (1) and (2) shown below.

$$(1) \text{ tr, tf} < \frac{\frac{1}{f_{cp}} - tw(\text{cph}) - tw(\text{cpl})}{2} \quad (2) \text{ tr, tf} \leq 50 \text{ ns}$$

Electrical Characteristics at T_a = –20 to +75°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	I _{IH}	V _{IN} = V _{DD} *7			5	μA
Input low-level voltage	I _{IL} 1	V _{IN} = V _{SS} *7	–5			μA
Output high-level voltage	V _{OH}	I _O = –0.4 mA: EIO1, EIO2	V _{DD} – 0.4		V _{DD}	V
Output low-level voltage	V _{OL}	I _O = 0.4 mA: EIO1, EIO2	V _{SS}		0.4	V
Output on resistance	R _{OUT}	V _{DDH} = 36 V *8 V _O – V _O = 0.5 V, V ₂ – V _O = 0.5 V V _O – V ₃ = 0.5 V, V _O – V ₅ = 0.5 V : O1 to O240		1	3	kΩ
Current drain	I _{DD}	V _{DD} = 2.7 to 5.5 V			5.0	mA
	I _{DDH}	V _{DD} = 2.7 to 5.5 V, V _{DDH} = 32 V *9			3.0	mA
		V _{DD} = 5 V ±10%, V _{DDH} = 36 V			3.0	mA
	I _{ST}	*10			500	μA

Notes: 7. D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, 2, BS

8. V_O is the voltage applied by an on-state output, V_O = V_{DDH}, V₂ = 18/20 (V_{DDH} – V_{SS}), V₃ = 2/20 (V_{DDH} – V_{SS}), V₅ = V_{SS}.

9. Measured when either LOAD = 28 kHz, CP = 10 MHz, and M = 75 Hz, or with no load and input at V_{IH} = V_{DD} or V_{IL} = V_{SS}.

10. The current drain in standby mode. Or when EIO_{on} (input) = V_{DD}.

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Switching Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{ V}$

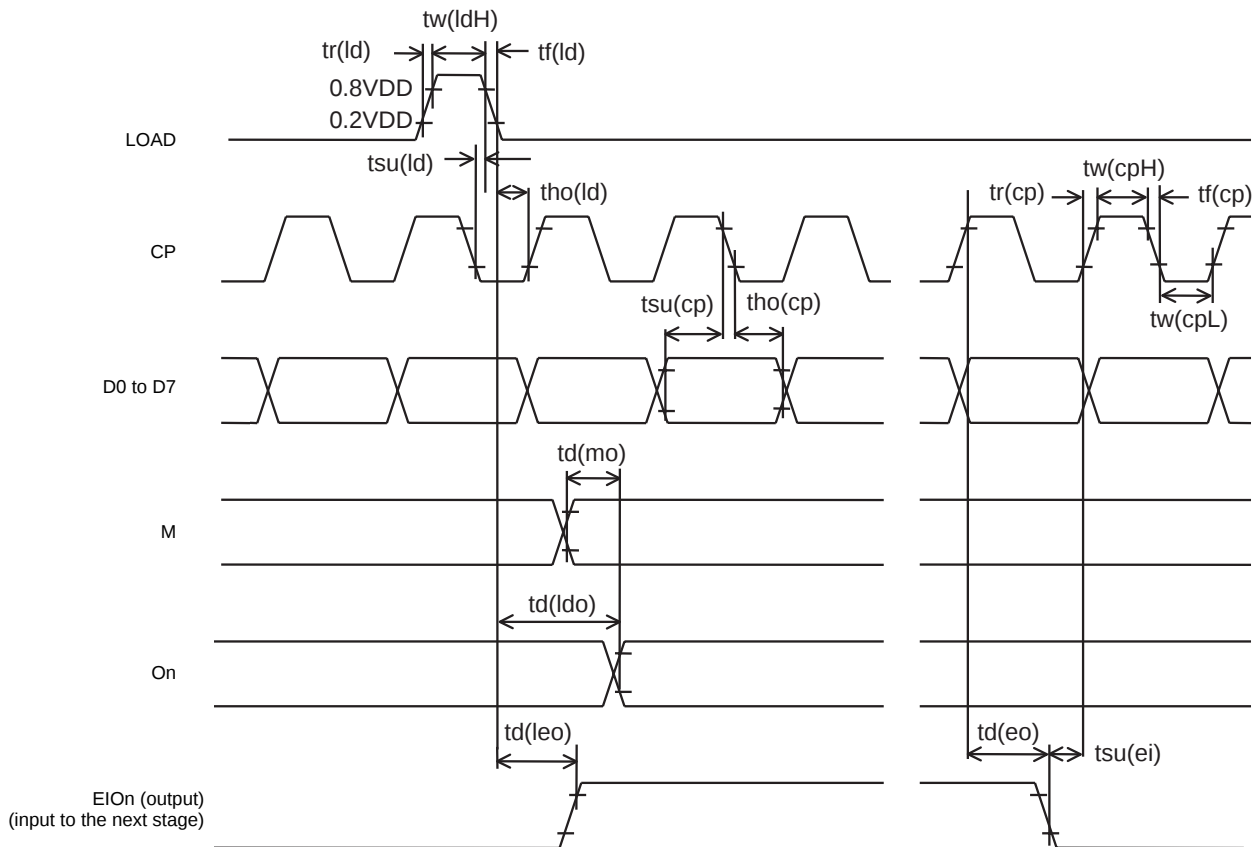
$V_{DD} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	$t_d(\text{eo})$	30 pF capacitance load: CP, EIO1, EIO2			40	ns
LOAD/EIO output delay time	$t_d(\text{leo})$	30 pF capacitance load: LOAD, EIO1, EIO2			70	ns
LOAD/On delay time	$t_d(\text{ldo})$	100 pF capacitance load: LOAD, O1 to O240			700	ns
M/On delay time	$t_d(\text{mo})$	100 pF capacitance load: M, O1 to O240			700	ns

$V_{DD} = 2.5$ to 4.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	$t_d(\text{eo})$	30 pF capacitance load: CP, EIO1, EIO2			80	ns
LOAD/EIO output delay time	$t_d(\text{leo})$	30 pF capacitance load: LOAD, EIO1, EIO2			130	ns
LOAD/On delay time	$t_d(\text{ldo})$	100 pF capacitance load: LOAD, O1 to O240			3	μs
M/On delay time	$t_d(\text{mo})$	100 pF capacitance load: M, O1 to O240			3	μs

Timing Chart ($V_{IH} = 0.8 V_{DD}$, $V_{IL} = 0.2 V_{DD}$)

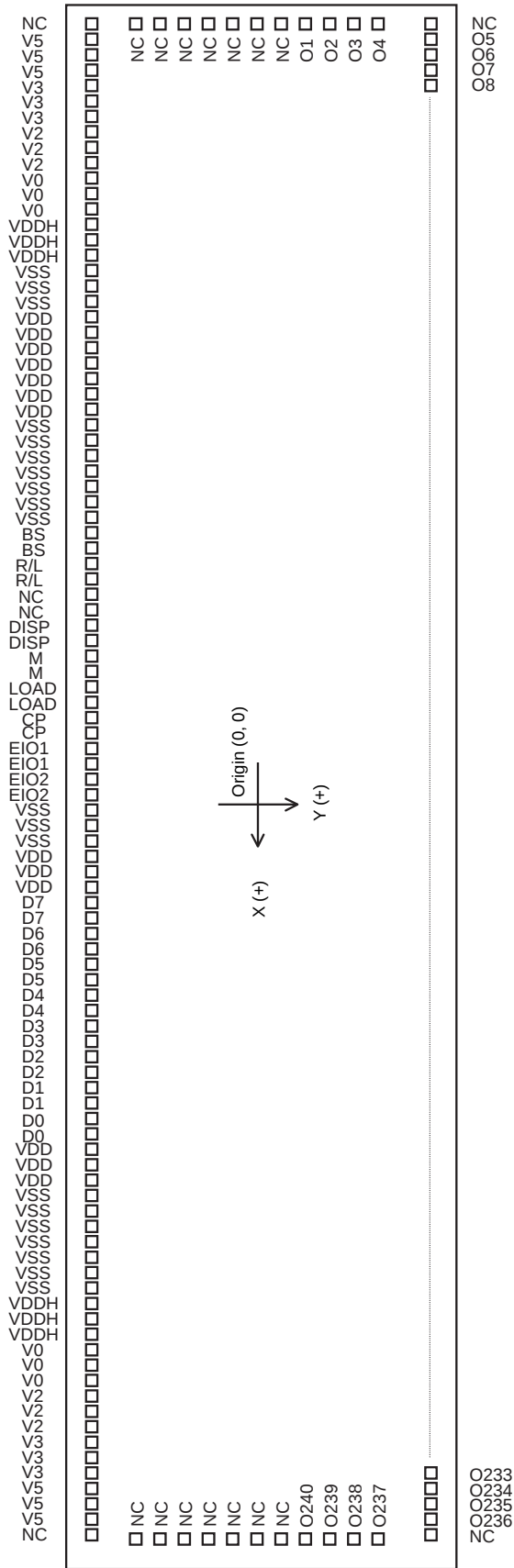


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Pin Functions

Pin	I/O	Function																																																																																																																																																
O1 to O240	O	LCD drive outputs																																																																																																																																																
		<table><tr><td>M</td><td>Data</td><td>DISP</td><td>On</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V0</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V5</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V5</td></tr></table>	M	Data	DISP	On	H	H	H	V0	H	L	H	V2	L	L	H	V3	L	H	H	V5	*	*	L	V5																																																																																																																								
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V _{SS}	—	GND																																																																																																																																																
DISP	I	LCD off function. When this pin is low, all outputs are held at the V5 level.																																																																																																																																																
M	I	Alternation signal input																																																																																																																																																
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Enable input: The enable input at the initial stage is fixed at the V _{SS} level, and the enable inputs of later stages are connected to the enable output from the previous stage. Enable output: When cascade connection is used, the enable output is connected to the enable input of the next stage.																																																																																																																																																		
CP	I	Data acquisition clock (falling edge)																																																																																																																																																
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R/L	I	Data shift direction setting																																																																																																																																																
		<table><tr><th>R/L</th><th>BS</th><th colspan="12">O1 to O240 outputs</th></tr><tr><td rowspan="2">L</td><td rowspan="2">H</td><td>O1</td><td>O2</td><td>O3</td><td>O4</td><td>→</td><td>...</td><td>O237</td><td>O238</td><td>O239</td><td>O240</td></tr><tr><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td></td><td></td><td>↑</td><td>↑</td><td>↑</td><td>↑</td></tr><tr><td rowspan="2">H</td><td rowspan="2">H</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td></td><td></td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>O1</td><td>O2</td><td>O3</td><td>O4</td><td>→</td><td>...</td><td>O237</td><td>O238</td><td>O239</td><td>O240</td></tr><tr><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td></td><td></td><td>↑</td><td>↑</td><td>↑</td><td>↑</td></tr><tr><td rowspan="2">L</td><td rowspan="2">L</td><td>D0</td><td>D1</td><td>D2</td><td>D3</td><td></td><td></td><td>D4</td><td>D5</td><td>D6</td><td>D7</td></tr><tr><td>O1</td><td>O2</td><td>O3</td><td>O4</td><td>→</td><td>...</td><td>O237</td><td>O238</td><td>O239</td><td>O240</td></tr><tr><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td></td><td></td><td>↑</td><td>↑</td><td>↑</td><td>↑</td></tr><tr><td rowspan="2">H</td><td rowspan="2">L</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td><td></td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr><tr><td>O1</td><td>O2</td><td>O3</td><td>O4</td><td>→</td><td>...</td><td>O237</td><td>O238</td><td>O239</td><td>O240</td></tr><tr><td>↑</td><td>↑</td><td>↑</td><td>↑</td><td></td><td></td><td>↑</td><td>↑</td><td>↑</td><td>↑</td></tr><tr><td rowspan="2">H</td><td rowspan="2">L</td><td>D0</td><td>D1</td><td>D2</td><td>D3</td><td></td><td></td><td>D0</td><td>D1</td><td>D2</td><td>D3</td></tr></table>	R/L	BS	O1 to O240 outputs												L	H	O1	O2	O3	O4	→	...	O237	O238	O239	O240	↑	↑	↑	↑			↑	↑	↑	↑	H	H	D7	D6	D5	D4			D3	D2	D1	D0	O1	O2	O3	O4	→	...	O237	O238	O239	O240	↑	↑	↑	↑			↑	↑	↑	↑	L	L	D0	D1	D2	D3			D4	D5	D6	D7	O1	O2	O3	O4	→	...	O237	O238	O239	O240	↑	↑	↑	↑			↑	↑	↑	↑	H	L	D3	D2	D1	D0			D3	D2	D1	D0	O1	O2	O3	O4	→	...	O237	O238	O239	O240	↑	↑	↑	↑			↑	↑	↑	↑	H	L	D0	D1	D2	D3			D0	D1	D2	D3
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D0 to D7	I	Parallel data inputs																																																																																																																																																
BS	I	Input bus width setting. A high level selects 8-bit input, and a low level selects 4-bit input. In 4-bit input mode, D0 to D3 are used for data acquisition and D4 to D7 must be tied to ground.																																																																																																																																																

Pad Assignment



Chip size: 15.7 × 2.0 mm

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LC4132C Pad Coordinates

Pin	X coordinate	Y coordinate	Bump type	Pin	X coordinate	Y coordinate	Bump type
NC	-7687.0	-794.0	D	V _{SS}	-172.0	-806.0	A
V5	-7587.0	-794.0	A	V _{SS}	7.0	-806.0	A
V5	-7487.0	-794.0	A	V _{SS}	186.0	-806.0	A
V5	-7387.0	-794.0	A	V _{DD}	365.0	-806.0	A
V3	-7287.0	-794.0	A	V _{DD}	544.0	-806.0	A
V3	-7187.0	-794.0	A	V _{DD}	723.0	-806.0	A
V3	-7087.0	-794.0	A	D7	949.0	-806.0	A
V2	-6987.0	-794.0	A	D7	1174.0	-806.0	A
V2	-6887.0	-794.0	A	D6	1399.0	-806.0	A
V2	-6787.0	-794.0	A	D6	1624.0	-806.0	A
V0	-6687.0	-794.0	A	D5	1849.0	-806.0	A
V0	-6587.0	-794.0	A	D5	2074.0	-806.0	A
V0	-6487.0	-794.0	A	D4	2299.0	-806.0	A
V _{DDH}	-6387.0	-794.0	A	D4	2524.0	-806.0	A
V _{DDH}	-6287.0	-794.0	A	D3	2749.0	-806.0	A
V _{DDH}	-6187.0	-794.0	A	D3	2974.0	-806.0	A
V _{SS}	-6087.0	-794.0	A	D2	3199.0	-806.0	A
V _{SS}	-5987.0	-794.0	A	D2	3424.0	-806.0	A
V _{SS}	-5887.0	-794.0	A	D1	3649.0	-806.0	A
V _{DD}	-5787.0	-794.0	A	D1	3874.0	-806.0	A
V _{DD}	-5687.0	-794.0	A	D0	4099.0	-806.0	A
V _{DD}	-5587.0	-794.0	A	D0	4324.0	-806.0	A
V _{DD}	-5487.0	-794.0	A	V _{DD}	4446.2	-794.0	A
V _{DD}	-5387.0	-794.0	A	V _{DD}	4646.2	-749.0	A
V _{DD}	-5287.0	-794.0	A	V _{DD}	4846.2	-794.0	A
V _{DD}	-5187.0	-794.0	A	V _{SS}	5046.2	-794.0	A
V _{SS}	-5087.0	-794.0	A	V _{SS}	5246.2	-794.0	A
V _{SS}	-4987.0	-794.0	A	V _{SS}	5446.2	-794.0	A
V _{SS}	-4887.0	-794.0	A	V _{SS}	5646.2	-794.0	A
V _{SS}	-4787.0	-794.0	A	V _{SS}	5887.0	-794.0	A
V _{SS}	-4687.0	-794.0	A	V _{SS}	5987.0	-794.0	A
V _{SS}	-4587.0	-794.0	A	V _{SS}	6087.0	-794.0	A
V _{SS}	-4487.0	-794.0	A	V _{DDH}	6187.0	-794.0	A
BS	-4161.3	-806.0	A	V _{DDH}	6287.0	-794.0	A
BS	-3936.4	-806.0	A	V _{DDH}	6387.0	-794.0	A
R/L	-3711.3	-806.0	A	V0	6487.0	-794.0	A
R/L	-3486.4	-806.0	A	V0	6587.0	-794.0	A
NC	-3261.3	-806.0	A	V0	6687.0	-794.0	A
NC	-3036.4	-806.0	A	V2	6787.0	-794.0	A
DISP	-2811.3	-806.0	A	V2	6887.0	-794.0	A
DISP	-2586.4	-806.0	A	V2	6987.0	-794.0	A
M	-2361.3	-806.0	A	V3	7087.0	-794.0	A
M	-2136.4	-806.0	A	V3	7187.0	-794.0	A
LOAD	-1911.3	-806.0	A	V3	7287.0	-794.0	A
LOAD	-1686.4	-806.0	A	V5	7387.0	-794.0	A
CP	-1461.3	-806.0	A	V5	7487.0	-794.0	A
CP	-1236.4	-806.0	A	V5	7587.0	-794.0	A
EIO1	-1011.3	-806.0	A	NC	7687.0	-794.0	D
EIO1	-786.4	-806.0	A				
EIO2	-561.3	-806.0	A				
EIO2	-336.4	-806.0	A				

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Pin	X coordinate	Y coordinate	Bump type	Pin	X coordinate	Y coordinate	Bump type
NC	-7676.0	-666.0	B	O36	-5577.0	829.0	C
NC	-7676.0	-534.0	B	O37	-5511.0	829.0	C
NC	-7676.0	-402.0	B	O38	-5445.0	829.0	C
NC	-7676.0	-270.0	B	O39	-5379.0	829.0	C
NC	-7676.0	-138.0	B	O40	-5313.0	829.0	C
NC	-7676.0	-6.0	B	O41	-5247.0	829.0	C
NC	-7676.0	126.0	B	O42	-5181.0	829.0	C
O1	-7676.0	258.0	B	O43	-5115.0	829.0	C
O2	-7676.0	390.0	B	O44	-5049.0	829.0	C
O3	-7676.0	522.0	B	O45	-4983.0	829.0	C
O4	-7676.0	654.0	B	O46	-4917.0	829.0	C
NC	-7689.0	829.0	C	O47	-4851.0	829.0	C
O5	-7623.0	829.0	C	O48	-4785.0	829.0	C
O6	-7557.0	829.0	C	O49	-4719.0	829.0	C
O7	-7491.0	829.0	C	O50	-4653.0	829.0	C
O8	-7425.0	829.0	C	O51	-4587.0	829.0	C
O9	-7359.0	829.0	C	O52	-4521.0	829.0	C
O10	-7293.0	829.0	C	O53	-4455.0	829.0	C
O11	-7227.0	829.0	C	O54	-4389.0	829.0	C
O12	-7161.0	829.0	C	O55	-4323.0	829.0	C
O13	-7095.0	829.0	C	O56	-4257.0	829.0	C
O14	-7029.0	829.0	C	O57	-4191.0	829.0	C
O15	-6963.0	829.0	C	O58	-4125.0	829.0	C
O16	-6897.0	829.0	C	O59	-4059.0	829.0	C
O17	-6831.0	829.0	C	O60	-3993.0	829.0	C
O18	-6765.0	829.0	C	O61	-3927.0	829.0	C
O19	-6699.0	829.0	C	O62	-3861.0	829.0	C
O20	-6633.0	829.0	C	O63	-3795.0	829.0	C
O21	-6567.0	829.0	C	O64	-3729.0	829.0	C
O22	-6501.0	829.0	C	O65	-3663.0	829.0	C
O23	-6435.0	829.0	C	O66	-3597.0	829.0	C
O24	-6369.0	829.0	C	O67	-3531.0	829.0	C
O25	-6303.0	829.0	C	O68	-3465.0	829.0	C
O26	-6237.0	829.0	C	O69	-3399.0	829.0	C
O27	-6171.0	829.0	C	O70	-3333.0	829.0	C
O28	-6105.0	829.0	C	O71	-3267.0	829.0	C
O29	-6039.0	829.0	C	O72	-3201.0	829.0	C
O30	-5973.0	829.0	C	O73	-3135.0	829.0	C
O31	-5907.0	829.0	C	O74	-3069.0	829.0	C
O32	-5841.0	829.0	C	O75	-3003.0	829.0	C
O33	-5775.0	829.0	C	O76	-2937.0	829.0	C
O34	-5709.0	829.0	C	O77	-2871.0	829.0	C
O35	-5643.0	829.0	C	O78	-2805.0	829.0	C

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Pin	X coordinate	Y coordinate	Bump type	Pin	X coordinate	Y coordinate	Bump type
O79	-2739.0	829.0	C	O122	99.0	829.0	C
O80	-2673.0	829.0	C	O123	165.0	829.0	C
O81	-2607.0	829.0	C	O124	231.0	829.0	C
O82	-2541.0	829.0	C	O125	297.0	829.0	C
O83	-2475.0	829.0	C	O126	363.0	829.0	C
O84	-2409.0	829.0	C	O127	429.0	829.0	C
O85	-2343.0	829.0	C	O128	495.0	829.0	C
O86	-2277.0	829.0	C	O129	561.0	829.0	C
O87	-2211.0	829.0	C	O130	627.0	829.0	C
O88	-2145.0	829.0	C	O131	693.0	829.0	C
O89	-2079.0	829.0	C	O132	759.0	829.0	C
O90	-2013.0	829.0	C	O133	825.0	829.0	C
O91	-1947.0	829.0	C	O134	891.0	829.0	C
O92	-1881.0	829.0	C	O135	957.0	829.0	C
O93	-1815.0	829.0	C	O136	1023.0	829.0	C
O94	-1749.0	829.0	C	O137	1089.0	829.0	C
O95	-1683.0	829.0	C	O138	1155.0	829.0	C
O96	-1617.0	829.0	C	O139	1221.0	829.0	C
O97	-1551.0	829.0	C	O140	1287.0	829.0	C
O98	-1485.0	829.0	C	O141	1353.0	829.0	C
O99	-1419.0	829.0	C	O142	1419.0	829.0	C
O100	-1353.0	829.0	C	O143	1485.0	829.0	C
O101	-1287.0	829.0	C	O144	1551.0	829.0	C
O102	-1221.0	829.0	C	O145	1617.0	829.0	C
O103	-1155.0	829.0	C	O146	1683.0	829.0	C
O104	-1089.0	829.0	C	O147	1749.0	829.0	C
O105	-1023.0	829.0	C	O148	1815.0	829.0	C
O106	-957.0	829.0	C	O149	1881.0	829.0	C
O107	-891.0	829.0	C	O150	1947.0	829.0	C
O108	-825.0	829.0	C	O151	2013.0	829.0	C
O109	-759.0	829.0	C	O152	2079.0	829.0	C
O110	-693.0	829.0	C	O153	2145.0	829.0	C
O111	-627.0	829.0	C	O154	2211.0	829.0	C
O112	-561.0	829.0	C	O155	2277.0	829.0	C
O113	-495.0	829.0	C	O156	2343.0	829.0	C
O114	-429.0	829.0	C	O157	2409.0	829.0	C
O115	-363.0	829.0	C	O158	2475.0	829.0	C
O116	-297.0	829.0	C	O159	2541.0	829.0	C
O117	-231.0	829.0	C	O160	2607.0	829.0	C
O118	-165.0	829.0	C	O161	2673.0	829.0	C
O119	-99.0	829.0	C	O162	2739.0	829.0	C
O120	-33.0	829.0	C	O163	2805.0	829.0	C
O121	33.0	829.0	C	O164	2871.0	829.0	C

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Pin	X coordinate	Y coordinate	Bump type	Pin	X coordinate	Y coordinate	Bump type
O165	2937.0	829.0	C	O208	5775.0	829.0	C
O166	3003.0	829.0	C	O209	5841.0	829.0	C
O167	3069.0	829.0	C	O210	5907.0	829.0	C
O168	3135.0	829.0	C	O211	5973.0	829.0	C
O169	3201.0	829.0	C	O212	6039.0	829.0	C
O170	3267.0	829.0	C	O213	6105.0	829.0	C
O171	3333.0	829.0	C	O214	6171.0	829.0	C
O172	3399.0	829.0	C	O215	6237.0	829.0	C
O173	3465.0	829.0	C	O216	6303.0	829.0	C
O174	3531.0	829.0	C	O217	6369.0	829.0	C
O175	3597.0	829.0	C	O218	6435.0	829.0	C
O176	3663.0	829.0	C	O219	6501.0	829.0	C
O177	3729.0	829.0	C	O220	6567.0	829.0	C
O178	3795.0	829.0	C	O221	6633.0	829.0	C
O179	3861.0	829.0	C	O222	6699.0	829.0	C
O180	3927.0	829.0	C	O223	6765.0	829.0	C
O181	3993.0	829.0	C	O224	6831.0	829.0	C
O182	4059.0	829.0	C	O225	6897.0	829.0	C
O183	4125.0	829.0	C	O226	6963.0	829.0	C
O184	4191.0	829.0	C	O227	7029.0	829.0	C
O185	4257.0	829.0	C	O228	7095.0	829.0	C
O186	4323.0	829.0	C	O229	7161.0	829.0	C
O187	4389.0	829.0	C	O230	7227.0	829.0	C
O188	4455.0	829.0	C	O231	7293.0	829.0	C
O189	4521.0	829.0	C	O232	7359.0	829.0	C
O190	4587.0	829.0	C	O233	7425.0	829.0	C
O191	4653.0	829.0	C	O234	7491.0	829.0	C
O192	4719.0	829.0	C	O235	7557.0	829.0	C
O193	4785.0	829.0	C	O236	7623.0	829.0	C
O194	4851.0	829.0	C	NC	7689.0	829.0	C
O195	4917.0	829.0	C	O237	7676.0	654.0	B
O196	4983.0	829.0	C	O238	7676.0	522.0	B
O197	5049.0	829.0	C	O239	7676.0	390.0	B
O198	5115.0	829.0	C	O240	7676.0	258.0	B
O199	5181.0	829.0	C	NC	7676.0	126.0	B
O200	5247.0	829.0	C	NC	7676.0	-6.0	B
O201	5313.0	829.0	C	NC	7676.0	-138.0	B
O202	5379.0	829.0	C	NC	7676.0	-270.0	B
O203	5445.0	829.0	C	NC	7676.0	-402.0	B
O204	5511.0	829.0	C	NC	7676.0	-534.0	B
O205	5577.0	829.0	C	NC	7676.0	-666.0	B
O206	5643.0	829.0	C				
O207	5709.0	829.0	C				

Bump type	Size (X, Y)
A	60 μm $\times$ 60 μm
B	75 μm $\times$ 48 μm
C	48 μm $\times$ 75 μm
D	72 μm $\times$ 72 μm

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