

FEATURES

- 4 A peak output current**
- Working voltage**
 - High-side or low-side relative to input: $565 V_{DC\ PEAK}$
 - High-side to low-side differential: $700 V_{DC\ PEAK}$
- High frequency operation: 1 MHz maximum**
- 3.3 V to 5 V CMOS input logic**
- 4.5 V to 18 V output drive**
- UVLO at $2.5 V_{DD1}$**
 - ADuM3223A/ADuM4223A UVLO at $4.1 V_{DD2}$
 - ADuM3223B/ADuM4223B UVLO at $7.0 V_{DD2}$
 - ADuM3223C/ADuM4223C UVLO at $11.0 V_{DD2}$
- Precise timing characteristics**
 - 49 ns maximum isolator and driver propagation delay
 - 5 ns maximum channel-to-channel matching
- CMOS input logic levels**
- High common-mode transient immunity: $>50\text{ kV}/\mu\text{s}$**
- Enhanced system-level ESD performance per IEC 61000-4-x**
- High junction temperature operation: 125°C**
- Default low output**
- Safety and regulatory approvals (pending)**
 - ADuM3223 narrow body, 16-lead SOIC
 - UL 1577 3000 V rms input-to-output withstand voltage
 - ADuM4223 wide body, 16-lead SOIC
 - UL 1577 5000 V rms input-to-output withstand voltage

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters

GENERAL DESCRIPTION

The ADuM3223/ADuM4223¹ are 4 A isolated, half-bridge gate drivers that employ the Analog Devices, Inc., *iCoupler*[®] technology to provide independent and isolated high-side and low-side outputs. The ADuM3223 provides 3000 V rms isolation in the narrow body, 16-lead SOIC package, and the ADuM4223 provides 5000 V rms isolation in the wide body, 16-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The ADuM3223/ADuM4223 isolators each provide two independent isolated channels. They operate with an input supply ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM3223/ADuM4223 offer the benefit of true, galvanic isolation between the input and each output. Each output may be continuously operated up to $560 V_{PEAK}$ relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side may be as high as $700 V_{PEAK}$.

As a result, the ADuM3223/ADuM4223 provide reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

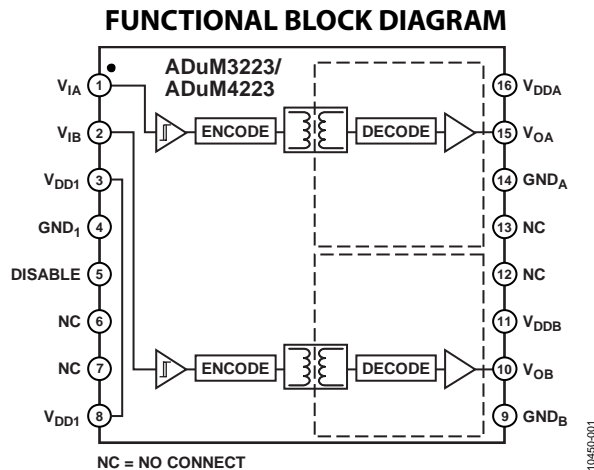


Figure 1.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. 0

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REVISION HISTORY

5/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. $4.5 \text{ V} \leq V_{DD1} \leq 5.5 \text{ V}$, $4.5 \text{ V} \leq V_{DD2} \leq 18 \text{ V}$, unless stated otherwise. All minimum/maximum specifications apply over $T_j = -40^\circ\text{C}$ to 125°C . All typical specifications are at $T_j = 25^\circ\text{C}$, $V_{DD1} = 5 \text{ V}$, $V_{DD2} = 12 \text{ V}$. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1(Q)}$		1.4	2.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.6	2.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA}/I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	-1	+0.01	+1	μA	$0 \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	V_{DD2}		V	$I_{Ox} = -20 \text{ mA}$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	$I_{Ox} = +20 \text{ mA}$, $V_{Ix} = V_{IxL}$
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A-grade
Hysteresis	V_{DD2UVH}		0.5		V	A-grade
Positive Going Threshold	V_{DD2UV+}		6.9	7.4	V	B-grade
Negative Going Threshold	V_{DD2UV-}	5.7	6.2		V	B-grade
Hysteresis	V_{DD2UVH}		0.7		V	B-grade
Positive Going Threshold	V_{DD2UV+}		10.5	11.1	V	C-grade
Negative Going Threshold	V_{DD2UV-}	8.9	9.6		V	C-grade
Hysteresis	V_{DD2UVH}		0.9		V	C-grade
Output Short-Circuit Pulsed Current ¹	$I_{OA(SC)}, I_{OB(SC)}$	2.0	4.0		A	$V_{DD2} = 12 \text{ V}$
Output Pulsed Source Resistance	R_{OA}, R_{OB}		1.1		Ω	$V_{DD2} = 12 \text{ V}$
Output Pulsed Sink Resistance	R_{OA}, R_{OB}		0.6		Ω	$V_{DD2} = 12 \text{ V}$
SWITCHING SPECIFICATIONS						
Pulse Width ²	PW	50			ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$
Maximum Data Rate ³		1			MHz	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$
Propagation Delay ⁴	t_{DHL}, t_{DLH}	26	38	49	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$; see Figure 20
ADuM3223A/ADuM4223A	t_{DHL}, t_{DLH}	30	42	54	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 4.5 \text{ V}$; see Figure 20
Propagation Delay Skew ⁵	t_{PSK}			12	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$; see Figure 20
Channel-to-Channel Matching ⁶	t_{PSKCD}		1	5	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$; see Figure 20
	t_{PSKCD}		1	7	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 4.5 \text{ V}$; see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	18	ns	$C_L = 2 \text{ nF}$, $V_{DD2} = 12 \text{ V}$; see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	$V_{DD2} = 12 \text{ V}$
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	$V_{DD2} = 12 \text{ V}$
Refresh Rate	f_r		1.2		Mbps	

¹ Short-circuit duration less than 1 μs . Average power must conform to the limit shown under the Absolute Maximum Ratings.

² The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.

⁴ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.

⁶ Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 18\text{ V}$, unless stated otherwise. All minimum/maximum specifications apply over $T_j = -40^\circ\text{C}$ to 125°C . All typical specifications are at $T_j = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 12\text{ V}$. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1(Q)}$		0.87	1.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DDO(Q)}$		2.3	3.2	mA	
Supply Current at 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.1	1.5	mA	Up to 1 MHz, no load
V_{DDA}/V_{DDB} Supply Current	$I_{DDA}/I_{DDB(Q)}$		5.6	8.0	mA	Up to 1 MHz, no load
Input Currents	I_{IA}, I_{IB}	-10	+0.01	+10	μA	$0 \leq V_{IA}, V_{IB} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	$V_{DD2} - 0.1$	V_{DD2}		V	$I_{Ox} = -20\text{ mA}$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	$I_{Ox} = +20\text{ mA}$, $V_{Ix} = V_{IxL}$
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		4.1	4.4	V	A-grade
Negative Going Threshold	V_{DD2UV-}	3.2	3.6		V	A-grade
Hysteresis	V_{DD2UVH}		0.5		V	A-grade
Positive Going Threshold	V_{DD2UV+}		6.9	7.4	V	B-grade
Negative Going Threshold	V_{DD2UV-}	5.7	6.2		V	B-grade
Hysteresis	V_{DD2UVH}		0.7		V	B-grade
Positive Going Threshold	V_{DD2UV+}		10.5	11.1	V	C-grade
Negative Going Threshold	V_{DD2UV-}	8.9	9.6		V	C-grade
Hysteresis	V_{DD2UVH}		0.9		V	C-grade
Output Short-Circuit Pulsed Current ¹	$I_{OA(SC)}, I_{OB(SC)}$	2.0	4.0		A	$V_{DD2} = 12\text{ V}$
Output Pulsed Source Resistance	R_{OA}, R_{OB}		1.1		Ω	$V_{DD2} = 12\text{ V}$
Output Pulsed Sink Resistance	R_{OA}, R_{OB}		0.6		Ω	$V_{DD2} = 12\text{ V}$
SWITCHING SPECIFICATIONS						
Pulse Width ²	PW	50			ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$
Maximum Data Rate ³		1			MHz	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$
Propagation Delay ⁴	t_{DHL}, t_{DLH}	30	42	54	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
ADuM3223A/ADuM4223A	t_{DHL}, t_{DLH}	32	46	60	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 4.5\text{ V}$, see Figure 20
Propagation Delay Skew ⁵	t_{PSK}			12	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
Channel-to-Channel Matching ⁶	t_{PSKCD}		1	5	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
	t_{PSKCD}		1	7	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 4.5\text{ V}$, see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	6	12	22	ns	$C_L = 2\text{ nF}$, $V_{DD2} = 12\text{ V}$, see Figure 20
Dynamic Input Supply Current Per Channel	$I_{DD1(D)}$		0.05		mA/Mbps	$V_{DD2} = 12\text{ V}$
Dynamic Output Supply Current Per Channel	$I_{DDO(D)}$		1.65		mA/Mbps	$V_{DD2} = 12\text{ V}$
Refresh Rate	f_r		1.1		Mbps	

¹ Short-circuit duration less than 1 μs . Average power must conform to the limit shown under the Absolute Maximum Ratings.

² The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.

⁴ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.

⁶ Channel-to-channel matching is the absolute value of the difference in propagation delays between the two channels.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)	R_{I-O}		10 ¹²		Ω	f = 1 MHz
Capacitance (Input-to-Output)	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance						
ADuM3223	θ_{JA}		76		°C/W	
ADuM4223	θ_{JA}		45		°C/W	
IC Junction-to-Case Thermal Resistance						
ADuM3223	θ_{JC}		42		°C/W	
ADuM4223	θ_{JC}		29		°C/W	

INSULATION AND SAFETY-RELATED SPECIFICATIONS**ADuM3223**

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

ADuM4223

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

REGULATORY INFORMATION

The [ADuM3223](#) approval is pending by the organizations listed in Table 6.

Table 6.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ²
Single/Protection 3000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

¹ In accordance with UL 1577, each ADuM3223 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 second (current leakage detection limit = 6 μ A).

² In accordance with DIN V VDE V 0884-10, each ADuM3223 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

The [ADuM4223](#) approval is pending by the organizations listed in Table 7.

Table 7.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ²
Single/Protection 5000 V rms Isolation Voltage	Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Basic insulation per CSA 60950-1-07 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0001

¹ In accordance with UL 1577, each ADuM4223 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μ A).

² In accordance with DIN V VDE V 0884-10, each ADuM4223 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 8. ADuM3223 VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Highest Allowable Overvoltage		V_{IOTM}	4000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μ s rise time, 50 μ s, 50% fall time	V_{IOSM}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	$^{\circ}$ C
Safety Total Dissipated Power		P_S	1.64	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

Table 9. ADuM4223 VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$		
After Environmental Tests Subgroup 1			1273	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μ s rise time, 50 μ s, 50% fall time	V_{IOSM}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	$^{\circ}$ C
Safety Total Dissipated Power		P_S	2.77	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

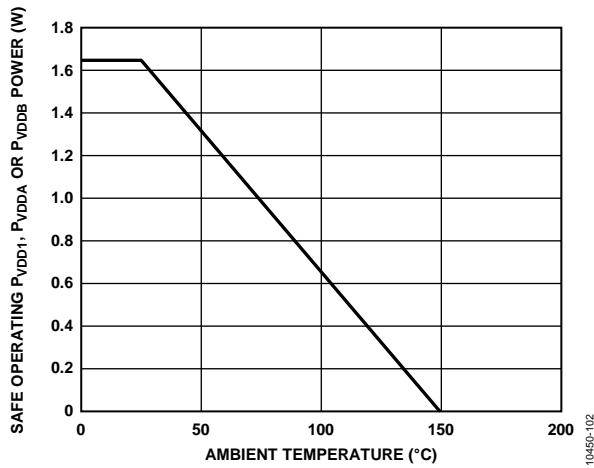


Figure 2. ADuM3223 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

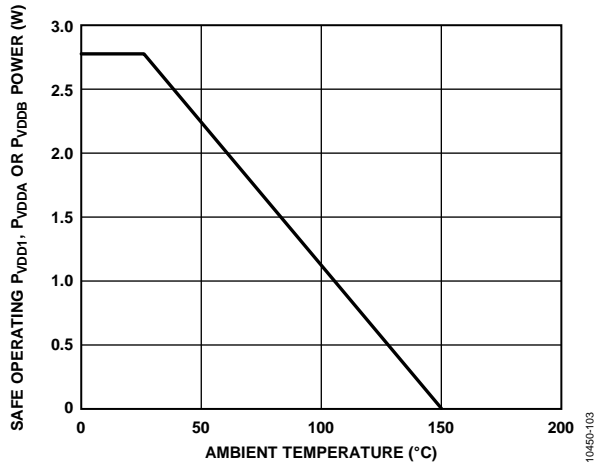


Figure 3. ADuM4223 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 10.

Parameter	Symbol	Min	Max	Unit
Operating Junction Temperature	T_J	-40	+125	°C
Supply Voltages ¹				
	V_{DD1}	3.0	5.5	V
	V_{DDA}, V_{DDB}	4.5	18	V
V_{DD1} Rise Time	T_{VDD1}		1	V/μs
Maximum Input Signal Rise and Fall Times	T_{VIA}, T_{VIB}		1	ms
Common-Mode Transient Immunity, Input to Output		-50	+50	kV/μs
Common-Mode Transient Immunity, Between Outputs		-50	+50	kV/μs

¹ All voltages are relative to their respective ground. See the Applications Information section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 11.

Parameter	Symbol	Rating
Storage Temperature	T_{ST}	-55 °C to +150 °C
Operating Junction Temperature	T_J	-40 °C to +150 °C
Supply Voltages ¹	V_{DD1}	-0.5 V to +7.0 V
	V_{DDA}, V_{DDB}	-0.5 V to +20 V
Input Voltage ¹	V_{IA}, V_{IB} DISABLE	-0.5 V to $V_{DD1} + 0.5$ V
Output Voltage ¹	V_{OA} V_{OB}	-0.5 V to $V_{DDA} + 0.5$ V -0.5 V to $V_{DDB} + 0.5$ V
Average Output Current, per Pin ²	I_O	-35 mA to +35 mA
Common-Mode Transients ³	CM_H, CM_L	-100 kV/μs to +100 kV/μs

¹ All voltages are relative to their respective ground.

² See Figure 2 and Figure 3 for information on maximum allowable current for various temperatures.

³ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 12. Maximum Continuous Working Voltage¹

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

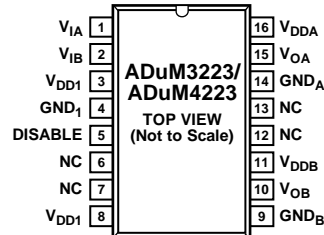
¹ Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 13. Truth Table ADuM3223/ADuM4223 (Positive Logic)¹

DISABLE	V _{IA} Input	V _{IB} Input	V _{DD1} State	V _{DDA} /V _{ddb} State	V _{OA} Output	V _{OB} Output	Notes
L	L	L	Powered	Powered	L	L	Outputs return to the input state within 1 μ s of DISABLE = L assertion.
L	L	H	Powered	Powered	L	H	Outputs return to the input state within 1 μ s of DISABLE = L assertion.
L	H	L	Powered	Powered	H	L	Outputs return to the input state within 1 μ s of DISABLE = L assertion.
L	H	H	Powered	Powered	H	H	Outputs return to the input state within 1 μ s of DISABLE = L assertion.
H	X	X	Powered	Powered	L	L	Outputs take on default low state within 3 μ s of DISABLE = H assertion.
L	L	L	Unpowered	Powered	L	L	Outputs return to the input state within 1 μ s of V _{DD1} power restoration.
X	X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μ s of V _{DDA} /V _{ddb} power restoration.

¹ X = don't care, L = low, and H = high.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT.
DO NOT CONNECT TO THIS PIN.

1045P-003

Figure 4. Pin Configuration

Table 14. ADuM3223/ADuM4223 Pin Function Descriptions

Pin No. ¹	Mnemonic	Description
1	V _{IA}	Logic Input A.
6, 7, 12, 13	NC	No Connect.
2	V _{IB}	Logic Input B.
3, 8	V _{DD1}	Input Supply Voltage.
4	GND ₁	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state within 3 μs of DISABLE = H assertion. Outputs return to the input state within 1 μs of DISABLE = L assertion.
9	GND _B	Ground Reference for Output B.
10	V _{OB}	Output B.
11	V _{DDB}	Output B Supply Voltage.
14	GND _A	Ground Reference for Output A.
15	V _{OA}	Output A.
16	V _{DDA}	Output A Supply Voltage.

¹ Pin 3 and Pin 8 are internally connected; connecting both pins to supply V_{DD1} is recommended.

For specific layout guidelines, refer to the [AN-1109](#) Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*.

TYPICAL PERFORMANCE CHARACTERISTICS

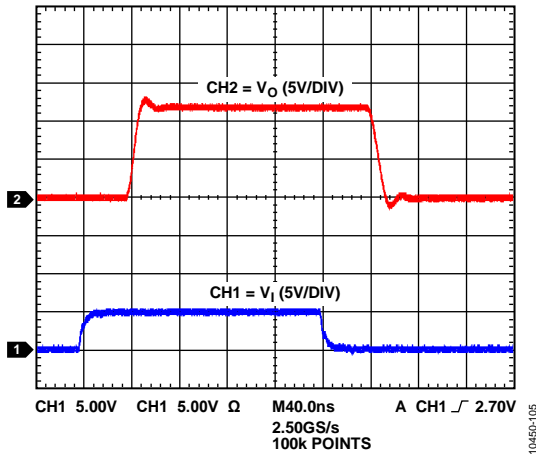


Figure 5. Output Waveform for 2 nF Load with 12 V Output Supply

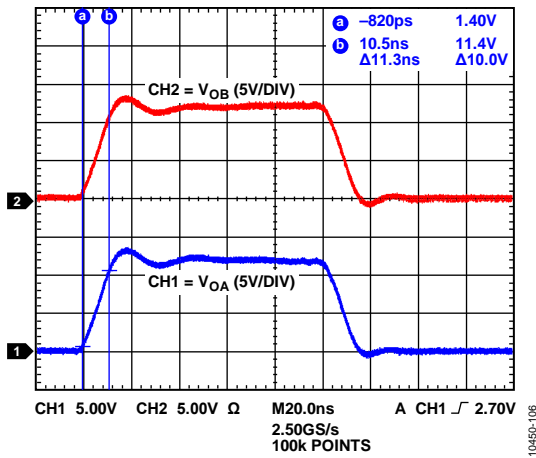


Figure 6. Output Matching and Rise Time Waveforms for 2 nF Load with 12 V Output Supply

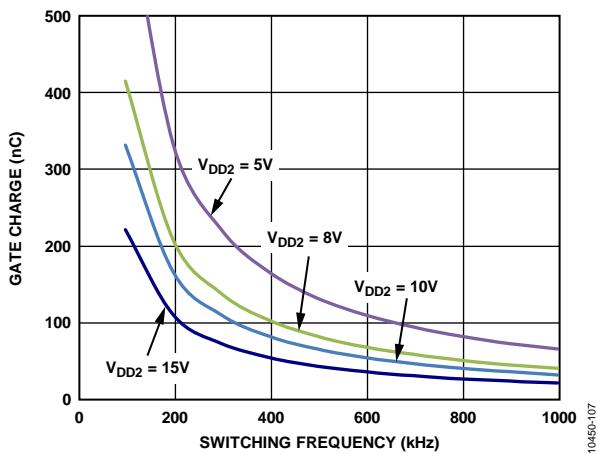


Figure 7. Typical ADuM3223 Maximum Load vs. Frequency ($R_G = 1 \Omega$)

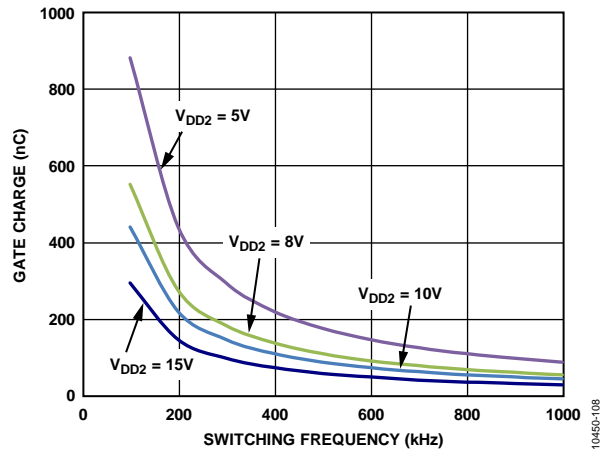


Figure 8. Typical ADuM4223 Maximum Load vs. Frequency ($R_G = 1 \Omega$)

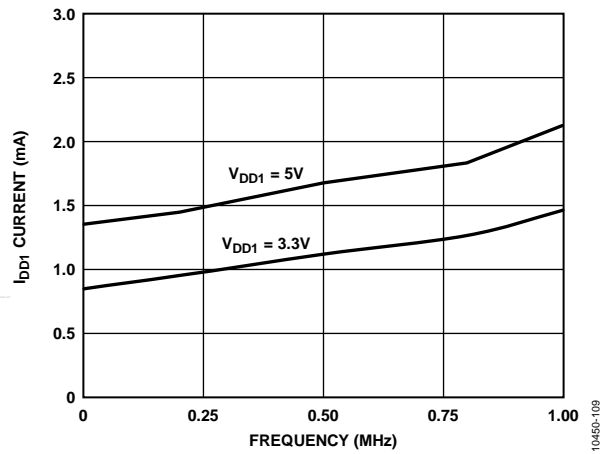


Figure 9. Typical I_{DD1} Supply Current vs. Frequency

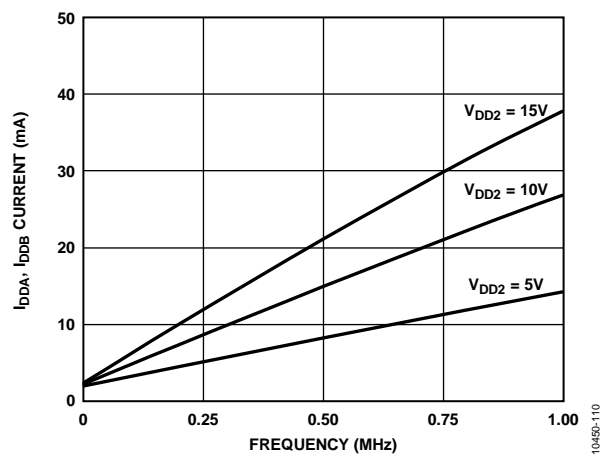


Figure 10. Typical I_{DDA} , I_{ddb} Supply Current vs. Frequency with 2 nF Load

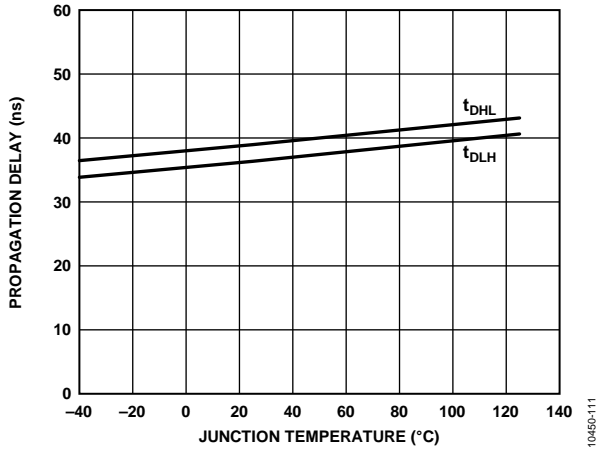


Figure 11. Typical Propagation Delay vs. Temperature

10450-111

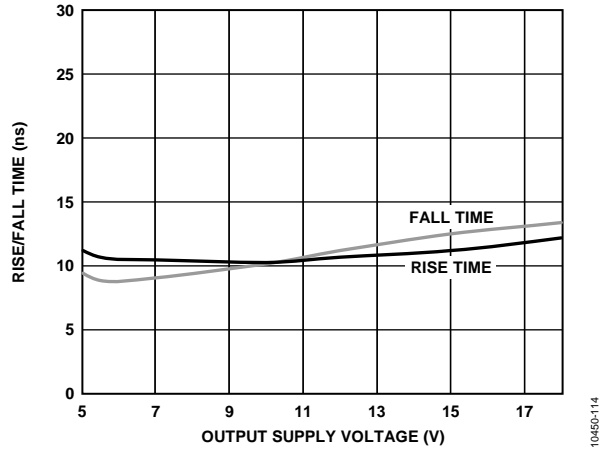


Figure 14. Typical Rise/Fall Time Variation vs. Output Supply Voltage

10450-114

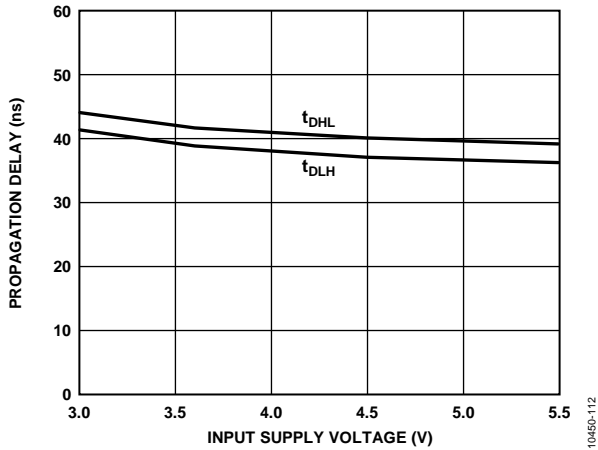


Figure 12. Typical Propagation Delay vs. Input Supply Voltage, $V_{DDA}, V_{ddb} = 12 V$

10450-112

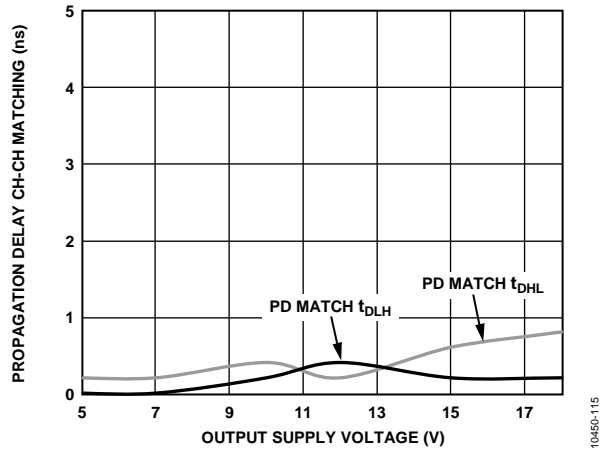


Figure 15. Typical Propagation Delay, Channel-to-Channel Matching vs. Output Supply Voltage

10450-115

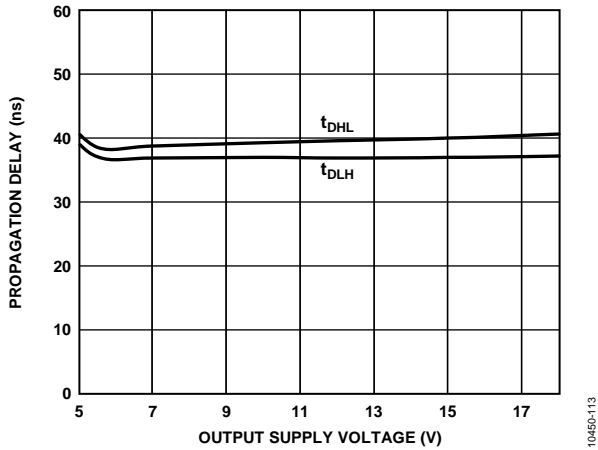


Figure 13. Typical Propagation Delay vs. Input Supply Voltage, $V_{DD1} = 5 V$

10450-113

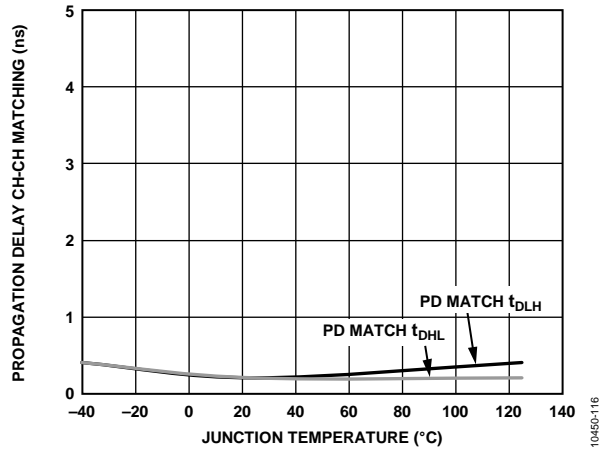


Figure 16. Typical Propagation Delay, Channel-to-Channel Matching vs. Temperature, $V_{DDA}, V_{ddb} = 12 V$

10450-116

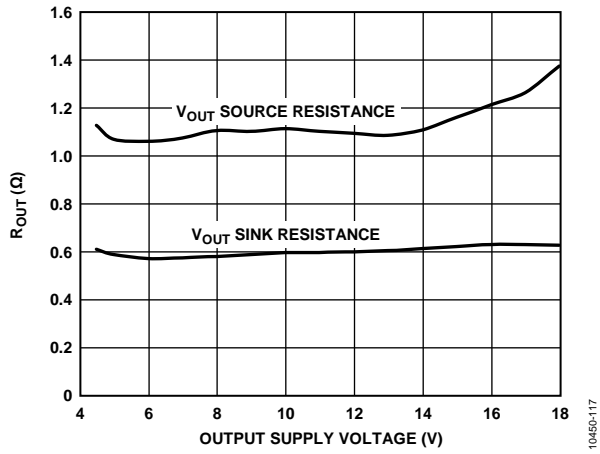


Figure 17. Typical Output Resistance vs. Output Supply Voltage

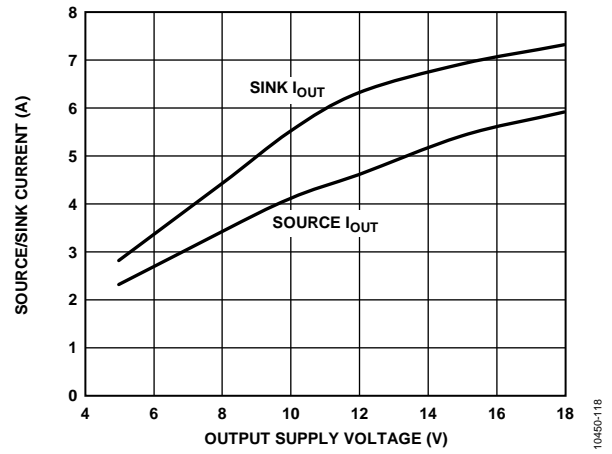


Figure 18. Typical Output Current vs. Output Supply Voltage

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM3223/ADuM4223 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 19. Use a small ceramic capacitor with a value between 0.01 μF and 0.1 μF to provide a good high frequency bypass. On the output power supply pin, V_{DDA} or V_{DDB} , it is recommended to also add a 10 μF capacitor to provide the charge required to drive the gate capacitance at the ADuM3223/ADuM4223 outputs. On the output supply pin, the bypass capacitor use of vias should be avoided or multiple vias should be employed to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin should not exceed 5 mm.

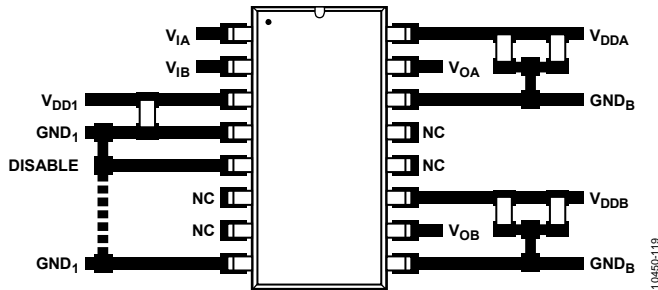


Figure 19. Recommended PCB Layout

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM3223/ADuM4223 specify t_{DLH} (see Figure 20) as the time between the rising input high logic threshold, V_{IH} , to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL} , is defined as the time between the input falling logic low threshold, V_{IL} , and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

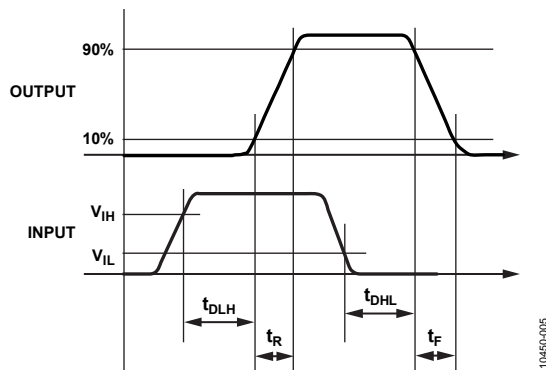


Figure 20. Propagation Delay Parameters

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3223/ADuM4223 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3223/ADuM4223 components operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the part, and heat is, therefore, dissipated mainly through the package pins.

Package thermal dissipation limits the performance of switching frequency vs. output load, as illustrated in Figure 7 and Figure 8 for the maximum load capacitance that can be driven with a 1 Ω series gate resistance for different values of output voltage. For example, this curve shows that a typical ADuM3223 can drive a large MOSFET with 140 nC gate charge at 8 V output (which is equivalent to a 17 nF load) up to a frequency of about 300 kHz.

OUTPUT LOAD CHARACTERISTICS

The ADuM3223/ADuM4223 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the printed circuit board trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate-to-source capacitance (C_{GS}), as shown in Figure 21.

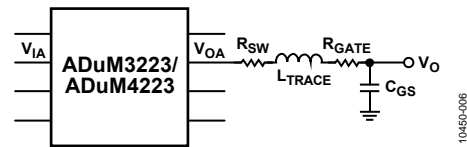


Figure 21. RLC Model of the Gate of an N-Channel MOSFET

R_{SW} is the switch resistance of the internal ADuM3223/ADuM4223 driver output, which is about 1.1 Ω . R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate-to-source capacitance, C_{GS} , of between 2 nF and 10 nF. L_{TRACE} is the inductance of the printed circuit board trace, typically a value of 5 nH or less for a well-designed layout with a very short and wide connection from the ADuM3223/ADuM4223 output to the gate of the MOSFET.

The following equation defines the Q factor of the RLC circuit, which indicates how the ADuM3223/ADuM4223 output responds to a step change. For a well-damped output, Q is less than 1. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

In Figure 5, the ADuM3223/ADuM4223 output waveforms for a 12 V output are shown for a C_{GS} of 2 nF. Note the small amount of ringing of the output in Figure 5 with C_{GS} of 2 nF, R_{SW} of 1.1 Ω, R_{GATE} of 0 Ω, and a calculated Q factor of 0.75, where less than 1 is desired for good damping.

Output ringing can be reduced by adding a series gate resistance to dampen the response. For applications of less than 1 nF load, it is recommended to add a series gate resistor of about 2 Ω to 5 Ω.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 μs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than about 3 μs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit. In addition, the outputs are in a low default state while the power is coming up before the UVLO threshold is crossed.

The ADuM3223/ADuM4223 is immune to external magnetic fields. The limitation on the ADuM3223/ADuM4223 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3223/ADuM4223 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3223/ADuM4223 and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 22.

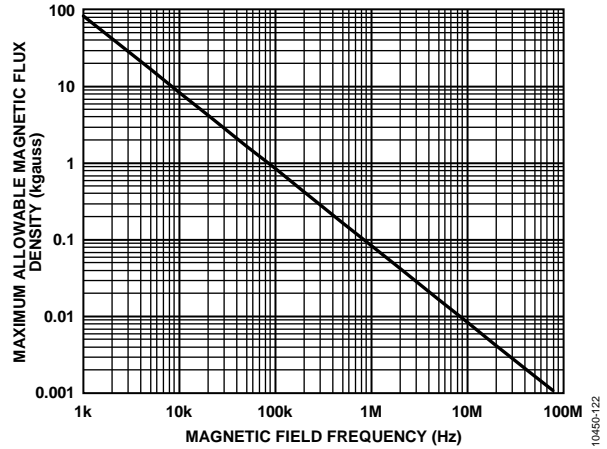


Figure 22. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.08 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3223/ADuM4223 transformers. Figure 23 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM3223/ADuM4223 are immune and only can be affected by extremely large currents operated at a high frequency and very close to the component. For the 1 MHz example, a 0.2 kA current must be placed 5 mm away from the ADuM3223/ADuM4223 to affect the component's operation.

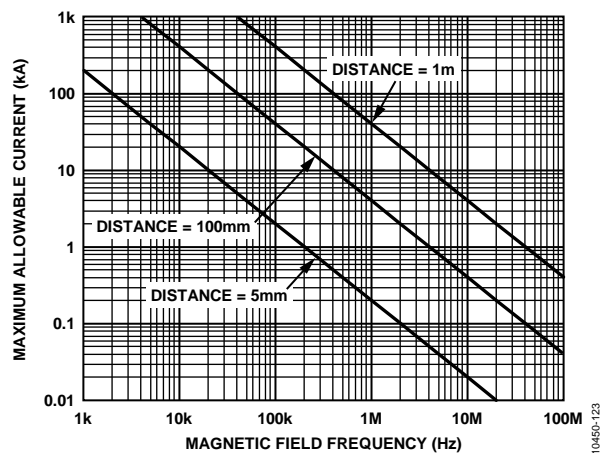


Figure 23. Maximum Allowable Current for Various Current-to-ADuM3223/ADuM4223 Spacings

POWER CONSUMPTION

The supply current at a given channel of the [ADuM3223/ADuM4223](#) isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total supply current, the supply currents for each input and output channel corresponding to I_{DDI} , I_{DDA} , and I_{DDB} are calculated and totaled.

Figure 9 provides total input I_{DDI} supply current as a function of data rate for both input channels. Figure 10 provides total I_{DDA} or I_{DDB} supply current as a function of data rate for both outputs loaded with 2 nF capacitance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM3223/ADuM4223](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 11 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the [ADuM3223/ADuM4223](#) depends on the voltage waveform type imposed across the isolation barrier. The *iCoupler* insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 24, Figure 25, and Figure 26 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *iCoupler* products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. Any cross-insulation voltage waveform that does not conform to Figure 25 or Figure 26 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 12.

Note that the voltage presented in Figure 25 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

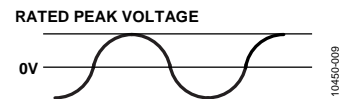


Figure 24. Bipolar AC Waveform

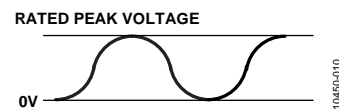


Figure 25. Unipolar AC Waveform

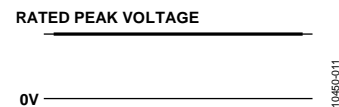
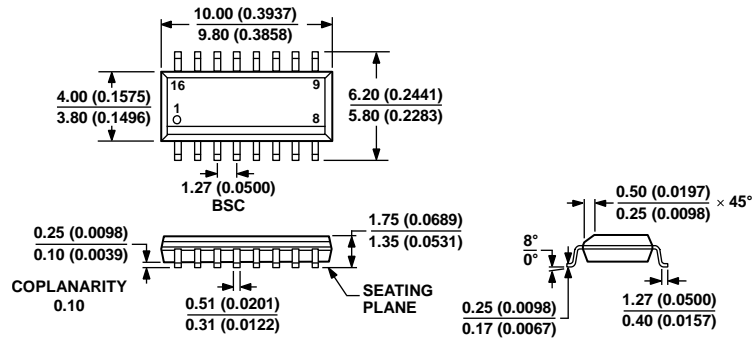


Figure 26. DC Waveform

OUTLINE DIMENSIONS

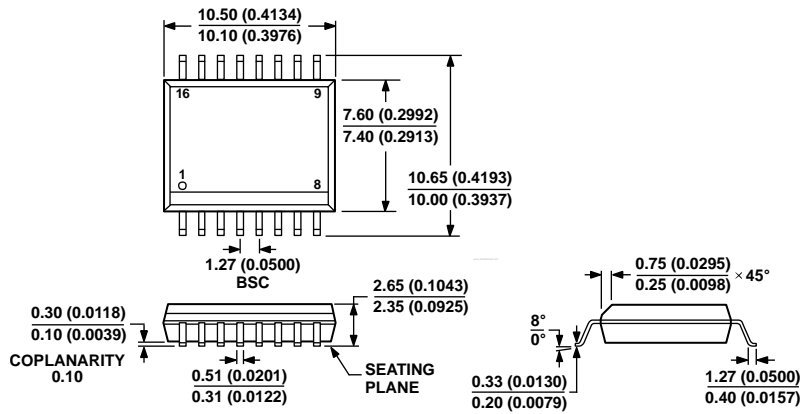


COMPLIANT TO JEDEC STANDARDS MS-012-AC
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Figure 27. 16-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 16-Lead Standard Small Outline Package [SOIC_W] Wide Body (RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

ORDERING GUIDE

Model ¹	No. of Channels	Output Peak Current (A)	Minimum Output Voltage (V)	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuM3223ARZ	2	4	4.5	−40°C to +125°C	16-Lead SOIC_N	R-16	
ADuM3223ARZ-RL7	2	4	4.5	−40°C to +125°C	16-Lead SOIC_N, 13" Tape and Reel	R-16	1,000
ADuM3223BRZ	2	4	7.5	−40°C to +125°C	16-Lead SOIC_N	R-16	
ADuM3223BRZ-RL7	2	4	7.5	−40°C to +125°C	16-Lead SOIC_N, 13" Tape and Reel	R-16	1,000
ADuM3223CRZ	2	4	11.5	−40°C to +125°C	16-Lead SOIC_N	R-16	
ADuM3223CRZ-RL7	2	4	11.5	−40°C to +125°C	16-Lead SOIC_N, 13" Tape and Reel	R-16	1,000
ADuM4223ARWZ	2	4	4.5	−40°C to +125°C	16-Lead SOIC_W	RW-16	
ADuM4223ARWZ-RL	2	4	4.5	−40°C to +125°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16	1,000
ADuM4223BRWZ	2	4	7.5	−40°C to +125°C	16-Lead SOIC_W	RW-16	
ADuM4223BRWZ-RL	2	4	7.5	−40°C to +125°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16	1,000
ADuM4223CRWZ	2	4	11.5	−40°C to +125°C	16-Lead SOIC_W	RW-16	
ADuM4223CRWZ-RL	2	4	11.5	−40°C to +125°C	16-Lead SOIC_W, 13" Tape and Reel	RW-16	1,000
EVAL-ADuM3223AEBZ	2	4	4.5	−40°C to +125°C	ADuM3223 evaluation board		
EVAL-ADuM4223AEBZ	2	4	4.5	−40°C to +125°C	ADuM4223 evaluation board		

¹ Z = RoHS Compliant Part.

NOTES