MC74VHC1G50

Buffer

The MC74VHC1G50 is an advanced high speed CMOS buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output.

The MC74VHC1G50 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1G50 to be used to interface 5.0 V circuits to 3.0 V circuits.

- High Speed: t_{PD} = 3.5 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FET = 104; Equivalent Gate = 26

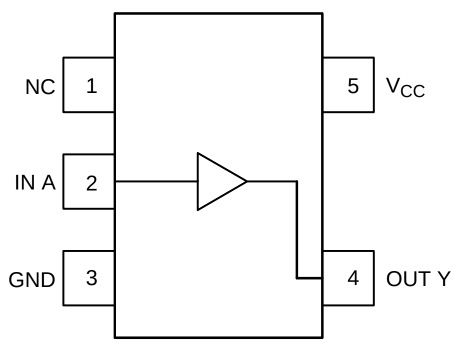

Figure 1. Pinout (Top View)

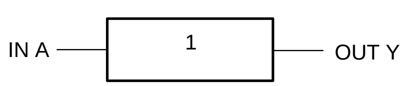

Figure 2. Logic Symbol

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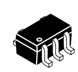
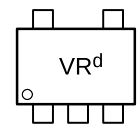
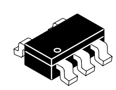
MARKING DIAGRAMS



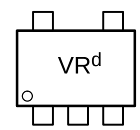
SC–88A / SOT–353/SC–70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code



TSOP–5/SOT–23/SC–59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

PIN ASSIGNMENT	
1	NC
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	Y Output
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (Note 1)

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	DC Input Voltage		–0.5 to +7.0	V
V_{OUT}	DC Output Voltage	$V_{CC} = 0$ High or Low State	–0.5 to 7.0 –0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air	SC–88A, TSOP–5	200	mW
θ_{JA}	Thermal resistance	SC–88A, TSOP–5	333	°C/W
T_L	Lead temperature, 1 mm from case for 10 s		260	°C
T_J	Junction temperature under bias		+150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{Latch–Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	±500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		–55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

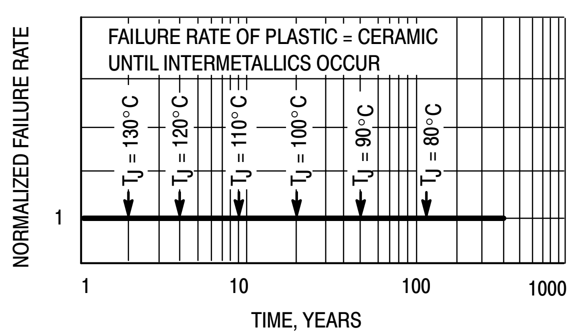


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4$ mA $I_{OL} = 8$ mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5$ V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS $C_{load} = 50$ pF, Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions		$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55 \le T_A \le 125°C$ Min	$-55 \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to $\overline{Y}$	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$ pF $C_L = 50$ pF		4.5 6.4	7.1 10.6		8.5 12.0		10.0 14.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$ pF $C_L = 50$ pF		3.5 4.5	5.5 7.5		6.5 8.5		8.0 10.0	
C_{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Note 6)	8.0	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

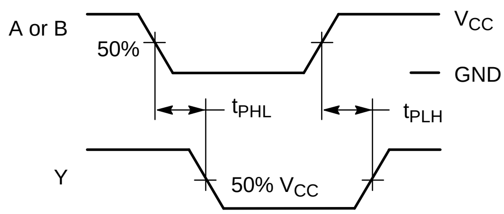


Figure 4. Switching Waveforms

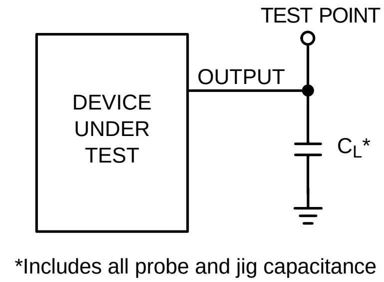


Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature: Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type	Tape and Reel Size
MC74VHC1G50DFT1	MC	74	VHC1G	50	DF	T1	SC–88A / SOT–353 / SC–70	178 mm (7”) 3000 Unit
MC74VHC1G50DFT2	MC	74	VHC1G	50	DF	T2	SC–88A / SOT–353 / SC–70	178 mm (7”) 3000 Unit
MC74VHC1G50DTT1	MC	74	VHC1G	50	DT	T1	TSOPS / SOT–23 / SC–59	178 mm (7”) 3000 Unit

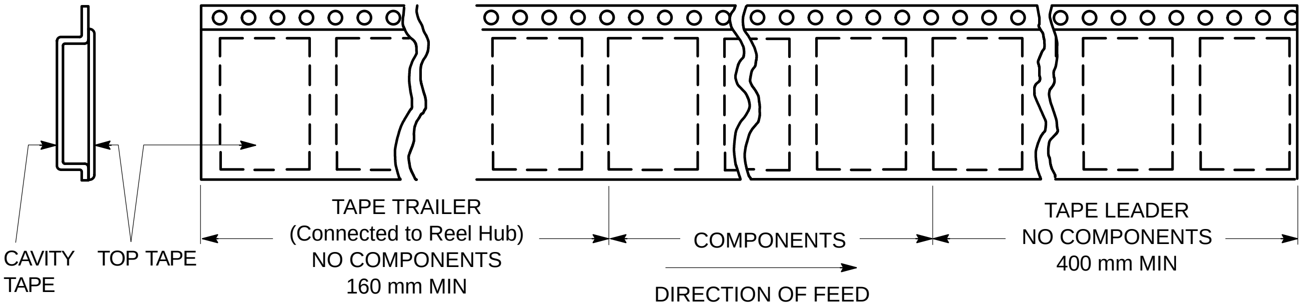


Figure 6. Tape Ends for Finished Goods

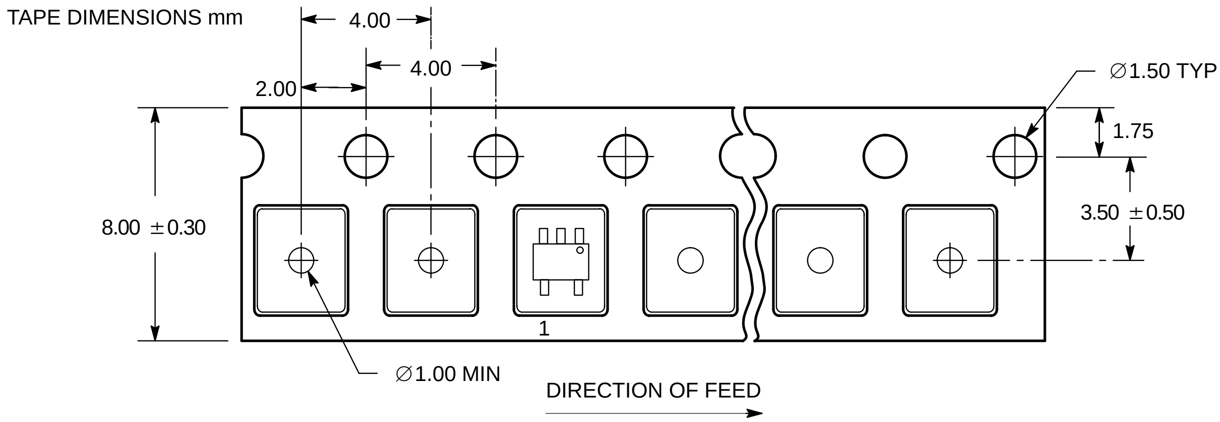


Figure 7. SC–70–5/SC–88A/SOT–353 DFT1 Reel Configuration/Orientation

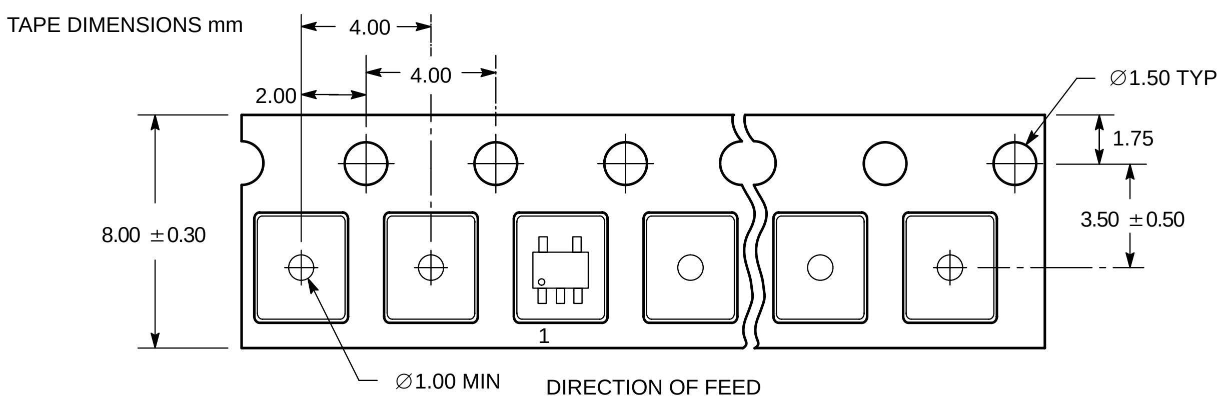


Figure 8. SC–70/SC–88A/SOT–353 DFT2 and SOT23–5/TSOP–5/SC59–5 DTT1 Reel Configuration/Orientation

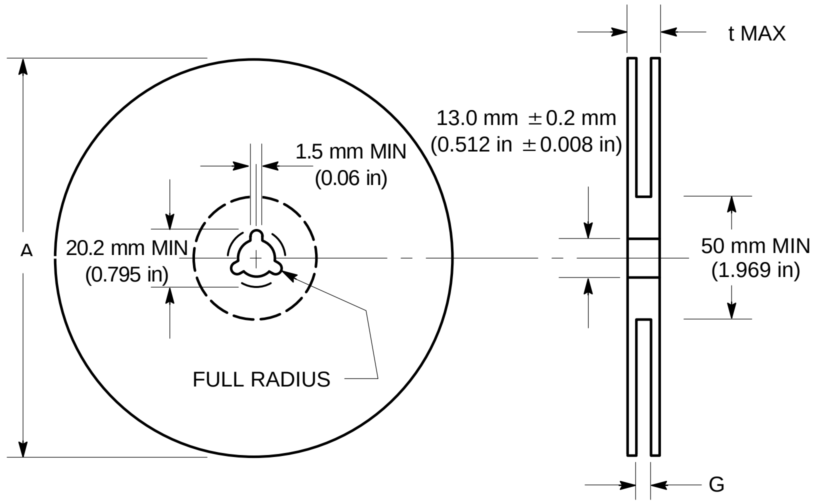


Figure 9. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, –0.0 (0.33 in + 0.059 in, –0.00)	14.4 mm (0.56 in)

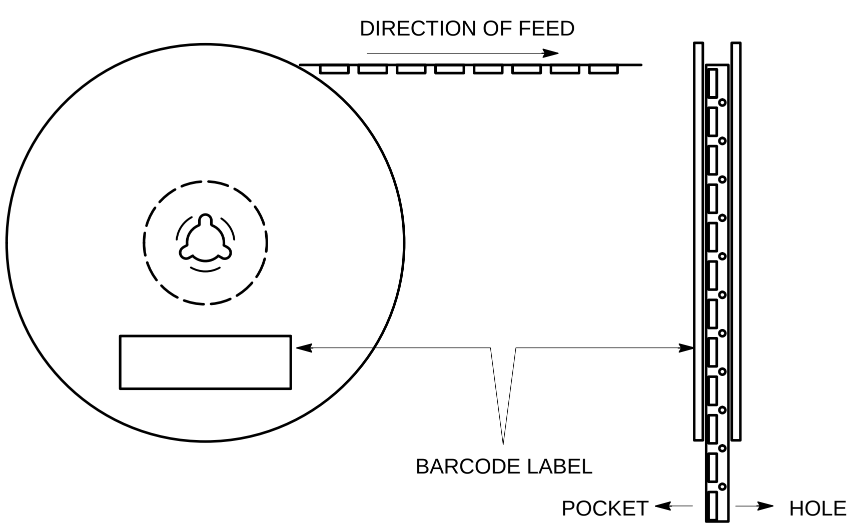
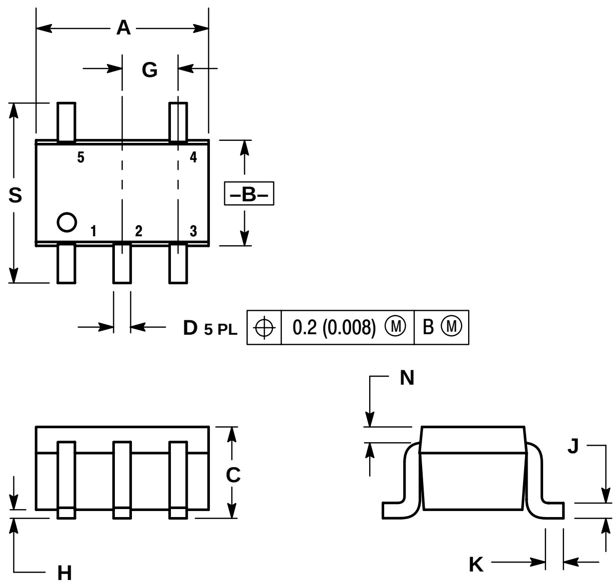


Figure 10. Reel Winding Direction

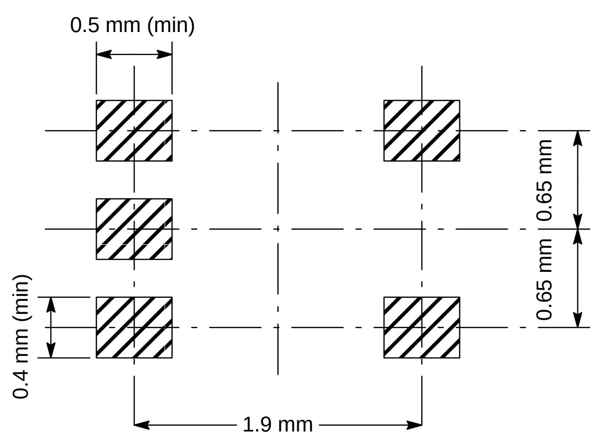
PACKAGE DIMENSIONS

SC–88A / SOT–353 / SC–70
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–02
ISSUE F



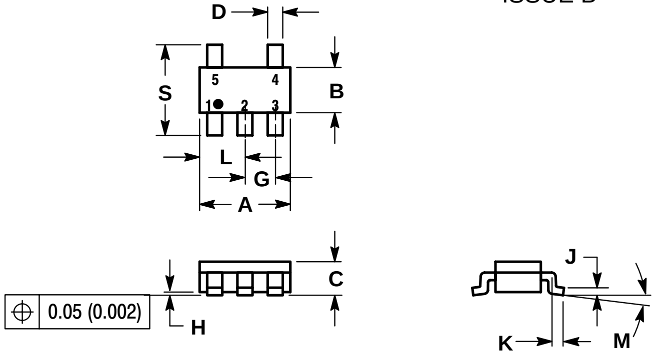
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A–01 OBSOLETE. NEW STANDARD 419A–02.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



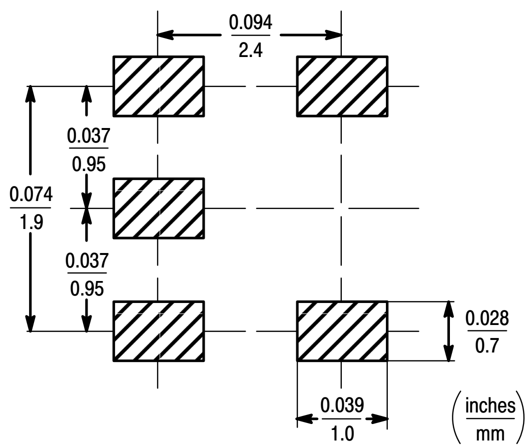
PACKAGE DIMENSIONS

TSOP–5 / SOT–23 / SC–59
DT SUFFIX
5–LEAD PACKAGE
CASE 483–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181



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