

The SL6619 is an advanced Direct Conversion FSK Data Receiver for operation up to 450 MHz. The device integrates all functions to convert a binary FSK modulated RF signal into a demodulated data stream.

Adjacent channel rejection is provided using tuneable gyrator filters. RF and audio AGC functions assist operation when large interfering signals are present and an automatic frequency control (AFC) function is provided to extend centre frequency acceptance.

### FEATURES

- Very Low Power Operation from Single Cell
- Superior Sensitivity
- Operation at 512, 1200 and 2400 Baud
- On Chip 1 Volt Regulator
- 1mm Height Miniature Package
- Automatic Frequency Control Function
- Programmable Post Detection Filter
- AGC Detection Circuitry
- Power Down Function
- Battery Strength Indicator

### APPLICATIONS

- Pagers, including Credit Card, PCMCIA and Watch Pagers
- Low Data Rate Receivers, e.g. Security Systems

### ORDERING INFORMATION

- SL6619/KG/TP1N** 1mm TQFP device, baked and dry packed, supplied in trays
- SL6619/KG/TP1Q** 1mm TQFP device, baked and dry packed, supplied in tape and reel

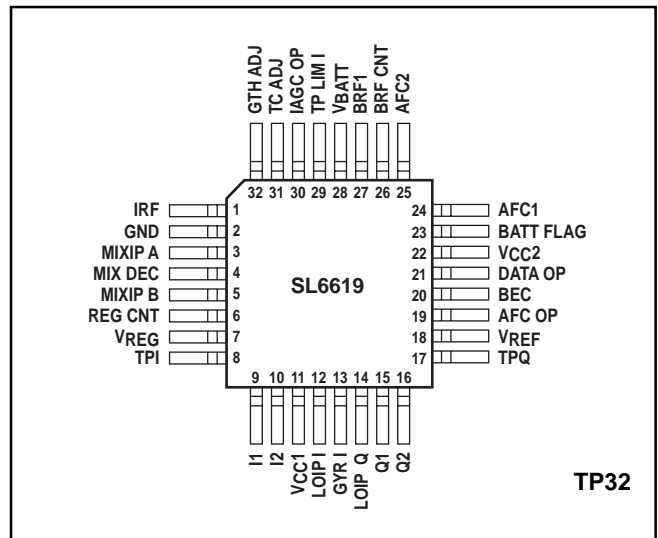


Fig. 1 Pin identification diagram (top view). See Table 1 for pin descriptions

### ABSOLUTE MAXIMUM RATINGS

|   |                  |
|---|------------------|
| Storage temperature   | -55°C to +150°C  |
| Operating temperature   | -10°C to +55°C   |
| Maximum voltage on any pin w.r.t. any other pin, subject to the following conditions: | +4V              |
| Current, pin 3 (MIXIP), pin 5 (MIXPB), pin 12 (LOIP1) and pin 14 (LOIPB)              | <5ma             |
| Most negative voltage on any pin  | -0.5V w.r.t. gnd |

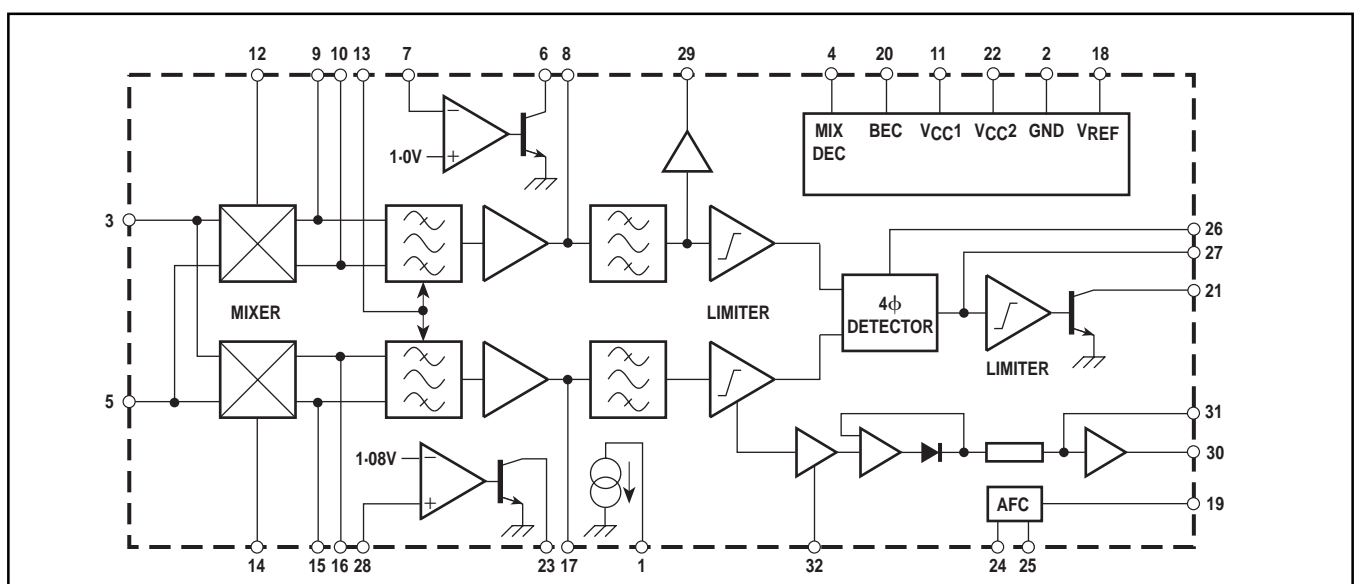


Fig. 2 Block diagram of SL6619

| Pin number | Pin name  | Pin description   |
|------------|-----------|---|
| 1          | IRF       | LNA current source  |
| 2          | GND       | Ground  |
| 3          | MIXIP A   | Mixer input A   |
| 4          | MIX DEC   | Mixer biasing decouple  |
| 5          | MIXIP B   | Mixer input B   |
| 6          | REG CNT   | 1V regulator control external PNP drive                         |
| 7          | VREG      | 1V regulator output voltage                                     |
| 8          | TPI       | I channel pre-yrator filter test point.                         |
| 9          | I1        | Mixer output, I channel   |
| 10         | I2        | Mixer output, I channel   |
| 11         | VCC1      | Positive supply 1   |
| 12         | LOIP I    | LO input channel I  |
| 13         | GYRI      | Gyrator current adjust pin                                      |
| 14         | LOIP Q    | LO input channel Q  |
| 15         | Q1        | Mixer output, Q channel   |
| 16         | Q2        | Mixer output, Q channel   |
| 17         | TPQ       | Q channel pre-yrator filter test point                          |
| 18         | VREF      | Reference voltage   |
| 19         | AFC OP    | AFC output  |
| 20         | BEC       | Battery economy control   |
| 21         | DATA OP   | Data output pin   |
| 22         | VCC2      | Positive supply 2   |
| 23         | BATT FLAG | Battery flag output   |
| 24         | AFC1      | AFC characteristic defining pin                                 |
| 25         | AFC2      | AFC characteristic defining pin                                 |
| 26         | BRF CNT   | Bit rate filter control   |
| 27         | BRF1      | Bit rate filter 1, output from detector                         |
| 28         | VBATT     | Battery flag input voltage                                      |
| 29         | TP LIM I  | I channel limiter (post gyrator filter) test point, output only |
| 30         | IAGC OP   | Audio AGC output current  |
| 31         | TC ADJ    | Audio AGC time constant adjust                                  |
| 32         | GTH ADJ   | Audio AGC gain and threshold adjust. RSSI signal indicator      |

Table 1 SL6619 pin descriptions

**ELECTRICAL CHARACTERISTICS (1)**

Electrical Characteristics (1) are guaranteed over the following range of operating conditions unless otherwise stated

$$T_{AMB} = +25^{\circ}\text{C}, V_{CC1} = 1.3\text{V}, V_{CC2} = 2.7\text{V}$$

| Characteristic                | Pin | Value                   |      |           | Units         | Conditions  |
|-------------------------------|-----|-------------------------|------|-----------|---------------|---|
|                               |     | Min.                    | Typ. | Max.      |               |   |
| Supply voltage, $V_{CC1}$     | 11  | 0.95                    | 1.3  | 2.7       | V             | $V_{CC1} \leq V_{CC2} - 0.8\text{V}$<br>Including IRF<br>$I_{LOAD} = 3\text{mA}$ , external PNP ( $\beta \geq 100$ , $V_{CE} = 0.1\text{V}$ )<br>External PNP ( $h_{FE} \geq 100$ , $V_{CE} = 0.1\text{V}$ )<br>PTAT, voltage on pin 1 = 0.3V and 1.3V<br>Typical temperature coefficient = +0.1mV/°C |
| Supply voltage, $V_{CC2}$     | 22  | 1.9                     | 2.7  | 3.5       | V             |   |
| Supply current, $I_{CC1}$     | 11  | 1.20                    | 1.60 | 2.2       | mA            |   |
| Supply current, $I_{CC2}$     | 22  | 260                     | 350  | 460       | $\mu\text{A}$ |   |
| 1 volt regulator, $V_{REG}$   | 7   | 0.95                    | 1.0  | 1.05      | V             |   |
| 1 volt regulator load current | 7   | 0.25                    |      | 3         | mA            |   |
| LNA current source, IRF       | 1   | 375                     | 500  | 700       | $\mu\text{A}$ |   |
| Reference voltage, $V_{REF}$  | 18  | 1.15                    | 1.25 | 1.31      | V             |   |
| $V_{REF}$ source current      | 18  |                         |      | 20        | $\mu\text{A}$ |   |
| $V_{REF}$ sink current        | 18  |                         |      | 1.0       | $\mu\text{A}$ |   |
| <b>Data Amplifier</b>         |     |                         |      |           |               | Output logic low, pin 21 voltage = 0.3V<br>Output logic high, pin 21 voltage = $V_{CC2}$<br>Preamble at 1200 baud, $\Delta f = 4\text{kHz}$ ,<br>pin 26 = 0V, BRF capacitor = 560pF,<br>DATA OP pullup resistor = 200k $\Omega$   |
| DATA OP sink current          | 21  | 25                      |      |           | $\mu\text{A}$ |   |
| DATA OP leakage current       | 21  |                         |      | 1.0       | $\mu\text{A}$ |   |
| Output mark:space ratio       | 21  | 7:9                     |      | 9:7       |               |   |
| <b>Battery Economy</b>        |     |                         |      |           |               | Pin 20 = logic low<br>Pin 20 = logic low<br>Powered up<br>Powered down<br>Powered up<br>Powered down  |
| Power down $I_{CC1}$          | 11  |                         | 0.5  | 10        | $\mu\text{A}$ |   |
| Power down $I_{CC2}$          | 22  |                         | 2.0  | 10        | $\mu\text{A}$ |   |
| BEC input logic high          | 20  | $V_{CC2} - 0.3\text{V}$ |      | $V_{CC2}$ | V             |   |
| BEC input logic low           | 20  | 0                       |      | 0.3       | V             |   |
| BEC input current             | 20  | -1.0                    |      | 1.0       | $\mu\text{A}$ |   |
| BEC input current             | 20  | -1.0                    |      | 1.0       | $\mu\text{A}$ |   |
| <b>Battery Flag</b>           |     |                         |      |           |               | Current sunk by pin 23 = 1 $\mu\text{A}$<br>Pin 28 voltage = 1.04V<br>Pin 28 voltage = 1.12V<br>Pin 28 voltage = 1.14V<br>$V_{BATT} = 1.14\text{V}$<br>$V_{BATT} = 1.04\text{V}$  |
| $V_{BATT}$ trigger point      | 28  | 1.04                    | 1.08 | 1.12      | V             |   |
| BATT FLAG sink current        | 23  |                         |      | 1.0       | $\mu\text{A}$ |   |
| BATT FLAG sink current        | 23  | 1.0                     |      |           | $\mu\text{A}$ |   |
| BATT FLAG sink current        | 23  | 25                      |      |           | $\mu\text{A}$ |   |
| $V_{BATT}$ input voltage      | 28  |                         |      | 2.0       | V             |   |
| $V_{BATT}$ input current      | 28  | -1.0                    |      | 1.0       | $\mu\text{A}$ |   |
| $V_{BATT}$ input current      | 28  | -1.0                    |      | 1.0       | $\mu\text{A}$ |   |

Continued...

**ELECTRICAL CHARACTERISTICS (1) (Cont.)**

Electrical Characteristics (1) are guaranteed over the following range of operating conditions unless otherwise stated

$$T_{AMB} = +25^{\circ}\text{C}, V_{CC1} = 1.3\text{V}, V_{CC2} = 2.7\text{V}$$

| Characteristic                  | Pin                | Value                |                      |                      | Units         | Conditions   |
|---------------------------------|--------------------|----------------------|----------------------|----------------------|---------------|--|
|                                 |                    | Min.                 | Typ.                 | Max.                 |               |  |
| <b>Mixers</b>                   |                    |                      |                      |                      |               |  |
| LO DC bias voltage              | 12,14              |                      | $V_{CC1}$            |                      | V             |  |
| Gain to TPI                     | 3,5,8,12           | 38                   | 42                   | 46                   | dB            | LO inputs (12, 14) driven in quadrature:<br>45mVrms at 450MHz, CW.<br>Mixer inputs (3, 5) driven differentially:<br>0.45mVrms at 450.004MHz, CW. |
| Gain to TPQ                     | 3,5,14,<br>17      | 38                   | 42                   | 46                   | dB            | As gain to TPI   |
| Match of gain to TPI<br>and TPQ | 3,5,8,<br>12,14,17 | -1                   | 0                    | +1                   | dB            | As gain to TPI   |
| <b>Audio AGC</b>                |                    |                      |                      |                      |               |  |
| IAGC OP max. sink current       | 30                 |                      | 40                   |                      | $\mu\text{A}$ | TPI, TPQ signals limiting  |
| IAGC OP leakage current         | 30                 |                      |                      | 1                    | $\mu\text{A}$ | No signal applied  |
| <b>AFC</b>                      |                    |                      |                      |                      |               |  |
| AFC DC current, $I_{AFC4k5}$    | 19                 |                      | 0.0                  |                      | $\mu\text{A}$ | $f_C = f_{LO} + 4.5\text{kHz}$ , CW  |
| AFC DC current                  | 19                 | $I_{AFC4k5}$<br>+0.2 | $I_{AFC4k5}$<br>+0.7 |                      | $\mu\text{A}$ | $f_C = f_{LO} + 2.5\text{kHz}$ , CW  |
| AFC DC current                  | 19                 |                      | $I_{AFC4k5}$<br>-0.9 | $I_{AFC4k5}$<br>-0.2 | $\mu\text{A}$ | $f_C = f_{LO} + 6.5\text{kHz}$ , CW  |
| <b>Bit Rate Filter Control</b>  |                    |                      |                      |                      |               |  |
| BRF CNT input logic high        | 26                 | $V_{CC2}$<br>-0.3    |                      | $V_{CC2}$            | V             | 2400 baud  |
| BRF CNT input logic low         | 26                 | 0                    |                      | 0.1                  | V             | 1200 baud  |
| Tristate I/P current window     | 26                 | -0.4                 |                      | +0.4                 | $\mu\text{A}$ | 512 baud   |
| BRF 1 output current            | 27                 |                      | 3.5                  |                      | $\mu\text{A}$ | Pin 26 logic high  |
| BRF 1 output current            | 27                 |                      | 1.7                  |                      | $\mu\text{A}$ | Pin 26 logic low   |
| BRF 1 output current            | 27                 |                      | 0.74                 |                      | $\mu\text{A}$ | Pin 26 logic tristate (open circuit)   |
| BRF CNT input high current      | 26                 | -7.5                 |                      | +7.5                 | $\mu\text{A}$ |  |
| BRF CNT input low current       | 26                 | -7.5                 |                      | +7.5                 | $\mu\text{A}$ |  |

**ELECTRICAL CHARACTERISTICS (2)**

Electrical Characteristics (2) are guaranteed over the following range of operating conditions unless otherwise stated.

Characteristics are tested at room temperature only and are guaranteed by characterisation test or design.

$$T_{AMB} = -10^{\circ}\text{C to } +55^{\circ}\text{C}, V_{CC1} = 1.4\text{V to } 2.0\text{V}, V_{CC2} = 2.3\text{V to } 3.2\text{V}, V_{CC1} < V_{CC2} - 0.8\text{V}$$

| Characteristic                | Pin | Value                   |      |           | Units         | Conditions  |
|-------------------------------|-----|-------------------------|------|-----------|---------------|---|
|                               |     | Min.                    | Typ. | Max.      |               |   |
| Supply voltage, $V_{CC1}$     | 11  | 0.95                    | 1.3  | 2.7       | V             | $V_{CC1} \leq V_{CC2} - 0.8\text{V}$ at $\geq 25^{\circ}\text{C}$ only<br>Including IRF<br>$I_{LOAD} = 3\text{mA}$ , external PNP ( $\beta \geq 100$ , $V_{CE} = 0.1\text{V}$ )<br>External PNP ( $h_{FE} \geq 100$ , $V_{CE} = 0.1\text{V}$ )<br>PTAT, voltage on pin 1 = 0.3V and 1.3V<br>Typical temperature coefficient = $+0.1\text{mV}/^{\circ}\text{C}$<br><br>Stable data O/P when 3dB above sensitivity.<br>$C_{VREF} = 2.2\mu\text{F}$<br>Fall to 10% of steady state $I_{CC1}$ . $C_{VREF} = 2.2\mu\text{F}$ |
| Supply voltage, $V_{CC2}$     | 22  | 1.9                     | 2.7  | 3.5       | V             |   |
| Supply current, $I_{CC1}$     | 11  |                         | 1.60 | 2.4       | mA            |   |
| Supply current, $I_{CC2}$     | 22  |                         | 350  | 510       | $\mu\text{A}$ |   |
| 1 volt regulator, $V_{REG}$   | 7   | 0.93                    | 1.0  | 1.05      | V             |   |
| 1 volt regulator load current | 7   | 0.25                    |      | 3         | mA            |   |
| LNA current source, IRF       | 1   | 375                     | 500  | 800       | $\mu\text{A}$ |   |
| Reference voltage, $V_{REF}$  | 18  | 1.13                    | 1.25 | 1.33      | V             |   |
| $V_{REF}$ source current      | 18  |                         |      | 18        | $\mu\text{A}$ |   |
| $V_{REF}$ sink current        | 18  |                         |      | 0.8       | $\mu\text{A}$ |   |
| Turn-on time                  |     |                         | 5    |           | ms            |   |
| Turn-off time                 |     |                         | 1    |           | ms            |   |
| <b>Data Amplifier</b>         |     |                         |      |           |               |   |
| DATA OP sink current          | 21  | 22                      |      |           | $\mu\text{A}$ | Output logic low, pin 21 voltage = 0.3V<br>Output logic high, pin 21 voltage = $V_{CC2}$<br>Preamble at 1200 baud, $\Delta f = 4\text{kHz}$ ,<br>pin 26 = 0V, BR capacitor = 560pF,<br>DATA OP pullup resistor = 200k $\Omega$  |
| DATA OP leakage current       | 21  |                         |      | 1.5       | $\mu\text{A}$ |   |
| Output mark:space ratio       | 21  | 7:9                     |      | 9:7       |               |   |
| <b>Battery Economy</b>        |     |                         |      |           |               |   |
| Power down $I_{CC1}$          | 11  |                         | 0.5  | 12        | $\mu\text{A}$ | Pin 20 = logic low<br>Pin 20 = logic low<br>Powered up<br>Powered down<br>Powered up<br>Powered down  |
| Power down $I_{CC2}$          | 22  |                         | 2.0  | 12        | $\mu\text{A}$ |   |
| BEC input logic high          | 20  | $V_{CC2} - 0.3\text{V}$ |      | $V_{CC2}$ | V             |   |
| BEC input logic low           | 20  | 0                       |      | 0.3       | V             |   |
| BEC input current             | 20  | -1.0                    |      | 1.5       | $\mu\text{A}$ |   |
| BEC input current             | 20  | -1.0                    |      | 1.5       | $\mu\text{A}$ |   |
| <b>Battery Flag</b>           |     |                         |      |           |               |   |
| $V_{BATT}$ trigger point      | 28  | 1.04                    | 1.08 | 1.12      | V             | Current sunk by pin 23 = $1\mu\text{A}$<br>Pin 28 voltage = 1.04V<br>Pin 28 voltage = 1.12V<br>Pin 28 voltage = 1.14V   |
| BATT FLAG sink current        | 23  |                         |      | 2         | $\mu\text{A}$ |   |
| BATT FLAG sink current        | 23  | 2                       |      |           | $\mu\text{A}$ |   |
| BATT FLAG sink current        | 23  | 20                      |      |           | $\mu\text{A}$ |   |
| $V_{BATT}$ input voltage      | 28  |                         |      | 2.0       | V             | $V_{BATT} = 1.14\text{V}$<br>$V_{BATT} = 1.04\text{V}$  |
| $V_{BATT}$ input current      | 28  | -1.5                    |      | 1.5       | $\mu\text{A}$ |   |
| $V_{BATT}$ input current      | 28  | -1.5                    |      | 1.5       | $\mu\text{A}$ |   |

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**ELECTRICAL CHARACTERISTICS (2) (Cont.)**

Electrical Characteristics (2) are guaranteed over the following range of operating conditions unless otherwise stated.

Characteristics are tested at room temperature only and are guaranteed by characterisation test or design.

$$T_{AMB} = -10^{\circ}\text{C to } +55^{\circ}\text{C}, V_{CC1} = 1.4\text{V to } 2.0\text{V}, V_{CC2} = 2.3\text{V to } 3.2\text{V}, V_{CC1} < V_{CC2} - 0.8\text{V}$$

| Characteristic                  | Pin                | Value                |                      |                      | Units         | Conditions   |
|---------------------------------|--------------------|----------------------|----------------------|----------------------|---------------|--|
|                                 |                    | Min.                 | Typ.                 | Max.                 |               |  |
| <b>Mixers</b>                   |                    |                      |                      |                      |               |  |
| LO DC bias voltage              | 12,14              |                      | $V_{CC1}$            |                      | V             |  |
| Gain to TPI                     | 3,5,8,12           | 35                   | 42                   | 46                   | dB            | LO inputs (12, 14) driven in quadrature:<br>45mVrms at 450MHz, CW.<br>Mixer inputs (3, 5) driven differentially:<br>0.45mVrms at 450.004MHz, CW. |
| Gain to TPQ                     | 3,5,14,<br>17      | 35                   | 42                   | 46                   | dB            | As gain to TPI   |
| Match of gain to TPI<br>and TPQ | 3,5,8,<br>12,14,17 | -1.5                 | 0                    | +1.5                 | dB            | As gain to TPI   |
| <b>Audio AGC</b>                |                    |                      |                      |                      |               |  |
| IAGC OP max. sink current       | 30                 | 15                   | 40                   | 80                   | $\mu\text{A}$ | TPI, TPQ signals limiting  |
| IAGC OP leakage current         | 30                 |                      |                      | 2                    | $\mu\text{A}$ | No signal applied  |
| <b>AFC</b>                      |                    |                      |                      |                      |               |  |
| AFC DC current, $I_{AFC4k5}$    | 19                 |                      | 0.0                  |                      | $\mu\text{A}$ | $f_C = f_{LO} + 4.5\text{kHz}$ , CW  |
| AFC DC current                  | 19                 | $I_{AFC4k5}$<br>+0.1 | $I_{AFC4k5}$<br>+0.7 |                      | $\mu\text{A}$ | $f_C = f_{LO} + 2.5\text{kHz}$ , CW  |
| AFC DC current                  | 19                 |                      | $I_{AFC4k5}$<br>-0.9 | $I_{AFC4k5}$<br>-0.1 | $\mu\text{A}$ | $f_C = f_{LO} + 6.5\text{kHz}$ , CW  |
| <b>Bit Rate Filter Control</b>  |                    |                      |                      |                      |               |  |
| BRF CNT input logic high        | 26                 | $V_{CC2}$<br>-0.3    |                      | $V_{CC2}$            | V             | 2400 baud  |
| BRF CNT input logic low         | 26                 | 0                    |                      | 0.1                  | V             | 1200 baud  |
| Tristate I/P current window     | 26                 | -0.4                 |                      | +0.4                 | $\mu\text{A}$ | 512 baud   |
| BRF 1 output current            | 27                 |                      | 3.5                  |                      | $\mu\text{A}$ | Pin 26 logic high  |
| BRF 1 output current            | 27                 |                      | 1.7                  |                      | $\mu\text{A}$ | Pin 26 logic low   |
| BRF 1 output current            | 27                 |                      | 0.74                 |                      | $\mu\text{A}$ | Pin 26 logic tristate (open circuit)   |
| BRF CNT input high current      | 26                 | -10                  |                      | +10                  | $\mu\text{A}$ |  |
| BRF CNT input low current       | 26                 | -10                  |                      | +10                  | $\mu\text{A}$ |  |

**RECEIVER CHARACTERISTICS (450MHz)**

Receiver Characteristics (450MHz) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are not tested but are guaranteed by characterisation test or design. All measurements made using the characterisation circuit Fig. 5. See Application Note AN137 for details of test method.

$T_{AMB} = -10^{\circ}\text{C}$  to  $+55^{\circ}\text{C}$ ,  $V_{CC1} = 1.04\text{V}$  to  $2.0\text{V}$ ,  $V_{CC2} = 2.3\text{V}$  to  $3.2\text{V}$ ,  $V_{CC1} < V_{CC2} - 0.8\text{V}$ , carrier frequency =  $450\text{MHz}$ , BER = 1 in 30, AFC open loop. LNA gain set such that an RF signal of  $-73\text{dBm}$  at the LNA input, offset from the LO by  $4\text{kHz}$ , gives a typical IF signal level of  $300\text{mV p-p}$  at TPI and TPQ. LNA noise figure  $< 2\text{dB}$

| Characteristic                             | Value     |           |           | Units | Conditions  |  |
|--|-----------|-----------|-----------|-------|---|--|
|  | Min.      | Typ.      | Max.      |       |   |  |
| <b>Sensitivity</b>                         |           | -128      |           | dBm   | 512bps, $\Delta f = 4.5\text{kHz}$  |  |
|  |           | -126      | -122      | dBm   | 1200bps, $\Delta f = 4.0\text{kHz}$   |  |
|  |           | -123      | -119      | dBm   | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$                                  |  |
| <b>Intermodulation, IP3</b>                | 50        | 57        |           | dB    | 512bps, $\Delta f = 4.5\text{kHz}$  |  |
|  |           | 55        |           | dB    | 1200bps, $\Delta f = 4.0\text{kHz}$   |  |
|  | 48        | 53        |           | dB    | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$ . Channel spacing $25\text{kHz}$ |  |
| <b>Adjacent Channel</b>                    | 62.5      | 74        |           | dB    | 512bps, $\Delta f = 4.5\text{kHz}$  |  |
|  |           | 72        |           | dB    | 1200bps, $\Delta f = 4.0\text{kHz}$   |  |
|  | 60        | 69        |           | dB    | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$ . Channel spacing $25\text{kHz}$ |  |
| <b>Deviation Acceptance</b>                | Up        | +1.9      |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC   |  |
|  | Down      | -2.5      |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC   |  |
|  | Up        | +1.8      | +3.0      | +4.6  | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC |
|  | Down      | -2.7      | -2.3      | -1.7  | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC |
|  | Up        | +1.7      | +2.5      | +4.6  | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC |
|  | Down      | -3        | -2.3      | -1.7  | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC |
| <b>Centre Frequency Acceptance</b>         |           | $\pm 2.8$ |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC   |  |
|  | $\pm 2.0$ | $\pm 2.5$ | $\pm 2.9$ | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC  |  |
|  | $\pm 2.0$ | $\pm 2.5$ | $\pm 3.2$ | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC  |  |
| <b>AFC Capture Range (AFC Closed Loop)</b> |           | $\pm 4$   |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ . All at sensitivity $+3\text{dB}$ or above              |  |
|  |           | $\pm 3.5$ |           | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ . All at sensitivity $+3\text{dB}$ or above             |  |
|  |           | $\pm 4$   |           | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ . All at sensitivity $+3\text{dB}$ or above             |  |

**RECEIVER CHARACTERISTICS (280MHz)**

Receiver Characteristics (280MHz) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are not tested but are guaranteed by characterisation test or design. All measurements made using the characterisation circuit Fig. 5. See Application Note AN137 for details of test method.

$T_{AMB} = -10^{\circ}\text{C}$  to  $+55^{\circ}\text{C}$ ,  $V_{CC1} = 1.04\text{V}$  to  $2.0\text{V}$ ,  $V_{CC2} = 2.3\text{V}$  to  $3.2\text{V}$ ,  $V_{CC1} < V_{CC2} - 0.8\text{V}$ , carrier frequency = 280MHz, BER = 1 in 30, AFC open loop. LNA gain set such that an RF signal of  $-73\text{dBm}$  at the LNA input, offset from the LO by 4kHz, gives a typical IF signal level of 300mV p-p at TPI and TPQ. LNA noise figure  $< 2\text{dB}$

| Characteristic                             | Value     |           |           | Units | Conditions   |  |
|--|-----------|-----------|-----------|-------|--|--|
|  | Min.      | Typ.      | Max.      |       |  |  |
| <b>Sensitivity</b>                         |           | -129      |           | dBm   | 512bps, $\Delta f = 4.5\text{kHz}$   |  |
|  | -128      | -127      | -124      | dBm   | 1200bps, $\Delta f = 4.0\text{kHz}$  |  |
|  | -127      | -124      | -121      | dBm   | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$                         |  |
| <b>Intermodulation, IP3</b>                |           | 57        |           | dB    | 512bps, $\Delta f = 4.5\text{kHz}$   |  |
|  | 52        | 56        | 60        | dB    | 1200bps, $\Delta f = 4.0\text{kHz}$  |  |
|  | 49        | 53.5      | 57        | dB    | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$ . Channel spacing 25kHz |  |
| <b>Adjacent Channel</b>                    |           | 74        |           | dB    | 512bps, $\Delta f = 4.5\text{kHz}$   |  |
|  | 62.5      | 72        | 80        | dB    | 1200bps, $\Delta f = 4.0\text{kHz}$  |  |
|  | 60        | 70        | 77        | dB    | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$ . Channel spacing 25kHz |  |
| <b>Deviation Acceptance</b>                | Up        | +1.9      |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC  |  |
|  | Down      | -2.5      |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC  |  |
|  | Up        | +1.8      | +3.0      | +4.6  | kHz  | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC |
|  | Down      | -2.7      | -2.3      | -1.7  | kHz  | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC |
|  | Up        | +1.7      | +2.5      | +4.6  | kHz  | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC |
|  | Down      | -3.0      | -2.3      | -1.7  | kHz  | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC |
| <b>Centre Frequency Acceptance</b>         |           | $\pm 2.8$ |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ , no AFC  |  |
|  | $\pm 2.0$ | $\pm 2.5$ | $\pm 2.9$ | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ , no AFC                                       |  |
|  | $\pm 2.0$ | $\pm 2.5$ | $\pm 3.2$ | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ , no AFC                                       |  |
| <b>AFC Capture Range (AFC Closed Loop)</b> |           | $\pm 4$   |           | kHz   | 512bps, $\Delta f = 4.5\text{kHz}$ . All at sensitivity +3dB or above              |  |
|  |           | $\pm 3.5$ |           | kHz   | 1200bps, $\Delta f = 4.0\text{kHz}$ . All at sensitivity +3dB or above             |  |
|  |           | $\pm 4$   |           | kHz   | 2400bps, $\Delta f = 4.5\text{kHz}$ . All at sensitivity +3dB or above             |  |
| <b>1MHz Blocking</b>                       |           | 75        |           | dB    | 512bps, $\Delta f = 4.5\text{kHz}$   |  |
|  | 67        | 75        | 78        | dB    | 1200bps, $\Delta f = 4.0\text{kHz}$  |  |
|  | 65        | 75        | 76        | dB    | 2400bps, $\Delta f = 4.5\text{kHz}$ . LO = $-15\text{dBm}$                         |  |



## OPERATION OF SL6619

### Low Noise Amplifier

To achieve optimum performance it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This is easily biased using the on-chip voltages and current source provided. All voltages and current sources used for bias of the RF amplifier, receiver and mixers should be RF decoupled using 1nF capacitors. The receiver also requires a stable Local Oscillator at the required channel frequency.

### Local Oscillator

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their  $-3\text{dB}/45^\circ$  transfer characteristic. The RC characteristics for I and Q channels are combined to give a full  $90^\circ$  phase differential between the LO ports of the device. Each LO port also requires an equal level of drive from the oscillator. This is achieved by forming the two RC networks into a power divider.

### Gyrator Filters

The on-chip filters include an adjustable gyrator filter. This may be adjusted by changing the value of the resistor connected between pin 13 and GND. This allows adjustment of the filters' cutoff frequency and allows for compensation for possible process variations.

### Audio AGC (Fig. 3)

The Audio AGC consists of a current sink which is controlled by the audio (baseband) signal. It has three parameters that may be controlled by the user. These are the attack (turn on) time, decay (duration) time and threshold level. The attack time is simply determined by the value of the external capacitor connected to TCADJ. The external capacitor is in series with an internal  $100\text{k}\Omega$  resistor and the time constant of this circuit dictates the attack time of the AGC.

$$\text{i.e. } t_{\text{ATTACK}} = 100\text{k}\Omega \times C18$$

The decay time is determined by the external resistor connected in parallel with the capacitor CTC. The decay time is simply

$$t_{\text{DECAY}} = R17 \times C18$$

When a large audio (baseband) signal is incident on the input to the AGC circuit, the variable current source is turned on. This causes a voltage drop across R13. The voltage potential between  $V_{\text{REF}}$  and the voltage on pin 31 causes a current to flow in pin 30. This charges up C18 through the  $100\text{k}\Omega$  internal resistor. As the voltage across the capacitor increases, a current source is turned on and this sinks current from pin 32. The current sink on pin 32 can be used to drive

the external AGC circuit by causing a PIN diode to conduct, reducing the signal to the RF amplifier.

### RF AGC

The RF AGC is an automatic gain control loop that protects the mixer's RF inputs, Pins 3 and 5, from large out of band RF signals. The loop consists of an RF received signal strength indicator which detect the signal at the inputs of the mixers. This RSSI signal is then used to control the LNA current source (pin 1).

### Regulator

The on-chip regulator should be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:

$$H_{\text{FE}} > 100 \text{ for } V_{\text{CE}} = 0.1\text{V}$$

If no external transistor is used, the maximum current sourcing capability of the regulator is limited to  $30\mu\text{A}$ .

### Automatic Frequency Control (Fig. 4)

The Automatic Frequency Control consists of a detection circuit which gives a current output at AFC OP whose magnitude and sign is a function of the difference between the local oscillator ( $f_{\text{LO}}$ ) and carrier frequencies ( $f_{\text{C}}$ ). This output current is then filtered by an off-chip integrating capacitor. The integrator's output voltage is used to control a voltage control crystal oscillator. This closes the AFC feedback loop giving the automatic frequency control function. For an FSK modulated incoming RF carrier, the AFC OP current's polarity is positive, i.e. current is sourced for  $f_{\text{LO}} < f_{\text{C}} < f_{\text{LO}} + 4\text{kHz}$  and negative, i.e. current is sunk, for  $f_{\text{LO}} > f_{\text{C}} > f_{\text{LO}} - 4\text{kHz}$ . The magnitude of the AFC OP current is a function of frequency offset and the transmitted data's bit stream. If the carrier frequency, ( $f_{\text{C}}$ ), equals the local oscillator frequency, ( $f_{\text{LO}}$ ) then the magnitude of the current is zero.

### BIT RATE FILTER CONTROL

The logic level on pin 26 controls the cutoff frequency of the 1st order bit rate for a given bit rate filter capacitor at pin 27. This allows the cutoff frequency to be changed between  $f_{\text{C}}$ ,  $2f_{\text{C}}$  and  $0.43f_{\text{C}}$  through the logic level on pin 26. This function is achieved by changing the value of the current in the  $4\phi$  detector's output stage. A logic zero (0V to 0.1V) on pin 26 gives a cutoff frequency of  $f_{\text{C}}$  a logic one ( $V_{\text{CC2}} - 0.3\text{V}$  to  $V_{\text{CC2}}$ ) gives a cut off frequency of  $2f_{\text{C}}$  and an open circuit at pin 26 gives a cutoff frequency of  $0.43f_{\text{C}}$ .

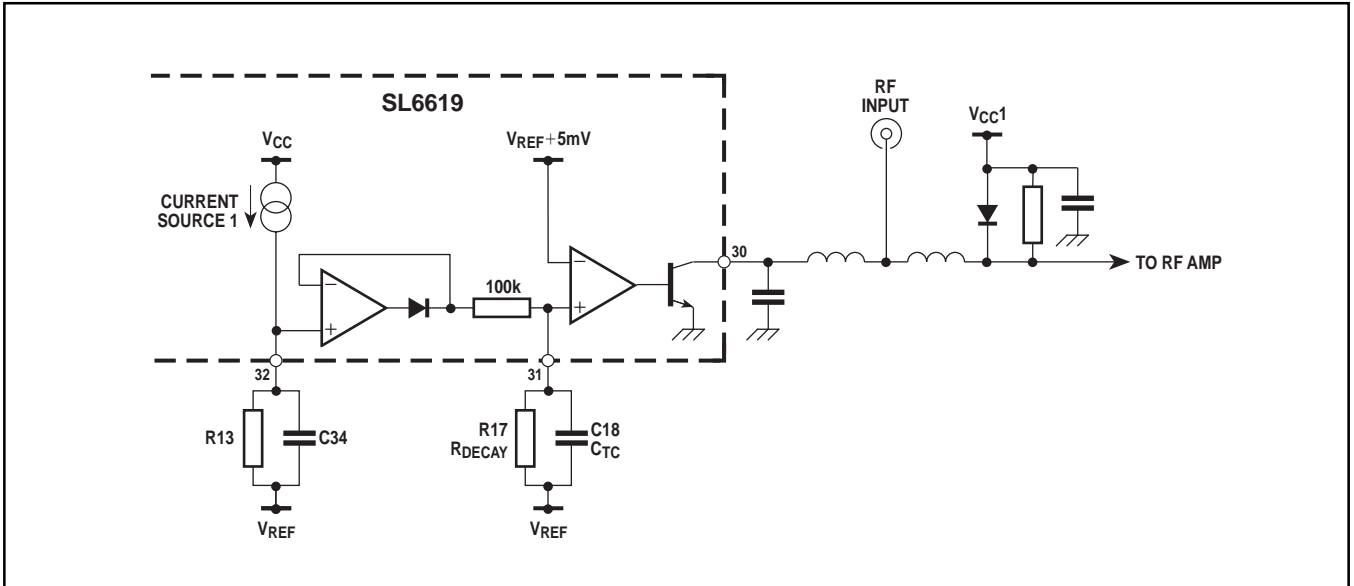


Fig.3 AGC schematic

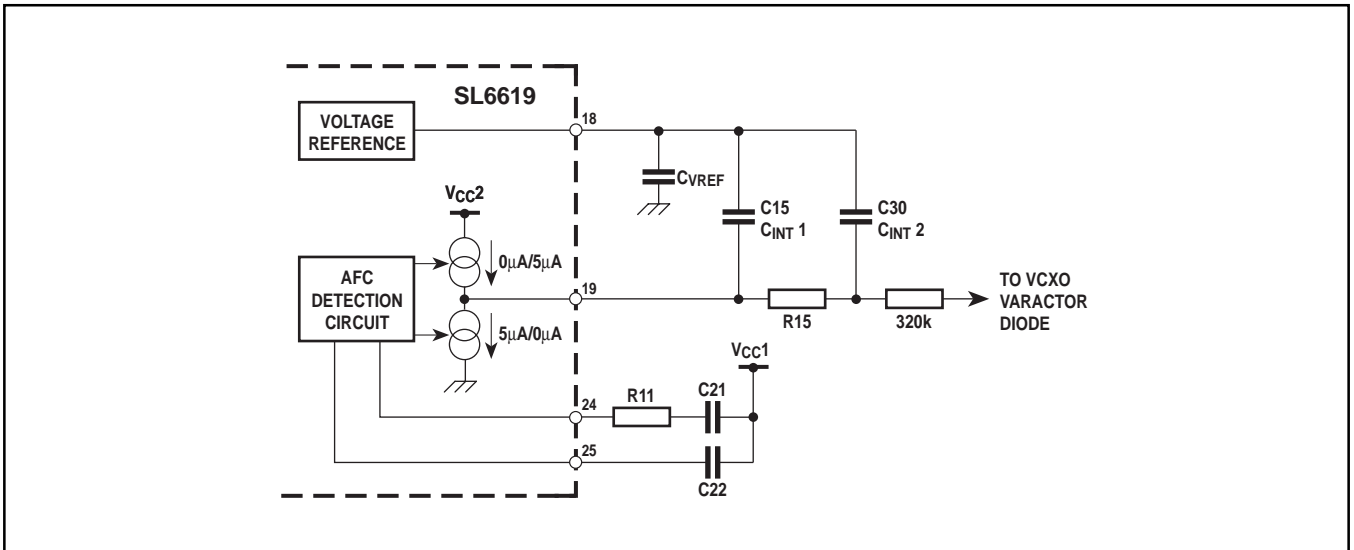


Fig. 4 AFC schematic

| Peak deviation (kHz) | Baud rate (bps) | Component (Fig. 4) |       |      |
|----------------------|-----------------|--------------------|-------|------|
|                      |                 | C22                | C21   | R11  |
| 3.5                  | 512, 1200, 2400 | 750pF              | 2.0nF | 15kΩ |
| 4                    | 512, 1200, 2400 | 560pF              | 1.5nF | 15kΩ |
| 4.5                  | 512, 1200, 2400 | 510pF              | 1.3nF | 15kΩ |
| 5                    | 512, 1200, 2400 | 470pF              | 1.2nF | 15kΩ |
| 5.5                  | 512, 1200, 2400 | 430pF              | 1.1nF | 15kΩ |

Table 2 AFC defining components

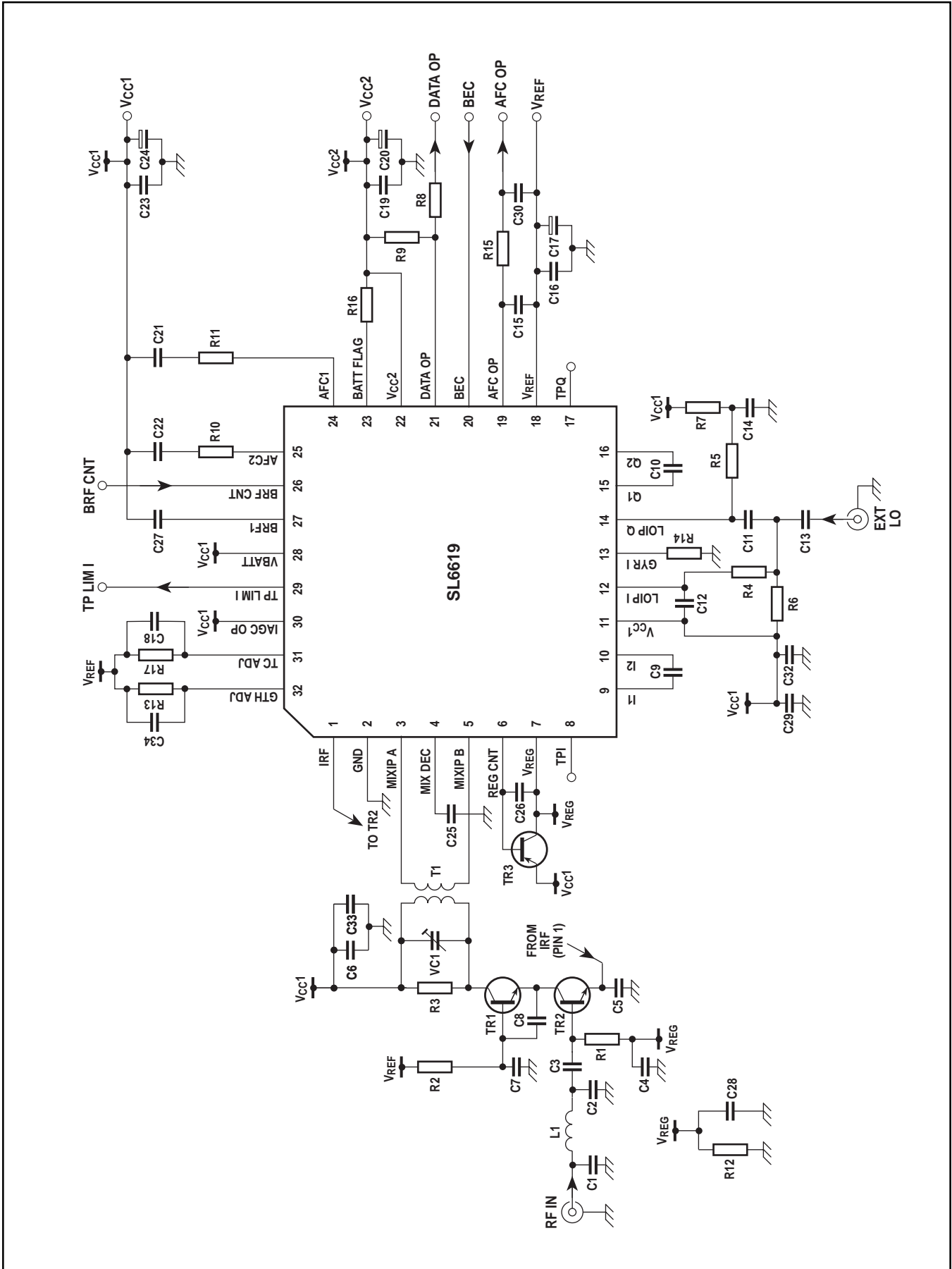


Fig. 5 SL6619 characterisation circuit (see Tables 3 and 4 for component values)

| Resistors |               | Capacitors |             | Capacitors (cont.) |             | Inductors          |                             |
|-----------|---------------|------------|-------------|--------------------|-------------|--------------------|-----------------------------|
| R1        | 4.7k $\Omega$ | C1         | 12pF        | C18                | 100nF       | L1                 | 56nH                        |
| R2        | 4.7k $\Omega$ | C2         | O/C         | C19                | 1nF         | T1                 | 30nH 1:1, Coilcraft M1686-A |
| R3        | 2k $\Omega$   | C3         | 220nF       | C20                | 2.2 $\mu$ F | <b>Transistors</b> |                             |
| R4        | 100 $\Omega$  | C4         | 1nF         | C21                | 1.5nF       | TR1                | Toshiba 2SC5065             |
| R5        | 100 $\Omega$  | C5         | 1nF         | C22                | 560pF       | TR2                | Toshiba 2SC5065             |
| R6        | 100 $\Omega$  | C6         | 1nF         | C23                | 1nF         | TR3                | FMMT589 (Zetex ZTX550)      |
| R7        | 100 $\Omega$  | C7         | 1nF         | C24                | 2.2 $\mu$ F |                    |                             |
| R8        | 430k $\Omega$ | C8         | 3.3pF       | C25                | 100nF       |                    |                             |
| R9        | 220k $\Omega$ | C9         | 4.7nF       | C26                | 100nF       |                    |                             |
| R10       | S/C           | C10        | 4.7nF       | C27                | 560pF       |                    |                             |
| R11       | 15k $\Omega$  | C11        | 4.7pF       | C28                | 1nF         |                    |                             |
| R12       | 2k $\Omega$   | C12        | 5.6pF       | C29                | 1nF         |                    |                             |
| R13       | 33k $\Omega$  | C13        | 1nF         | C30                | 1nF         |                    |                             |
| R14       | 180k $\Omega$ | C14        | 1nF         | C32                | 100nF       |                    |                             |
| R15       | 430k $\Omega$ | C15        | 1nF         | C33                | 100nF       |                    |                             |
| R16       | 220k $\Omega$ | C16        | 1nF         | C34                | 100nF       |                    |                             |
| R17       | 220k $\Omega$ | C17        | 2.2 $\mu$ F | VC1                | 3-10pF      |                    |                             |

Table 3 Component list for 280MHz characterisation board

| Resistors |               | Capacitors |             | Capacitors (cont.) |             | Inductors          |                             |
|-----------|---------------|------------|-------------|--------------------|-------------|--------------------|-----------------------------|
| R1        | 4.7k $\Omega$ | C1         | O/C         | C18                | 100nF       | L1                 | 47nH                        |
| R2        | 4.7k $\Omega$ | C2         | O/C         | C19                | 1nF         | T1                 | 16nH 1:1, Coilcraft Q4123-A |
| R3        | 1.8k $\Omega$ | C3         | 1nF         | C20                | 2.2 $\mu$ F | <b>Transistors</b> |                             |
| R4        | 100 $\Omega$  | C4         | 1nF         | C21                | 1.5nF       | TR1                | Philips BFT25A              |
| R5        | 100 $\Omega$  | C5         | 1nF         | C22                | 560pF       | TR2                | Philips BFT25A              |
| R6        | 100 $\Omega$  | C6         | 1nF         | C23                | 1nF         | TR3                | FMMT589 (Zetex ZTX550)      |
| R7        | 100 $\Omega$  | C7         | 1nF         | C24                | 2.2 $\mu$ F |                    |                             |
| R8        | 430k $\Omega$ | C8         | 3.3pF       | C25                | 100nF       |                    |                             |
| R9        | 220k $\Omega$ | C9         | 4.7nF       | C26                | 100nF       |                    |                             |
| R10       | S/C           | C10        | 4.7nF       | C27                | 560pF       |                    |                             |
| R11       | 15k $\Omega$  | C11        | 3.9pF       | C28                | 1nF         |                    |                             |
| R12       | 2k $\Omega$   | C12        | 3.3pF       | C29                | 1nF         |                    |                             |
| R13       | 33k $\Omega$  | C13        | 1nF         | C30                | 1nF         |                    |                             |
| R14       | 180k $\Omega$ | C14        | 1nF         | C32                | 100nF       |                    |                             |
| R15       | 430k $\Omega$ | C15        | 1nF         | C33                | 100nF       |                    |                             |
| R16       | 220k $\Omega$ | C16        | 1nF         | C34                | 100nF       |                    |                             |
| R17       | 220k $\Omega$ | C17        | 2.2 $\mu$ F | VC1                | 3-10pF      |                    |                             |

Table 4 Component list for 450MHz characterisation board

TYPICAL DC PARAMETERS (FIGS. 6 TO 8)

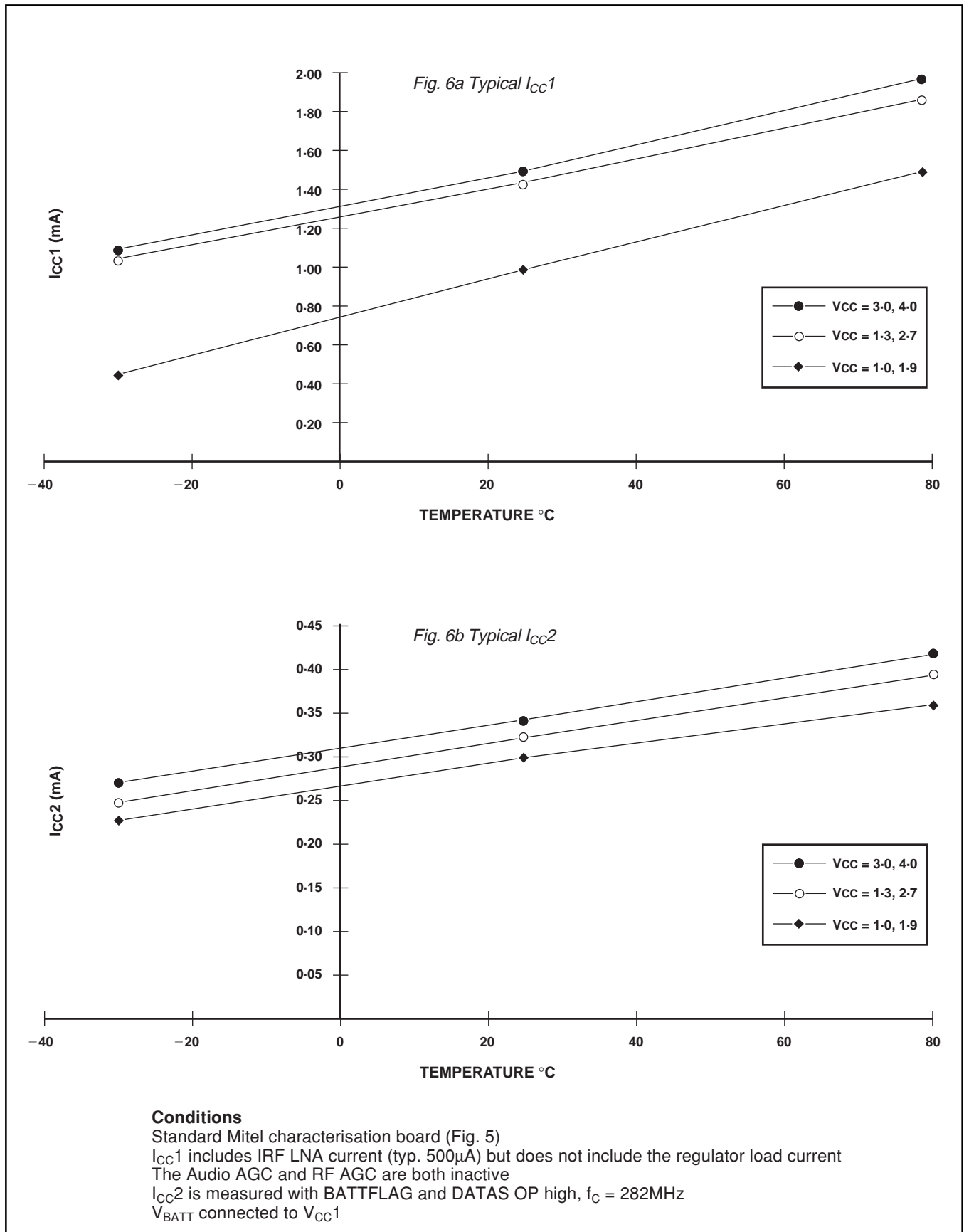


Fig. 6 Typical  $I_{CC1}$  and  $I_{CC2}$  v. supply and temperature

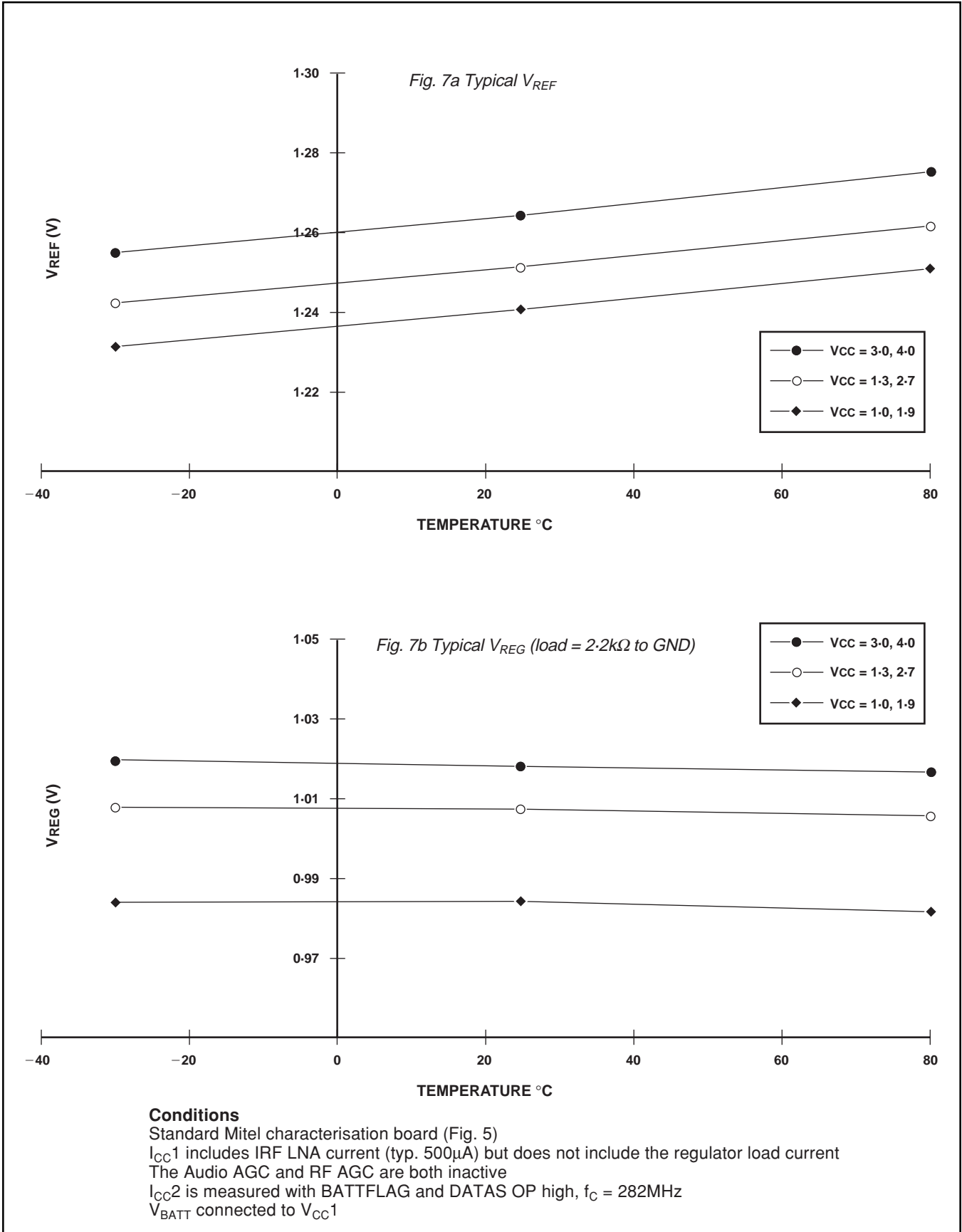
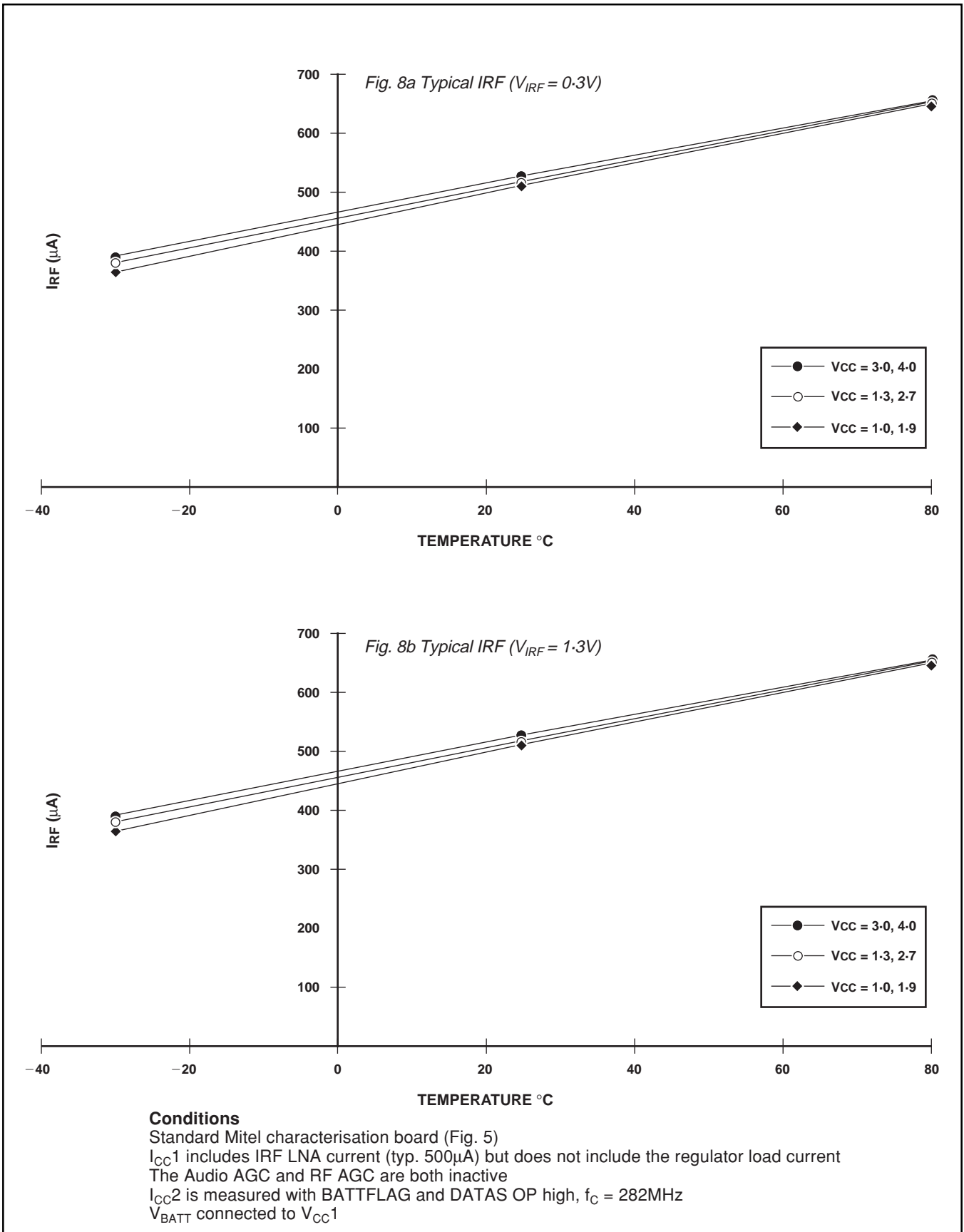


Fig. 7 Typical  $V_{REF}$  and  $V_{REG}$  v. supply and temperature

Fig. 8 Typical  $I_{RF}$  v. supply and temperature

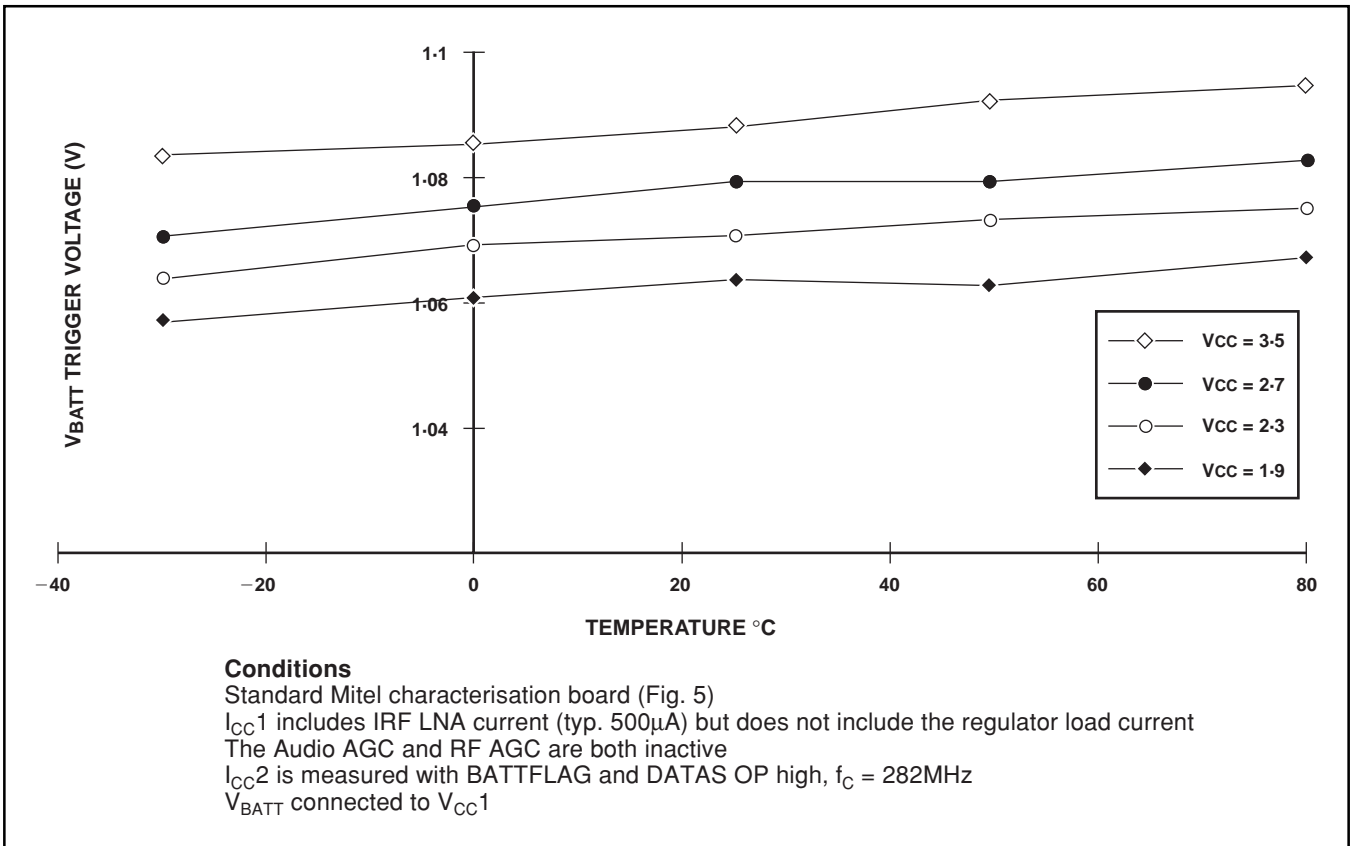


Fig. 9 Typical battery flag trigger voltage ( $V_{BATTFLAG} = V_{CC}/2$ ) v. supply and temperature

TYPICAL AC PARAMETERS (FIGS. 10 TO 13)

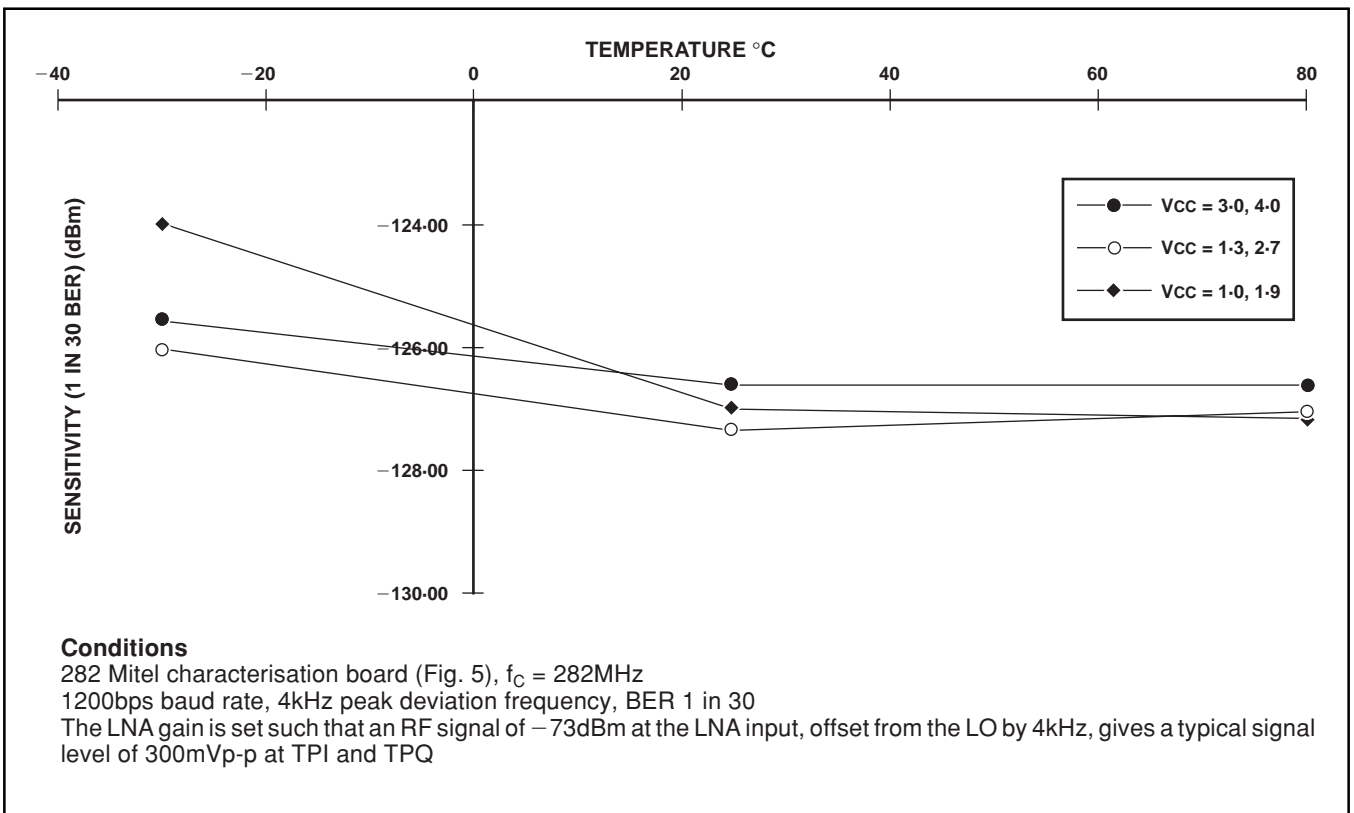


Fig. 10 Typical sensitivity v. supply and temperature



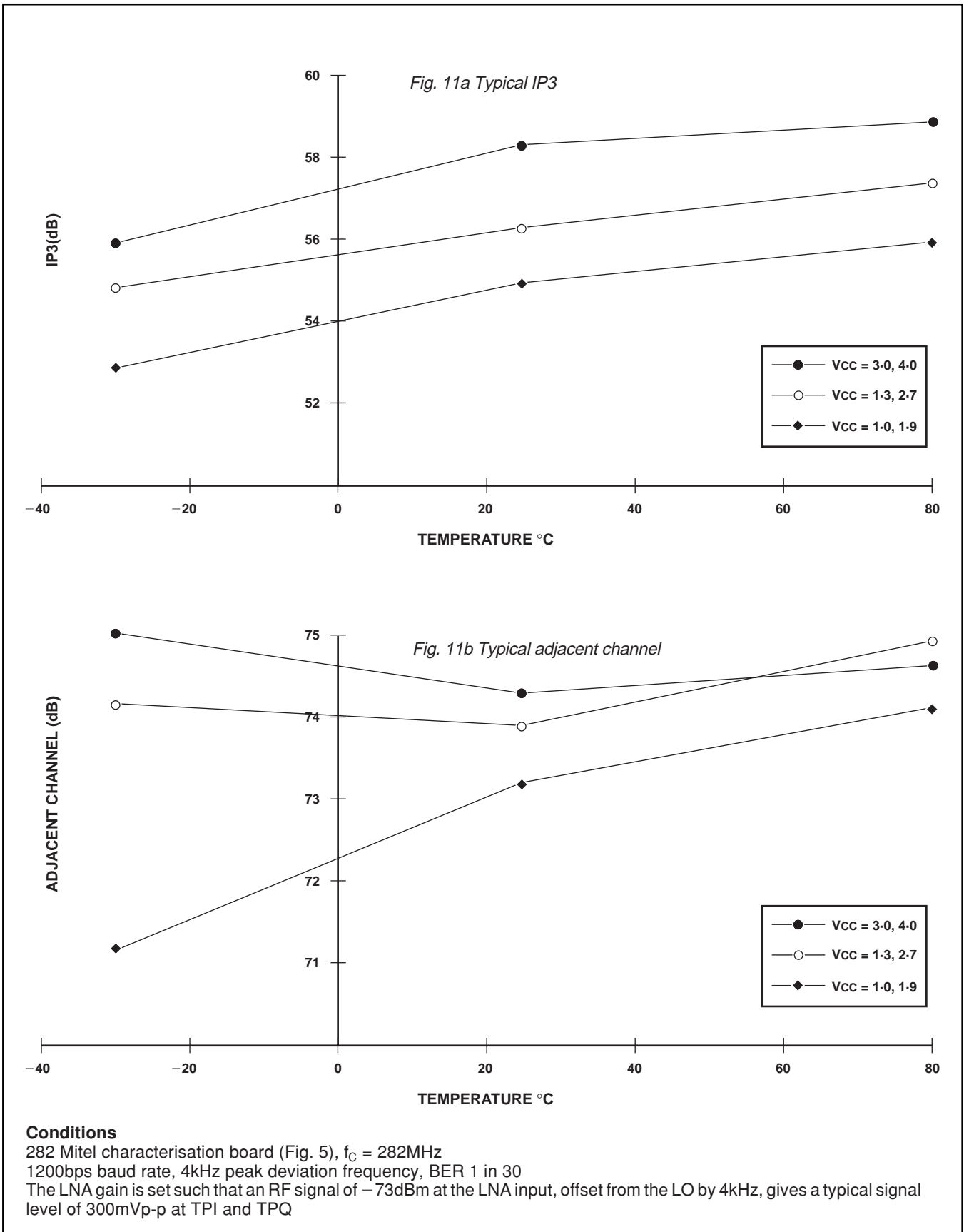


Fig. 11 Typical IP3 and adjacent channel v. supply and temperature

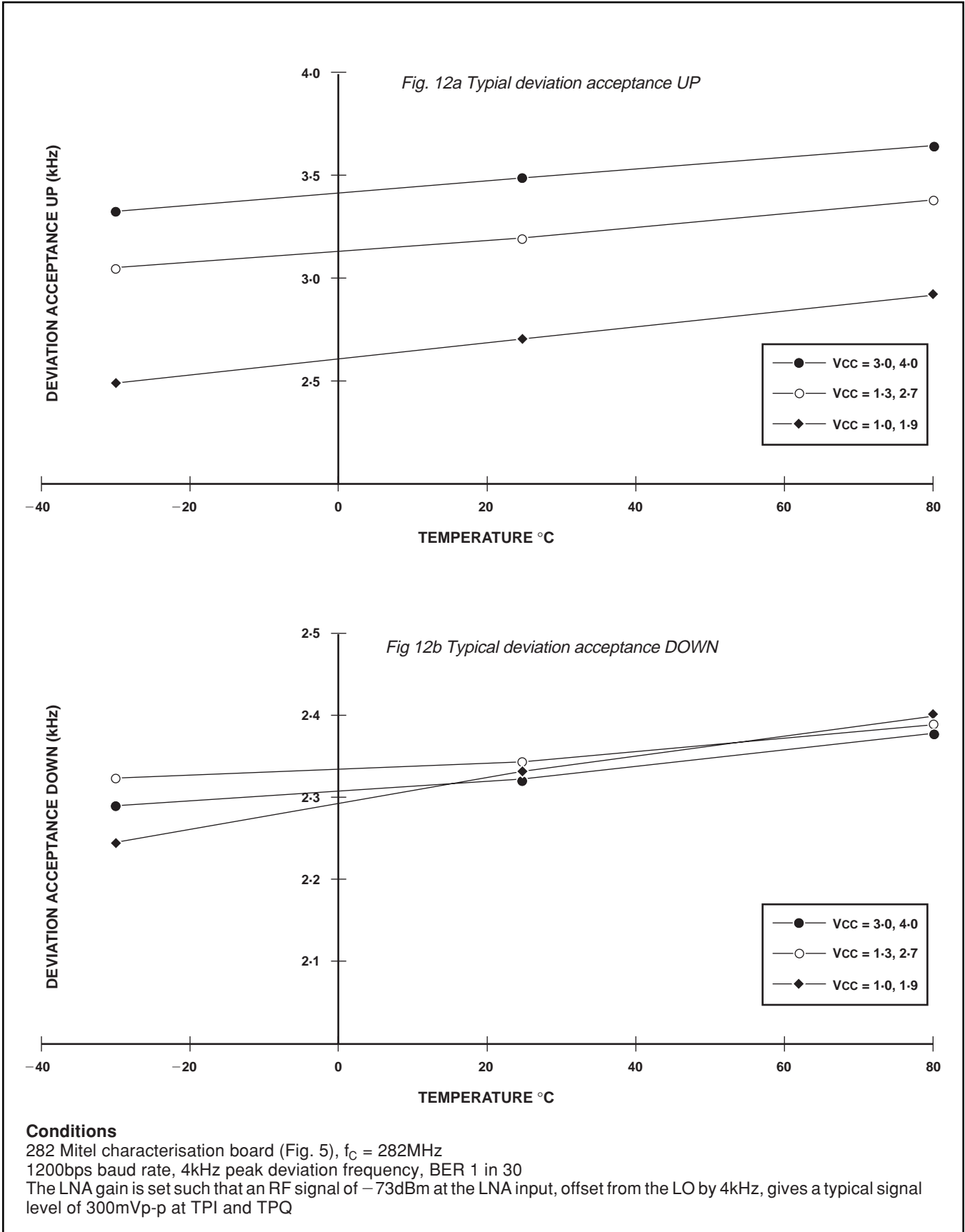


Fig. 12 Typical deviation acceptance v. supply and temperature

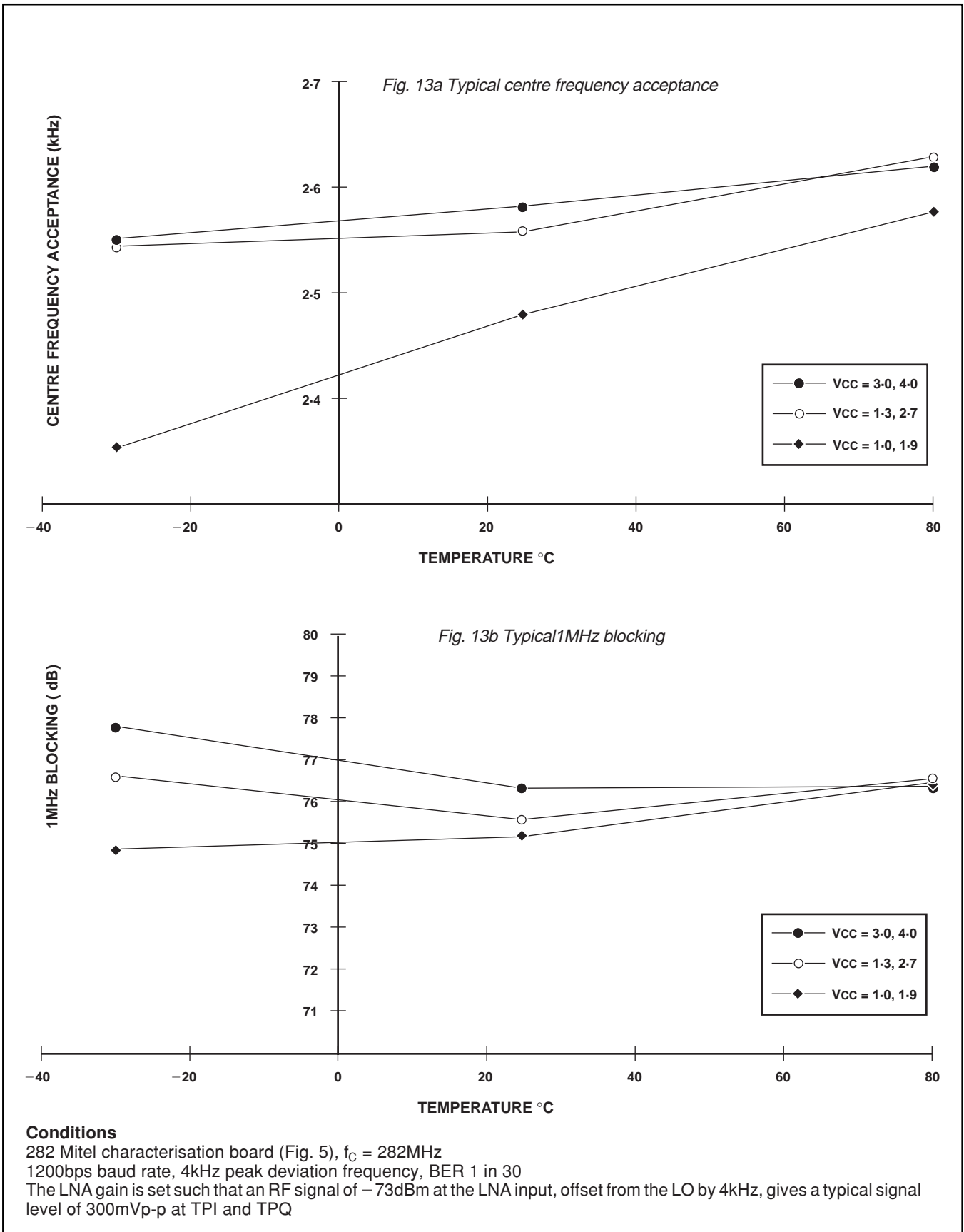
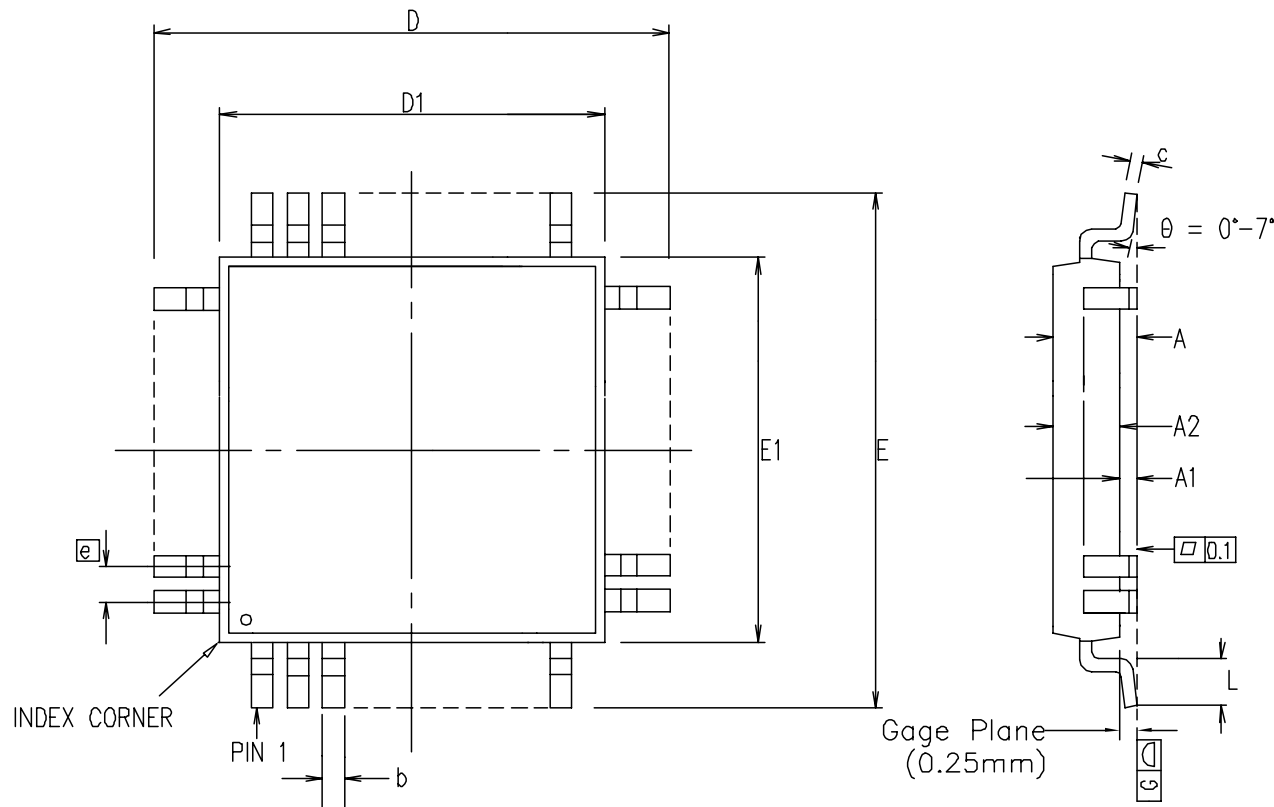


Fig. 13 Typical centre frequency acceptance and 1MHz blocking v. supply and temperature



| Symbol       | Control Dimensions<br>in millimetres |      | Altern. Dimensions<br>in inches |       |
|--------------|--------------------------------------|------|---------------------------------|-------|
|              | MIN                                  | MAX  | MIN                             | MAX   |
| A            | ---                                  | 1.20 | ---                             | 0.047 |
| A1           | 0.05                                 | 0.15 | 0.002                           | 0.006 |
| A2           | 0.95                                 | 1.05 | 0.037                           | 0.041 |
| D            | 9.00 BSC                             |      | 0.354 BSC                       |       |
| D1           | 7.00 BSC                             |      | 0.276 BSC                       |       |
| E            | 9.00 BSC                             |      | 0.354 BSC                       |       |
| E1           | 7.00 BSC                             |      | 0.276 BSC                       |       |
| L            | 0.45                                 | 0.75 | 0.018                           | 0.030 |
| e            | 0.80 BSC                             |      | 0.031 BSC                       |       |
| b            | 0.30                                 | 0.45 | 0.012                           | 0.018 |
| c            | 0.09                                 | 0.20 | 0.004                           | 0.008 |
| Pin features |                                      |      |                                 |       |
| N            | 32                                   |      |                                 |       |
| ND           | 8                                    |      |                                 |       |
| NE           | 8                                    |      |                                 |       |
| NOTE         | SQUARE                               |      |                                 |       |

Conforms to JEDEC MS-026 ABA Iss. C

- Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
  2. Controlling dimensions are in millimeters.
  3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
  4. Dimension D1 and E1 do not include mould protrusion.
  5. Dimension b does not include dambar protrusion.
  6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51612/001 (Swindon)

|          |         |        |  |  |                     |
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| APPROVED |         |        |  |  |                     |

|   |
|---|
| ORIGINATING SITE: SWINDON   |
| Title: Package Outline Drawing for<br>32 lds TQFP (TP)<br>(7x7x1.0) mm, Body+2.0 mm |
| Drawing Number<br>GPD00233  |



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