

Sample-and-Hold Driver IC for LCD

Description

The CXA2504N comprises a 6-channel sample-and-hold circuit and driver for liquid crystal display.

Features

- Built-in sample-and-hold circuit for phase matching
- Sample-and-hold circuit slew rate 280V/μs (Typ.)
- Driver slew rate 190V/μs (Typ.)
(for 300pF load capacitance)
- Sample-and-hold circuit slew rate adjustment function
- Driver slew rate adjustment function

Structure

Bipolar silicon monolithic IC

Applications

- Liquid crystal projectors
- Liquid crystal viewfinders
- Small liquid crystal monitors



Absolute Maximum Ratings (Ta = 25°C)

- | | | | |
|---|------------------------------|--------------------|--------------|
| • Supply voltage | Vcc1 | 17 | V |
| | Vcc2 | 17 | V |
| | Vcc3 | 7 | V |
| • Input pin voltage 1 | VIN1*1 | Vcc1 | V |
| | VIN2*2 | Vcc3 | V |
| • Digital input pin voltage | VP*3 | -0.3 to Vcc3 + 0.3 | V |
| • Operating temperature | Topr | -25 to +75 | °C |
| • Storage temperature | Tstg | -55 to +150 | °C |
| • Allowable power dissipation (Ta ≤ 25°C) | Pd | 1.72*4 | W |
| | • Reduction rate (Ta > 25°C) | | 13.8*4 mW/°C |

Operating Conditions

- | | | | |
|----------------|------|------------|---|
| Supply voltage | Vcc1 | 15.5 ± 0.8 | V |
| | Vcc2 | 15.5 ± 0.8 | V |
| | Vcc3 | 5.0 ± 0.5 | V |

*1 Applies to Pins 4, 5, 6, 7, 8, 13, 14, 15, 16, 24, 26, 28, 34, 36 and 38.

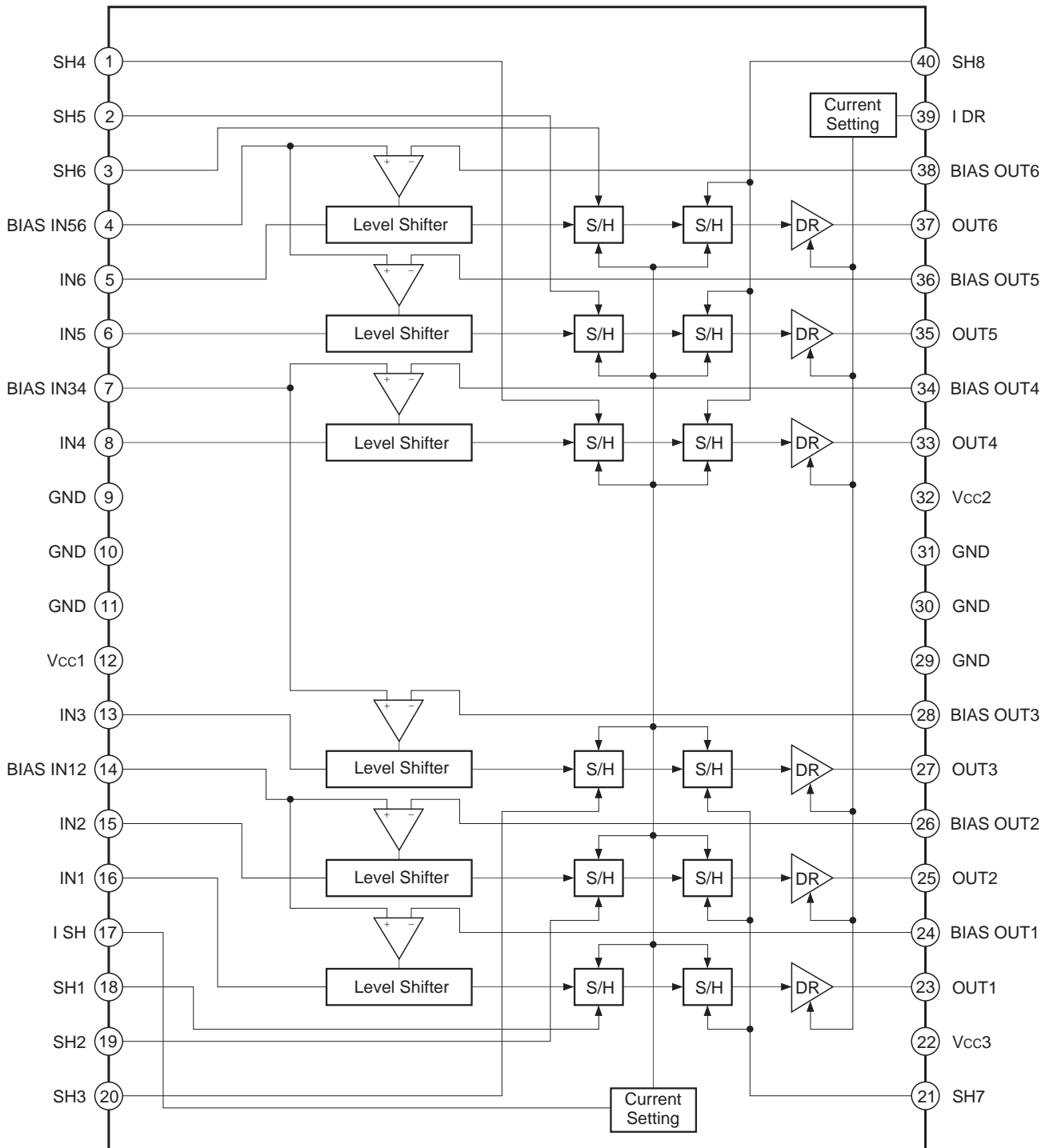
*2 Applies to Pins 17 and 39.

*3 Applies to Pins 1, 2, 3, 18, 19, 20, 21 and 40.

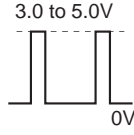
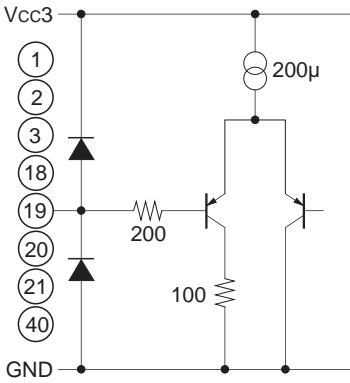
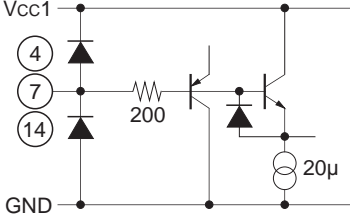
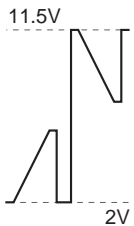
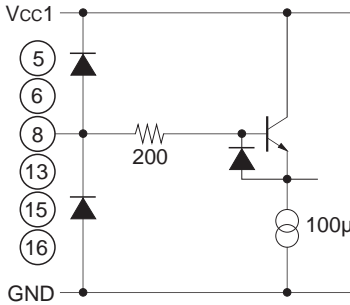
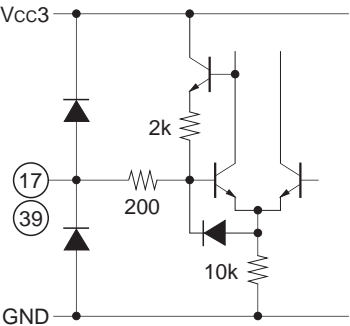
*4 When mounted on 40 × 40mm² square epoxy board.

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Block Diagram



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SH4			CH4 sampling pulse input
2	SH5			CH5 sampling pulse input
3	SH6			CH6 sampling pulse input
18	SH1			CH1 sampling pulse input
19	SH2			CH2 sampling pulse input
20	SH3			CH3 sampling pulse input
21	SH7			Pulse input for simultaneous resampling of CH1, 2, and 3
40	SH8			Pulse input for simultaneous resampling of CH4, 5, and 6
4	BIAS IN56			Inputs IN5 and 6 signal center voltage
7	BIAS IN34			Inputs IN3 and 4 signal center voltage
14	BIAS IN12			Inputs IN1 and 2 signal center voltage
5	IN6			CH6 input*1
6	IN5			CH5 input*1
8	IN4			CH4 input*1
13	IN3			CH3 input*1
15	IN2			CH2 input*1
16	IN1			CH1 input*1
17	I SH	1.2V		Sets sample-and-hold circuit current. Sample-and-hold circuit slew rate changes.
39	I DR	1.2V		Sets output driver circuit current. Output driver circuit slew rate changes.

*1 Do not input a signal of 2V or less to IN1 to IN6.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23	OUT1			CH1 output*2
25	OUT2			CH2 output*2
27	OUT3			CH3 output*2
33	OUT4			CH4 output*2
35	OUT5			CH5 output*2
37	OUT6			CH6 output*2
24	BIAS OUT1			Inputs OUT1 signal center voltage
26	BIAS OUT2			Inputs OUT2 signal center voltage
28	BIAS OUT3			Inputs OUT3 signal center voltage
34	BIAS OUT4			Inputs OUT4 signal center voltage
36	BIAS OUT5			Inputs OUT5 signal center voltage
38	BIAS OUT6			Inputs OUT6 signal center voltage
12	Vcc1	15.5V		Power supply for level shifter and S/H circuit
22	Vcc3	5.0V		5V system power supply
32	Vcc2	15.5V		Output driver power supply
9	GND			GND*3
10	GND			GND*3
11	GND			GND*3
29	GND			GND*3
30	GND			GND*3
31	GND			GND*3

*2 Power consumption varies depending on the output signal when driving load capacitance. Be careful not to go over the package allowable power dissipation.

*3 Pins 9 to 11 and 29 to 31 must be connected to GND potential; they must not be open.

Electrical Characteristics

Unless otherwise specified:

$V_{cc1} = V_{cc2} = 15.5V$, $V_{cc3} = 5.0V$, $T_a = 25^{\circ}C$

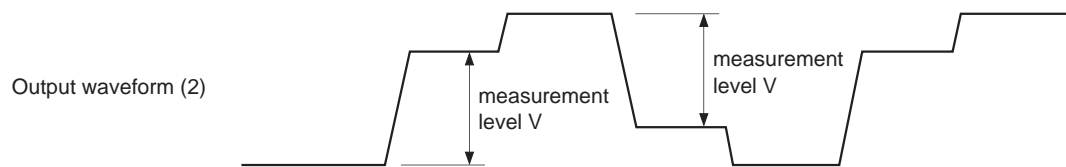
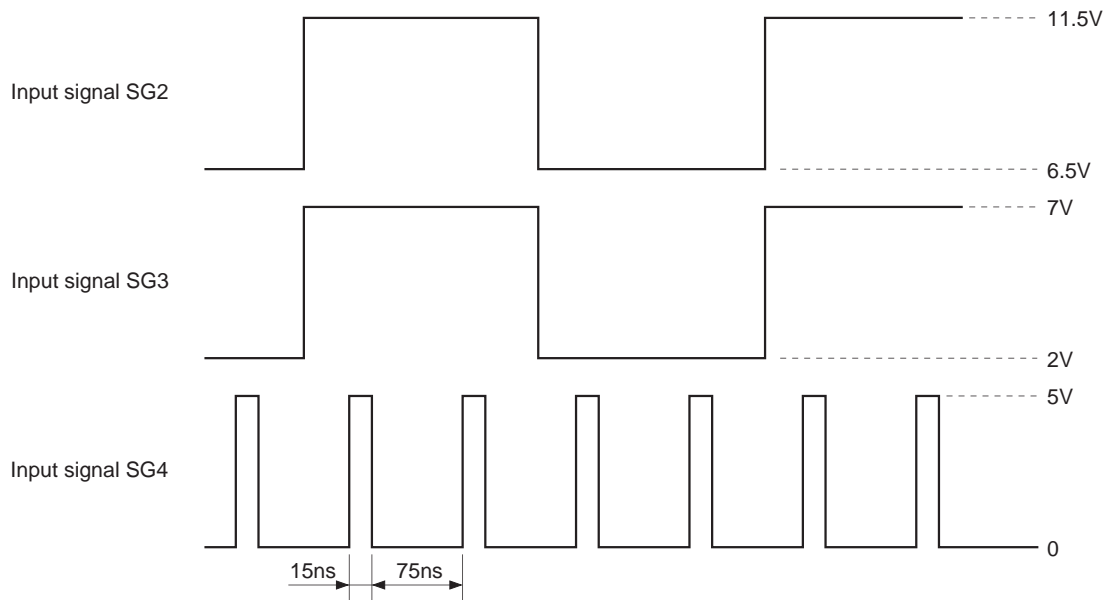
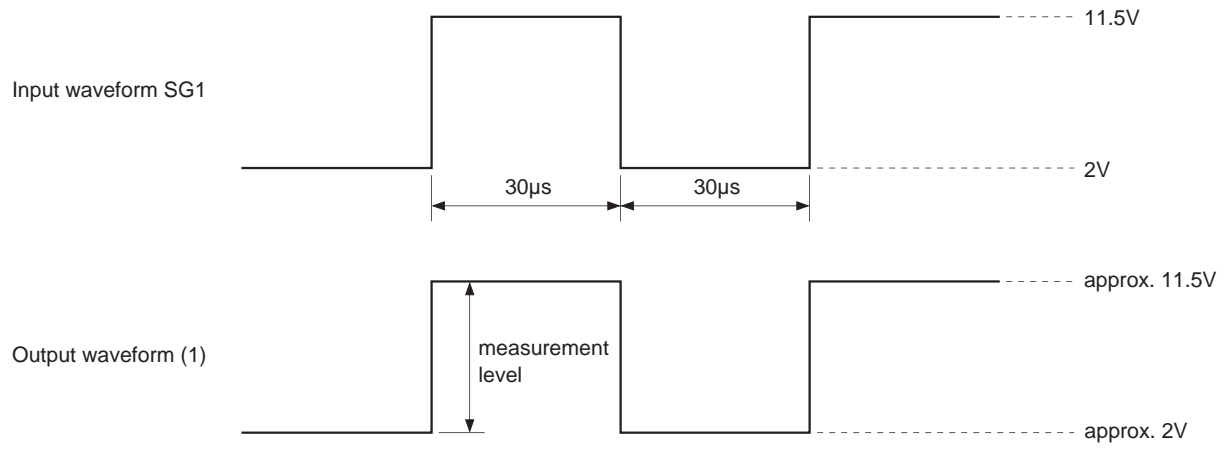
SW1 → b, SW2 → b, SW3 → b, SW4 → b, SW5 → a, SW6 → a, SW7 → b, SW8 → a, SW13 → a, SW14 → b,
SW15 → a, SW16 → a, SW18 → b, SW19 → b, SW20 → b, SW21 → b, SW24 → b, SW26 → b, SW28 → b,
SW34 → b, SW36 → b, SW38 → b, SW40 → b

$V_1 = 5V$, $V_2 = 5V$, $V_3 = 5V$, $V_{18} = 5V$, $V_{19} = 5V$, $V_{20} = 5V$, $V_{21} = 5V$, $V_{40} = 5V$, $C_L = 300pF$

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
1	Current consumption (1)	Icc1	SW5 → b, SW6 → b, SW8 → b, SW13 → b, SW15 → b, SW16 → b, $V_1 = V_6 = V_8 = V_{13} = V_{15} = V_{16} = 7V$	—	17	24	mA
2	Current consumption (2)	Icc2		—	8	14	mA
3	Current consumption (3)	Icc3		—	12	17	mA
4	SH4 "H" pin current	I1H	SW1 → b, $V_1 = 5V$	-0.1	0	0.1	μA
5	SH4 "L" pin current	I1L	SW1 → b, $V_1 = 0V$	-12	-5.0	—	μA
6	SH5 "H" pin current	I2H	SW2 → b, $V_2 = 5V$	-0.1	0	0.1	μA
7	SH5 "L" pin current	I2L	SW2 → b, $V_2 = 0V$	-12	-5.0	—	μA
8	SH6 "H" pin current	I3H	SW3 → b, $V_3 = 5V$	-0.1	0	0.1	μA
9	SH6 "L" pin current	I3L	SW3 → b, $V_3 = 0V$	-12	-5.0	—	μA
10	BIAS IN56 pin current	I4	SW4 → a, $V_4 = 7V$	-0.2	0	0.2	μA
11	IN6 pin current	I5	SW5 → b, $V_5 = 7V$	—	0.5	2.0	μA
12	IN5 pin current	I6	SW6 → b, $V_6 = 7V$	—	0.5	2.0	μA
13	BIAS IN34 pin current	I7	SW7 → a, $V_7 = 7V$	-0.2	0	0.2	μA
14	IN4 pin current	I8	SW8 → b, $V_8 = 7V$	—	0.5	2.0	μA
15	IN3 pin current	I13	SW13 → b, $V_{13} = 7V$	—	0.5	2.0	μA
16	BIAS IN12 pin current	I14	SW14 → a, $V_{14} = 7V$	-0.2	0	0.2	μA
17	IN2 pin current	I15	SW15 → b, $V_{15} = 7V$	—	0.5	2.0	μA
18	IN1 pin current	I16	SW16 → b, $V_{16} = 7V$	—	0.5	2.0	μA
19	SH1 "H" pin current	I18H	SW18 → b, $V_{18} = 5V$	-0.1	0	0.1	μA
20	SH1 "L" pin current	I18L	SW18 → b, $V_{18} = 0V$	-12	-5	—	μA
21	SH2 "H" pin current	I19H	SW19 → b, $V_{19} = 5V$	-0.1	0	0.1	μA
22	SH2 "L" pin current	I19L	SW19 → b, $V_{19} = 0V$	-12	-5	—	μA
23	SH3 "H" pin current	I20H	SW20 → b, $V_{20} = 5V$	-0.1	0	0.1	μA
24	SH3 "L" pin current	I20L	SW20 → b, $V_{20} = 0V$	-12	-5	—	μA
25	SH7 "H" pin current	I21H	SW21 → b, $V_{21} = 5V$	-0.1	0	0.1	μA
26	SH7 "L" pin current	I21L	SW21 → b, $V_{21} = 0V$	-12	-5	—	μA
27	BIAS OUT1 pin current	I24	SW24 → a, $V_{24} = 7V$	-0.2	0	0.2	μA
28	BIAS OUT2 pin current	I26	SW26 → a, $V_{26} = 7V$	-0.2	0	0.2	μA
29	BIAS OUT3 pin current	I28	SW28 → a, $V_{28} = 7V$	-0.2	0	0.2	μA
30	BIAS OUT4 pin current	I34	SW34 → a, $V_{34} = 7V$	-0.2	0	0.2	μA
31	BIAS OUT5 pin current	I36	SW36 → a, $V_{36} = 7V$	-0.2	0	0.2	μA

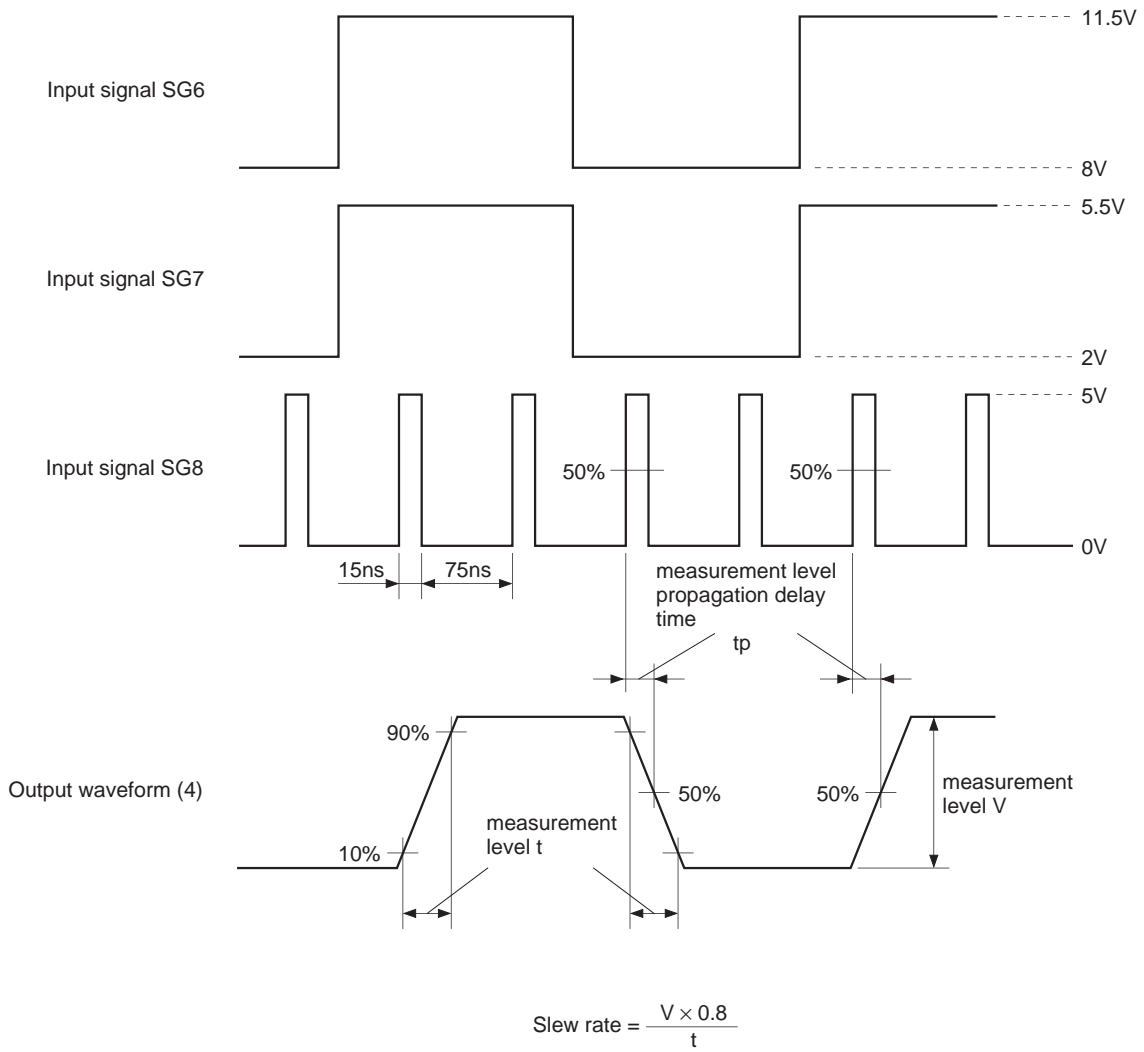
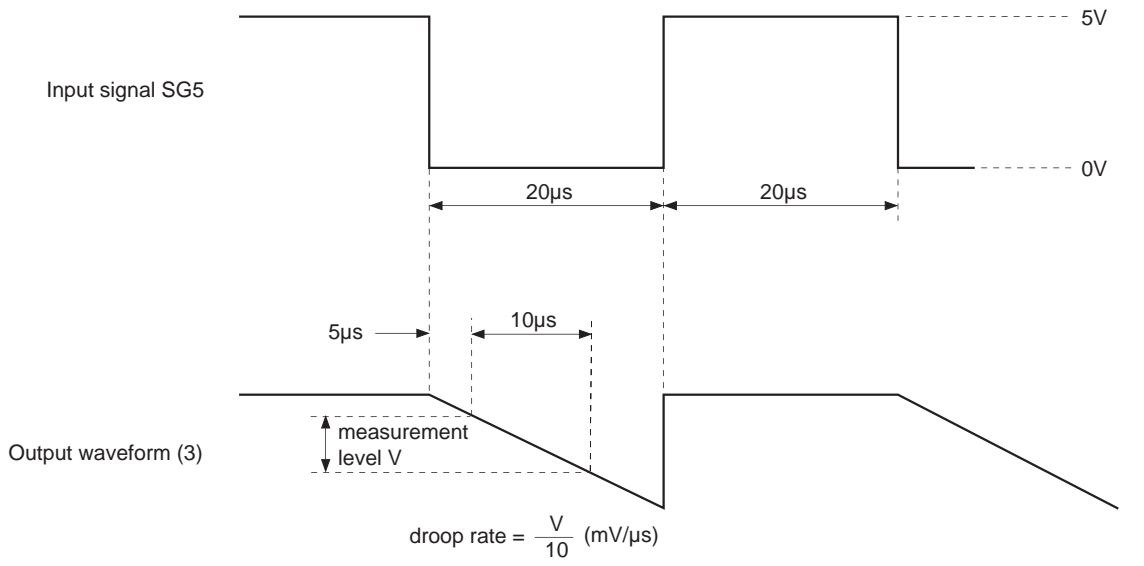
No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
32	BIAS OUT6 pin current	I ₃₈	SW38 → a, V ₃₈ = 7V	-0.2	0	0.2	μA
33	SH8 "H" pin current	I _{40H}	SW40 → b, V ₄₀ = 5V	-0.1	0	0.1	μA
34	SH8 "L" pin current	I _{40L}	SW40 → b, V ₄₀ = 0V	-12	-5	—	μA
35	I SH pin voltage	V ₁₇		—	1.2	—	V
36	I DR pin voltage	V ₃₉		—	1.2	—	V
37	Output potential difference between channels	ΔV _O	Set SW5 → b, SW6 → b, SW8 → b, SW13 → b, SW15 → b, SW16 → b, V ₅ = V ₆ = V ₈ = V ₁₃ = V ₁₅ = V ₁₆ = 2V, 7V, 11.5V. Measure output DC voltage for TP23, TP25, TP27, TP33, TP35 and TP37 relative to each input DC voltage. ΔV _O = MAX (output voltage – input voltage) – MIN (output voltage – input voltage)	—	—	25	mV
38	Gain difference between channels	ΔV _d	Set SW4 → a, SW5 → b, SW6 → b, SW7 → a, SW8 → b, SW13 → b, SW14 → a, SW15 → b, SW16 → b, SW24 → a, SW26 → b, SW28 → b, SW34 → b, SW36 → b, SW38 → b, V ₄ = V ₇ = V ₁₄ = V ₂₄ = V ₂₆ = V ₂₈ = V ₃₄ = V ₃₆ = V ₃₈ = 7V, V ₅ = V ₆ = V ₈ = V ₁₃ = V ₁₅ = V ₁₆ = 2V, 11.5V. Measure output DC voltage for TP23, TP25, TP27, TP33, TP35 and TP37 relative to each input DC voltage. ΔV _{dmax} = MAX (output voltage (11.5V input) – output voltage (2.0V input)) ΔV _{dmin} = MIN (output voltage (11.5V input) – output voltage (2.0V input)) And, calculate the difference between channels of its voltage difference. ΔV _d = ΔV _{dmax} – ΔV _{dmin}	—	—	25	mV
39	Input/output gain	G _{IO}	Set SW4 → a, SW7 → a, SW14 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, V ₄ = V ₇ = V ₁₄ = V ₂₄ = V ₂₆ = V ₂₈ = V ₃₄ = V ₃₆ = V ₃₈ = 7V. Input SG1 to (IN1) to (IN6) and measure gain between input and output for TP23, TP25, TP27, TP33, TP35 and TP37 (refer to output waveforms (1)).	-0.5	-0.1	—	dB
40	Sample-and-hold slew rate (1)	R _{TSH1}	Set SW1 → a, SW2 → a, SW3 → a, SW4 → a, SW7 → a, SW14 → a, SW18 → a, SW19 → a, SW20 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, V ₄ = V ₇ = V ₁₄ = V ₂₄ = V ₂₆ = V ₂₈ = V ₃₄ = V ₃₆ = V ₃₈ = 7V, (SH1) to (SH6) = SG4. Input SG2 and SG3 to (IN1) to (IN6) and measure output waveform (2) V for TP23, TP25, TP27, TP33, TP35 and TP37. $R_{TSH1} = \frac{V}{15 \times 10^{-3}} \text{ (V/}\mu\text{s)}$	220	280	—	V/μs
41	Sample-and-hold slew rate (2)	R _{TSH2}	Set SW4 → a, SW7 → a, SW14 → a, SW21 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, SW40 → a, V ₄ = V ₇ = V ₁₄ = V ₂₄ = V ₂₆ = V ₂₈ = V ₃₄ = V ₃₆ = V ₃₈ = 7V, (SH7) = (SH8) = SG4. Input SG2 and SG3 to (IN1) to (IN6) and measure output waveform (2) V for TP23, TP25, TP27, TP33, TP35 and TP37. $R_{TSH2} = \frac{V}{15 \times 10^{-3}} \text{ (V/}\mu\text{s)}$	220	280	—	V/μs

No.	Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
42	Sample-and-hold droop rate (1)	RD1	Set SW1 → a, SW2 → a, SW3 → a, SW4 → a, SW5 → b, SW6 → b, SW7 → a, SW8 → b, SW13 → b, SW14 → a, SW15 → b, SW16 → b, SW18 → a, SW19 → a, SW20 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, V4 = V7 = V14 = V24 = V26 = V28 = V34 = V36 = V38 = 7V, (SH1) to (SH6) = SG5, V5 = V6 = V8 = V13 = V15 = V16 = 2V, 7V, 11.5V. Measure output waveform (3) V for TP23, TP25, TP27, TP33, TP35 and TP37 relative to each input DC. $RD1 = \frac{V}{10}$ (mV/μs)	—	—	±40	mV/ μs
43	Sample-and-hold droop rate (2)	RD2	Set SW4 → a, SW5 → b, SW6 → b, SW7 → a, SW8 → b, SW13 → b, SW14 → a, SW15 → b, SW16 → b, SW21 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, SW40 → a, V4 = V7 = V14 = V24 = V26 = V28 = V34 = V36 = V38 = 7V, (SH7) = (SH8) = SG5, V5 = V6 = V8 = V13 = V15 = V16 = 2V, 7V, 11.5V. Measure output waveform (3) V for TP23, TP25, TP27, TP33, TP35 and TP37 relative to each input DC. $RD2 = \frac{V}{10}$ (mV/μs)	—	—	±40	mV/ μs
44	Driver slew rate	RTDR	Set SW4 → a, SW7 → a, SW14 → a, SW21 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, SW40 → a, V4 = V7 = V14 = V24 = V26 = V28 = V34 = V36 = V38 = 7V, (SH7) = (SH8) = SG8. Input SG6 and SG7 to (IN1) to (IN6) and measure output waveform (4) t and V for TP23, TP25, TP27, TP33, TP35 and TP37. $RTDR = \frac{V \times 0.8}{t}$ (V/μs)	130	190	—	V/μs
45	SH7, SH8 → output propagation delay time	t _{PLH} (H) t _{PHL} (H) t _{PLH} (L) t _{PHL} (L)	Set SW4 → a, SW7 → a, SW14 → a, SW21 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, SW40 → a, V4 = V7 = V14 = V24 = V26 = V28 = V34 = V36 = V38 = 7V, (SH7) = (SH8) = SG8. Input SG6 and SG7 to (IN1) to (IN6) and for each of the four conditions for input signal rise and fall, measure output waveform (4) t _P for TP23, TP25, TP27, TP33, TP35 and TP37.	13	17	21	ns
46	Input → output propagation delay time	t _{DLH} (H) t _{DHL} (H) t _{DLH} (L) t _{DHL} (L)	Set SW4 → a, SW7 → a, SW14 → a, SW24 → a, SW26 → a, SW28 → a, SW34 → a, SW36 → a, SW38 → a, V4 = V7 = V14 = V24 = V26 = V28 = V34 = V36 = V38 = 7V, CL = 0pF. Input SG9 and SG10 to (IN1) to (IN6) and for each of the four conditions for input signal rise and fall, measure output waveform (5) t _D for TP23, TP25, TP27, TP33, TP35 and TP37.	7	10	13	ns
47	Input dynamic range	V _{DIN}		2.0	—	11.5	V

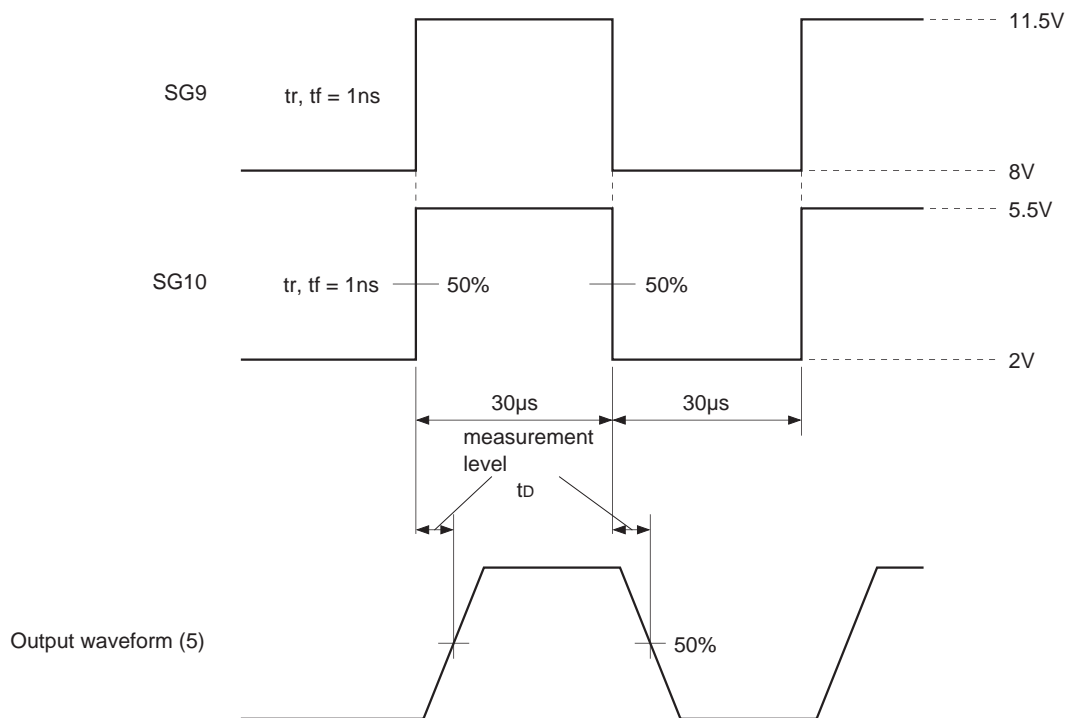


$$\text{Sample-and-hold slew rate} = \frac{V}{15 \times 10^{-3}}$$

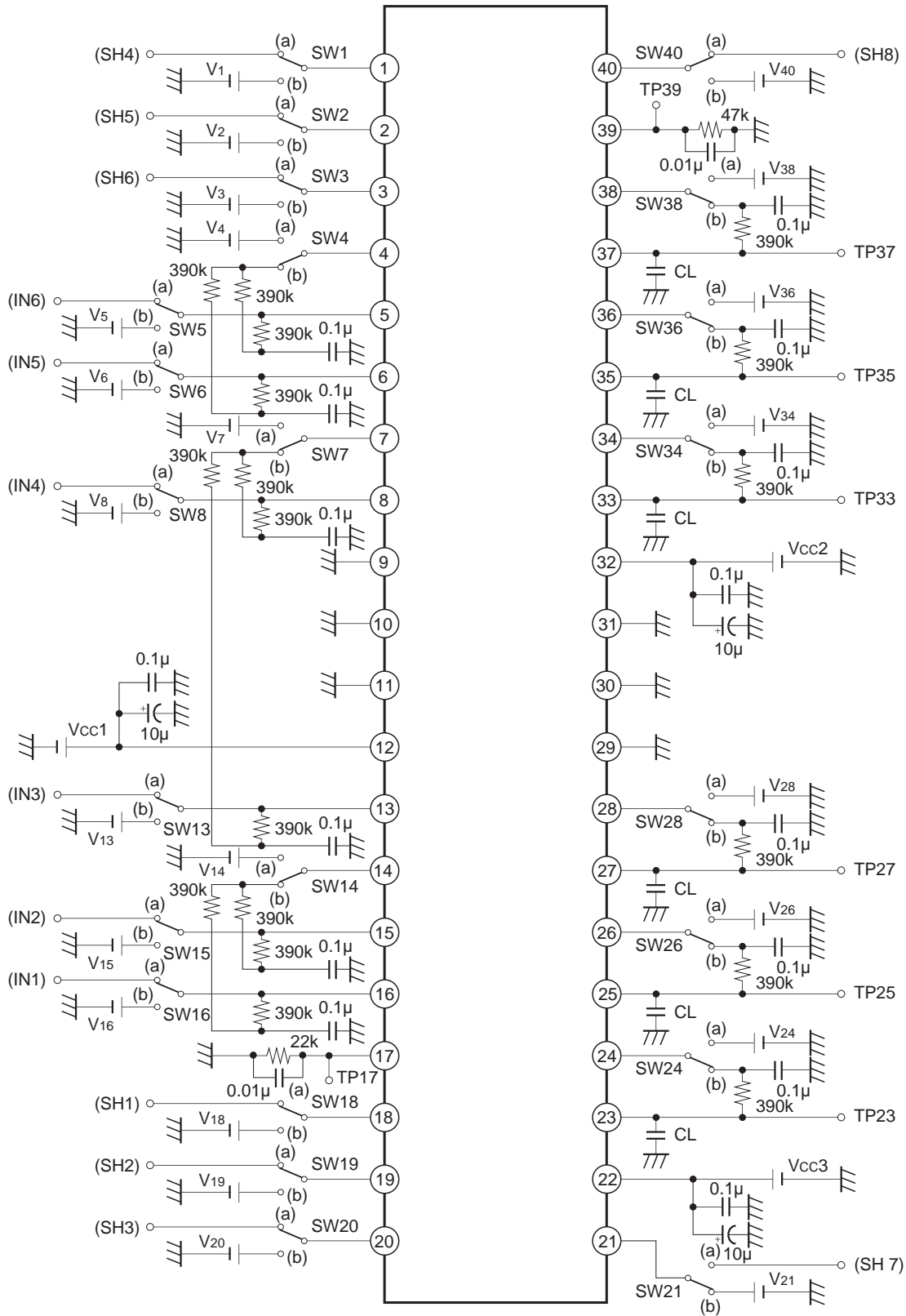
SG2 and SG3 must change completely within SG4 "L" interval.



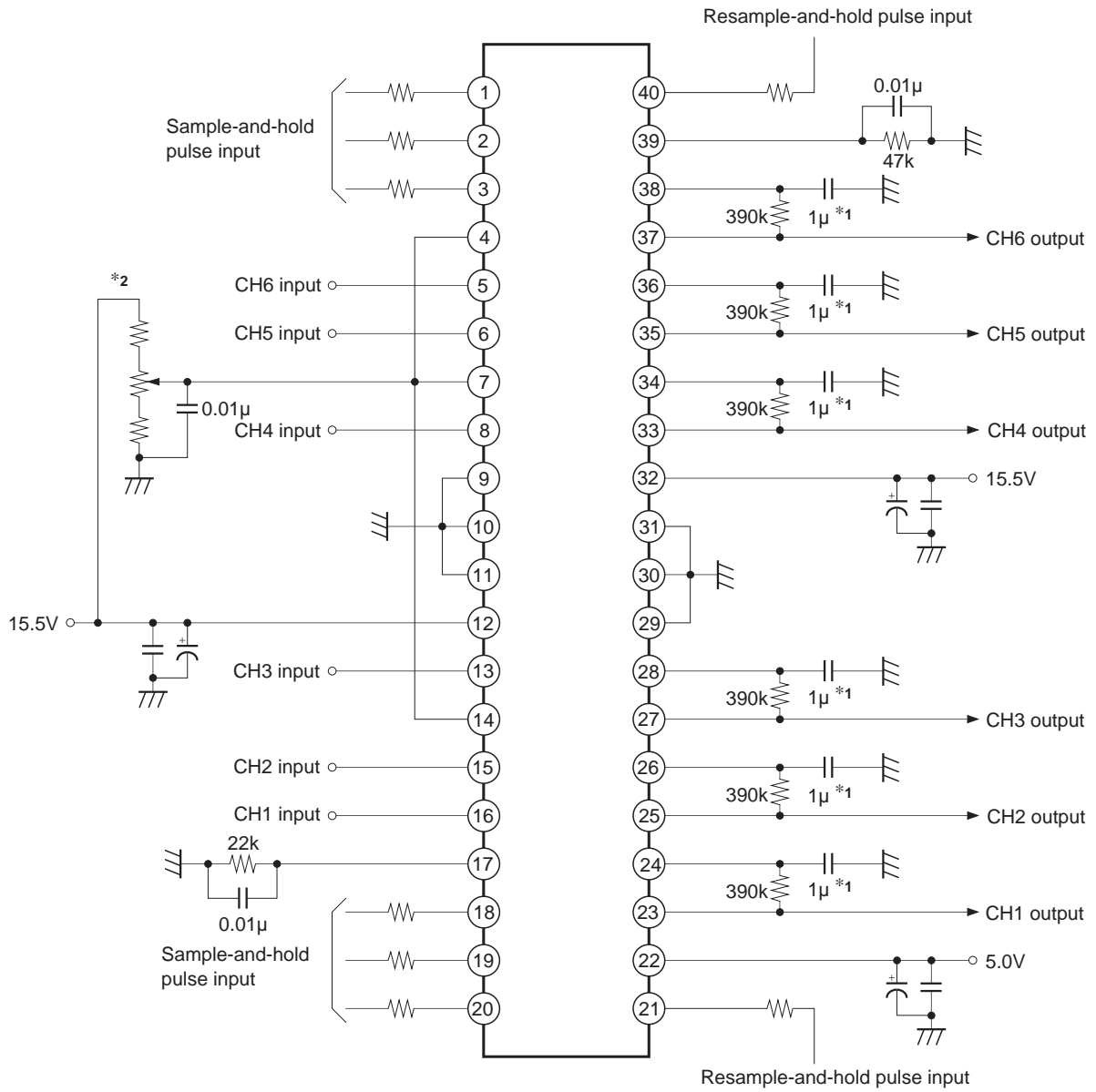
SG5 and SG6 must change completely within SG7 "L" interval.



Electrical Characteristics Measurement Circuit



Application Circuit



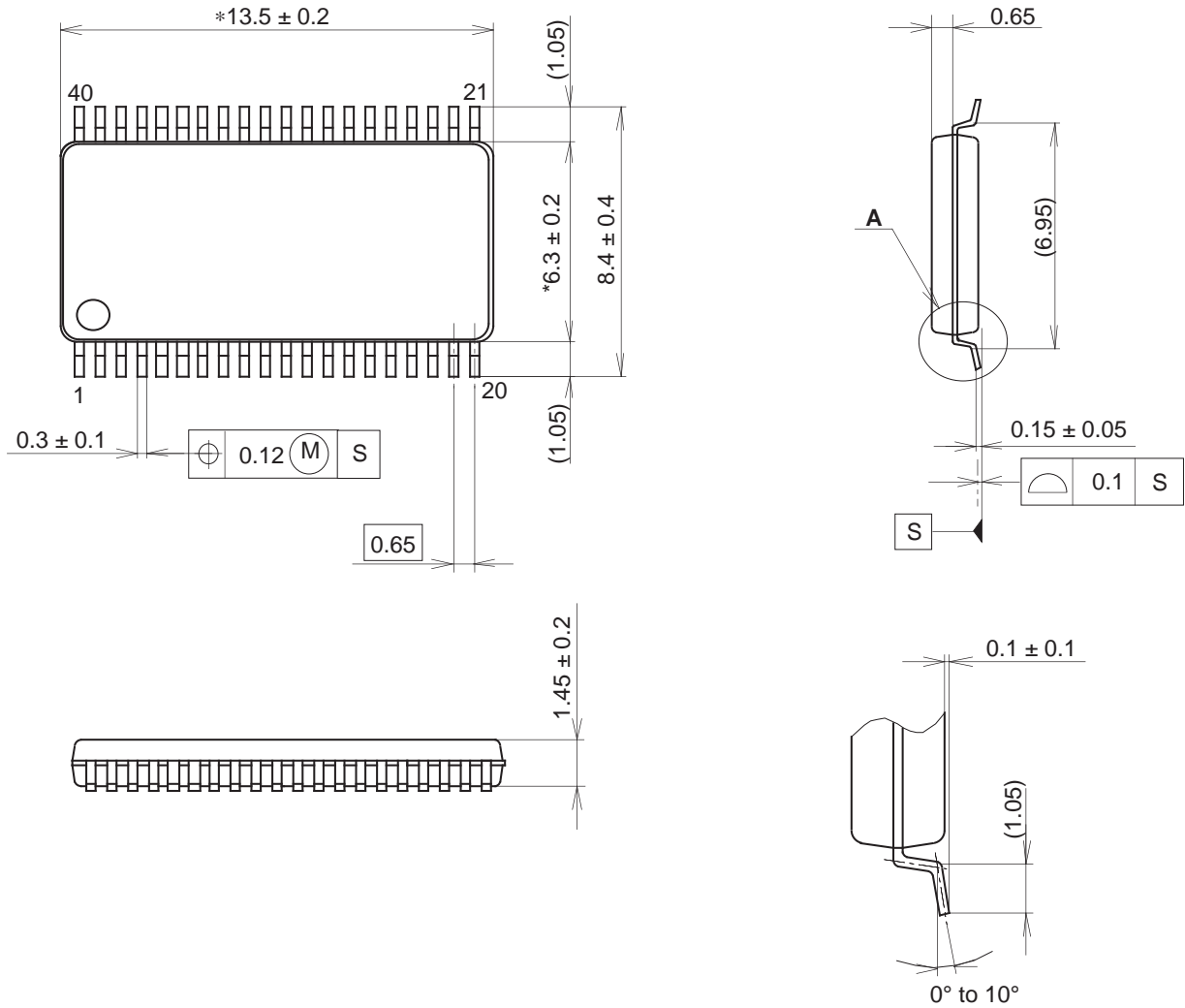
*1 Use a ceramic capacitor with low leak.

*2 Adjust to CH1 to 6 input signal DC voltage (within $\pm 150\text{mV}$).

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

40PIN SSOP(PLASTIC)



NOTE : “*” Dimensions do not include mold protrusion.

DETAIL A

PACKAGE STRUCTURE

SONY CODE	SSOP-40P-L111
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g