REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table I: Correct limits, figure I: Correct case outline. Editorial changes throughout.	92-02-21	Monica L. Poelking
B	Changes in accordance with NOR 5962-R098-93	93-03-10	Monica L. Poelking
C	Add device 02. Editorial changes throughout.	94-04-25	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
Tim H. Noh

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
28 March 1990

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 56-BIT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON

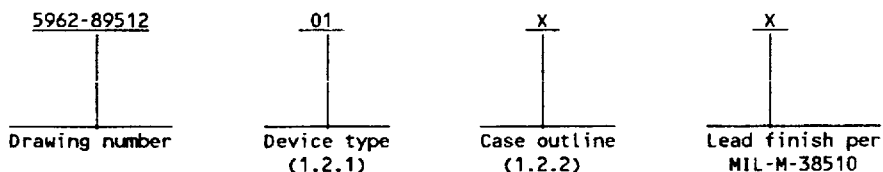| SIZE A	CAGE CODE 67268	5962-89512
SHEET	1	OF	48

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1. SCOPE

1.1 <u>Scope</u>. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 <u>Part or Identifying Number (PIN)</u>. The complete PIN shall be as shown in the following example:

```
5962-89512          01          X          X
     |               |           |          |
     |               |           |          |
     |               |           |          |
Drawing number   Device type  Case outline  Lead finish per
                   (1.2.1)      (1.2.2)      MIL-M-38510
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1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	56001-20	56-bit general purpose DSP
02	56001A-20	56-bit general purpose DSP

1.2.2 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA5-P88	88	Pin grid array
Y	See figure 1	100	Leaded chip carrier

1.3 <u>Absolute maximum ratings</u>.

Supply voltage range with respect to GND (V_{CC}) - - - - - - - - -0.3 V dc to +7.0 V dc
Input voltage (V_{IN})- -0.5 V dc to V_{CC}
Storage temperature range- - - - - - - - - - - - - - - - - - - -65°C to +150°C
Maximum power dissipation
    device 01 - 1.1 W
    device 02 - 0.63 W
Maximum operating temperature (T_C) - - - - - - - - - - - - - -55°C to +125°C
Lead temperature (soldering, 5 seconds)- - - - - - - - - - - - +270°C
Junction temperature (T_J)- - - - - - - - - - - - - - - - - - - +150°C
Thermal resistance, junction-to-case (θ_{JC}):
    Case X - See MIL-STD-1835
    Case Y - 10°C/W

1.4 <u>Recommended operating conditions</u>.

Supply voltage (V_{CC})
    device 01 - 4.5 V dc to 5.5 V dc
    device 02 - 4.75 V dc to 5.25 V dc
High level input voltage (V_{IH}) - - - - - - - - - - - - - - - 2 V dc to V_{CC}
Low level input voltage (V_{IL})- - - - - - - - - - - - - - - - -0.5 V dc to 0.8 V dc
Minimum high level output voltage (V_{OH})- - - - - - - - - - - 2.4 V dc
Maximum low level output voltage (V_{OL}) - - - - - - - - - - - 0.8 V dc
Frequency of operation - 4.0 to 20.5 MHz
Case operating temperature - - - - - - - - - - - - - - - - - - -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
2/ $V_{IL} \leq 0.2$ V dc, $V_{IH} \geq V_{CC} - 2.0$ V dc. No dc loads. EXTAL is driven by a square wave.
3/ In order to obtain these results all inputs must be terminated, i.e., not allowed to float.

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standard, and bulletin</u>. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

  MILITARY

    MIL-M-38510   -   Microcircuits, General Specification for.

STANDARD

  MILITARY

    MIL-STD-883   -   Test Methods and Procedures for Microelectronics.
    MIL-STD-1835   -   Microcircuit Case Outlines.

BULLETIN

  MILITARY

    MIL-BUL-103   -   List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.2 herein and figure 1

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Block diagram</u>. The block diagram shall be as specified on figure 3.

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3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

    a. Burn-in test, method 1015 of MIL-STD-883.

    (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall include the requirements for inputs, outputs, biases, and power dissapation, as applicable, in accordance with the specified purpose of method 1015.

    (2) T_A = +125°C, minimum.

    b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE I. <u>Electrical performance characteristics.</u>

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Input high voltage Except EXTAL, RESET, MODA, MODB	V_{IH}		1, 2, 3	All	2.0	V_{CC}	V
Input low voltage Except EXTAL, MODA, MODB	V_{IL}				-0.5	0.8	
Input high voltage: EXTAL	V_{IHC}			01	V_{CC} - 0.2	V_{CC}	
				02	4.0	V_{CC}	
Input low voltage: EXTAL	V_{ILC}			01	-0.5	0.4	
				02	-0.5	0.6	
Input high voltage: RESET	V_{IHR}			All	2.5	V_{CC}	
Input low voltage: RESET	V_{ILR}			01		0.6	
				02	-0.5	0.8	
Input high voltage: MODA, MODB	V_{IHM}			All	3.5	V_{CC}	
Input low voltage: MODA, MODB	V_{ILM}			01	-0.5	0.6	
				02	-0.5	2.0	
Input leakage current: EXTAL, RESET, MODA, MODB, BR	I_{IN}		1, 2, 3	01	-1.0	1.0	μA
			1, 2	02	-1.0	1.0	
			3	02	-10	-10	
Three state input current	I_{TSI}	$V_{CC} = V_{CC}$ max $V_{IH} = 2.4$ V, $V_{IL} = 0.5$ V	1, 2, 3	All	-10	10	
Output high voltage	V_{OHC}	$V_{CC} = V_{CC}$ min $I_{OH} = -10$ μA		01	4.3		V
Output high voltage	V_{OH}	$V_{CC} = V_{CC}$ min $I_{OH} = -400$ μA		All	2.4		
Output low voltage	V_{OLC}	$V_{CC} = V_{CC}$ min $I_{OL} = -10$ μA		01		0.1	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Output low voltage: Except HREQ	V_{OL}	$V_{CC} = V_{CC}$ min $I_{OL} = 1.6$ mA	1, 2, 3	All		0.4	V
Output low voltage: Open drain output HREQ	V_{OLOD}	$V_{CC} = V_{CC}$ min $I_{OL} = 6.7$ mA		01		0.8	
Total supply current	I_{DD}	$V_{CC} = V_{CC}$ max $V_{DD} = 5.0$ V, $f_o = 20.5$ MHz		01		200	mA
				02		115	
Total supply current: In WAIT mode 2/	I_{IDW}	$V_{CC} = V_{CC}$ max		01		50	
				02		20	
Total supply current: In STOP mode 2/	I_{DDS}			01		10	
				02		2	
Input capacitance	C_{IN}	See 4.3.1c	4	All		10	pF
Functional test		See 4.3.1d	7, 8	All			
Frequency of operation	f_o	$V_{CC} = V_{CC}$ min EXTAL pin	9,10,11	All	4.0	20.5	MHz
External clock input high	1	EXTAL pin, see figure 4 external clock timing		All	22	150	ns
External clock input low	2	$V_{CC} = V_{CC}$ min 3/ 4/			22	150	
Clock cycle time = 2T	3	See figure 4 external clock timing 4/			48.75	250	
Instruction cycle time time = Icyc	4	$V_{CC} = V_{CC}$ min			97.5	500	
Delay from RESET assertion to address high impedance	9	See figure 4, reset timing $V_{CC} = V_{CC}$ min	9,10,11			50	ns
Minimum stabalization	10a	See figure 4, reset timing $V_{CC} = V_{CC}$ min 5/			15E4T		
	10b	See figure 4, reset timing $V_{CC} = V_{CC}$ min 6/			50T		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Delay from asynchronous RESET deassertion to first external address output (internal RESET negation)	11	See figure 4, reset and synchronous reset timing $V_{CC} = V_{CC}$ min	9,10,11	All	16T	18T+ 40	ns
Synchronous RESET setup time from RESET deassertion to falling edge of external clock	12 7/	See figure 4, synchronous reset timing $V_{CC} = V_{CC}$ min			20	2T -10	
Synchronous RESET delay time from the sync. falling edge of ext. clock to the first external address output	13			01	16T+8	16T+ 30	
				02	16T+5 7/	16T+ 30	
Mode select setup time	14	See figure 4, operating mode select timing $V_{CC} = V_{CC}$ min		All	100		
Mode select hold time	15				0		
Minimum edge-triggered interrupt request width	16	$V_{CC} = V_{CC}$ min See figure 4, external interrupt timing Assertion: De-assertion:		01	48		
				02	25 15		
Delay from IRQA,IRQB assertion to external memory access address output valid caused by first interrupt instruction fetch	17	See figure 4, external level sensitive fast interrupt timing $V_{CC} = V_{CC}$ min 8/ Fetch: Ex:		01	19T		
				02	11T 19T		
Delay from IRQA, IRQB to assertion to gen.-purpose transfer output valid caused by first interrupt instruction execution.	18	$V_{CC} = V_{CC}$ min	9,10,11	All	23T		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Delay from address output valid caused by first interrupt instruction fetch to interrupt request deaasertion for level sensitive fast interrupts	19	See figure 4, external level sensitive fast interrupt timing $V_{CC} = V_{CC}$ min 8/	9,10,11	All		5T+2T *WS-44	ns
Delay from RD assertion to interrupt request deassertion for level sensitive fast interrupts	20					4T+2T *WS-40	
Delay from WR assertion to interrupt request deassertion for level sensitive fast interrupts WS = 0	21a					4T -40	
Delay from WR assertion to interrupt request deassertion for level sensitive fast interrupts WS > 0	21b					3T+2T *WS-40	
Delay from general purpose output valid to interrupt request deassertion for level sensitive fast interrupts, If second interrupt instruction is single cycle	22a					T-60	
Delay from general purpose output valid to interrupt request deassertion for level sensitive fast interrupts, if second interrupt instruction is two cycles	22b					5T -60	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Synchronous interrupt set-up time from IRQA, IRQB assertion to the synchronous rising edge of external clock	23	See figure 4, synchronous interrupt from wait state timing	9,10,11	All	25	2T-10	ns
Synchronous interrupt delay time from the synchronous rising edge of the external clock to the first external address output valid caused by the first instruction fetch after coming out of wait state	24	$V_{CC} = V_{CC}$ min		01	19T+8	19T+30	
				02	27T+8 7/	27T+30	
Duration for IRQA assertion to recover from STOP state	25	$V_{CC} = V_{CC}$ min, See figure 4, recovery from stop state using IRQA		01	19T+8	19T+30	
				02	25		
Delay from IRQA assertion to fetch of first interrupt instruction	26a	$V_{CC} = V_{CC}$ min, OMR bit 6 = 0 Stable external clock see figure 4, recovery from stop state using IRQA		01	128000T +17T		
				02	131090T		
Delay from IRQA assertion to fetch of first interrupt instruction	26b	$V_{CC} = V_{CC}$ min, OMR bit 6 = 1 Internal crystal oscillator clock, see figure 4, recovery from stop state using IRQA		01	150000T		
				02	34T		
Duration of level sensitive IRQA assertion to fetch of first interrupt instruction	27a	$V_{CC} = V_{CC}$ min, OMR bit 6 = 0 External clock see figure 4, recovery from stop state and using IRQA interrupt service		01	128000T +17T		
				02	131067T		
Duration of level sensitive IRQA assertion to fetch of first interrupt instruction	27b	$V_{CC} = V_{CC}$ min, OMR bit 6 = 1 Internal clock see figure 4, recovery from stop state and using IRQA interrupt service		01	150000T		
				02	11T		
Delay from level sensitive IRQA assertion to fetch of first interrupt instruction	28a	$V_{CC} = V_{CC}$ min, OMR bit 6 = 0 External clock see figure 4, recovery from stop state and using IRQA interrupt service		01	128000T +17T		
				02	131090T		
Delay from level sensitive IRQA assertion to fetch of first interrupt instruction	28b	$V_{CC} = V_{CC}$ min, OMR bit 6 = 1 Internal clock see figure 4, recovery from stop state and using IRQA interrupt service		01	150000T		
				02	34T		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Min	Max	Unit
Host synchronization delay 9/	30	V_{CC} = V_{CC} min See figure 4, host synchronous delay	9,10,11	All	T	3T	ns
HEN/HACK assertion width (CVR, ICR, ISR Read)	31	V_{CC} = V_{CC} min See figure 4, host read and write cycles		02	2T+60		
HEN/HACK assertion width (read)	31a			All	50		
HEN/HACK assertion width (write)	31b			All	25		
HEN/HACK deassertion width	32			All	25		
Min cycle between two HEN	32a			02	4T+60		
Host data input setup time before HEN/HACK deassertion	33	V_{CC} = V_{CC} min See figure 4, host write cycle and host DMA write cycle		All	5		
Host data input hold time after HEN/HACK deassertion	34				5		
HEN/HACK assertion to output data active from high impedance	35	See figure 4, host interrupt vector register (IVR) read, host read cycle and write cycle			0		
HEN/HACK assertion to output data valid	36	V_{CC} = V_{CC} min				50	
HEN/HACK deassertion to output data high impedance	37					35	
Output data hold time after HEN/HACK deassertion	38				5		
HR/W low setup time before HEN assertion	39	See figure 4, host write cycle			0		
HR/W low hold time after HEN deassertion	40	V_{CC} = V_{CC} min			5		
HR/W high setup time to HEN assertion	41	V_{CC} = V_{CC} min See figure 4, host IVR read and host read cycle			0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
HR/W high hold time after HEN/HACK deassertion	42	$V_{CC} = V_{CC}$ min See figure 4, host IVR read and host read cycle	9,10,11	All	5		ns
HA0-HA2 setup time before HEN assertion	43	$V_{CC} = V_{CC}$ min See figure 4, host read cycle and write cycle	9,10	01	0		
			11		2		
HA0-HA2 setup time before HEN assertion	43		9,10,11	02	1		
HA0-HA2 hold time after HEN deassertion	44		9,10,11		5		
DMA HACK assertion to HREQ deassrtion	45	$V_{CC} = V_{CC}$ min See figure 4, host DMA read and write cycles HREQ is pulled up by a 1 kΩ resistor		01	5	30	
				02	5 7/	60	
DMA HACK deassertion to HREQ assertion (for DMA RXL read)	46a			All	tHSDL +3T+5		
DMA HACK deassertion to HREQ assertion (for DMA TXL write)	46b				tHSDL +2T+5		
DMA HACK deassertion to HREQ assertion (for all other cases)	46c				5		
Delay from HEN deassertion HREQ assertion for RXL read	47				tHSDL +3T+5		
Delay from HEN deassertion to HREQ assertion for TXL write	48				tHSDL +2T+5		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Delay from HEN assertion to HREQ deassertion for RXL read, (TXL write)	49	V_{CC} = V_{CC} min See figure 4, host read/ write cycles HREQ is pulled up by a 1 kΩ resistor	9,10,11	All	5	75	ns
Synchronous clock cycle 10/	55	V_{CC} = V_{CC} min See figure 4, SCI synchronous mode timing			16T		
Clock low period	56				16T/2 -20		
Clock high period	57			01	16T/2 -10		
				02	16T/2 -20		
Output clock rise/fall time	58			01		20	
Output data setup to clock falling edge (internal clock)	59			All	16T/4 +T-50		
Output data hold after clock rising edge (internal clock)	60				16T/4 -T-15		
Input data setup time before clock rising edge (internal clock)	61				16T/4 +T+45		
Input data not valid before clock rising edge (internal clock)	62			01		16T/4 -10	
				02		16T/4 +T-10	
Clock falling edge to output data valid (external clock)	63			All		63	
Output data hold after clock rising edge (external clock)	64				2T+12		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Min	Max	Unit
Input data setup time before clock rising edge (external clock)	65	$V_{CC} = V_{CC}$ min See figure 4, SCI synchronous mode timing	9,10,11	All	30		ns
Input data hold time after clock rising edge (external clock)	66				40		
Asynchronous clock cycle 11/	67	See figure 4, SCI asynchronous mode timing $V_{CC} = V_{CC}$ min		01	128T/2-20		
				02	128T		
Clock low period 7/	68			All	128T/2-20		
Clock high period 7/	69				128T/2-20		
Output clock rise/fall time	70			01		20	
Output data setup to clock rising edge (internal clock)	71			All	128T/2-100		
Output data hold after clock rising edge (internal clock)	72				128T/2-100		
Clock cycle 12/	80	See figure 4, SSI receiver and transceiver timing			8T		
Clock high period	81				8T/2-20		
Clock low period	82	$V_{CC} = V_{CC}$ min			8T/2-20		
Output clock rise/fall time	83			01		20	
RXC rising edge to FSR out (bl) high. external clock.	84a	See figure 4, SSI receiver timing 13/ $V_{CC} = V_{CC}$ min		All		80	
RXC rising edge to FSR out (bl) high. internal clock, asynchronous mode	84b					50	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
RXC rising edge to FSR out (bl) low. external clock	85a	$V_{CC} = V_{CC}$ min See figure 4, SSI receiver timing	9,10,11	01		80	ns
				02		70	
RXC rising edge to FSR out (bl) low. internal clock asynchronous mode	85b			All		40	
RXC rising edge to FSR out (wl) high. external clock.	86a			01		80	
				02		70	
RXC rising edge to FSR out (wl) high. internal clock, asynchronous mode	86b			All		40	
RXC rising edge to FSR out (wl) low. external clock.	87a			01		80	
				02		70	
RXC rising edge to FSR out (wl) low. internal clock, asynchronous mode.	87b			All		40	
Data in setup time before RXC (SCK in synchronous mode) falling edge. external clock.	88a				15		
Data in setup time before RXC (SCK in synchronous mode) falling edge. internal clock, asynchronous mode	88b				35		
Data in setup time before RXC (SCK in synchronous mode) falling edge. internal clock, synchronous mode.	88c				25		
Data in hold time after RXC falling edge external clock	89a			01	33		
				02	35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Data in hold time after RXC falling edge internal clock	89b	$V_{CC} = V_{CC}$ min See figure 4, SSI receiver timing	9,10,11	All	5		ns
FSR input (bl) high before RXC falling edge external clock. 13/	90a				15		
FSR input (bl) high before RXC falling edge internal clock, asynchronous mode. 13/	90b				35		
FSR input (wl) high before RXC falling edge external clock 13/	91a			01	15		
				02	20		
FSR input (wl) high before RXC falling edge internal clock, asynchronous mode. 13/	91b			All	55		
FSR input hold time after RXC falling edge external clock	92a			01	33		
				02	35		
FSR input hold time after RXC falling edge internal clock	92b			All	5		
Flags input setup before RXC falling edge external clock	93a			01	24		
				02	30		
Flags input setup before RXC falling edge internal clock, synchronous mode	93b			All	50		
Flags input hold time after RXC falling edge external clock	94a			01	24		
				02	35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Flags input hold time after RXC falling edge internal clock, synchronous	94b	$V_{CC} = V_{CC}$ min See figure 4, SSI receiver timing	9,10,11	All	5		ns
TXC input edge to FST out (bl) high, external clk	95a	$V_{CC} = V_{CC}$ min See figure 4, SSI receiver timing		01		80	
				02		70	
TXC input edge to FST out (bl) high, internal clk	95b	13/		All		30	
TXC rising edge to FST out (bl) low, external clk	96a			01		80	
				02		65	
TXC rising edge to FST out (bl) low, internal clk	96b			All		35	
TXC rising edge to FST out (wl) high, external clk	97a			01		80	
				02		65	
TXC rising edge to FST out (wl) high, internal clk	97b			All		35	
TXC rising edge to FST out (wl) low, external clk	98a			01		80	
				02		65	
TXC rising edge to FST out (wl) low, internal clock	98b			All		35	
TXC rising edge to data out enable from high impedance external clock	99a	See figure 4, SSI transmitter timing $V_{CC} = V_{CC}$ min		All		65	
TXC rising edge to data out enable from high impedance internal clock	99b					40	
TXC rising edge to data out valid external clock	100a		9	01		80	
				02		65	
TXC rising edge to data out valid external clock	100a		10	01		85	
				02		65	

See footnotes at end of table.

TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
TXC rising edge to data out valid external clock	100a	See figure 4, SSI transmitter timing	11	01		70	ns
				02		65	
TXC rising edge to data out valid internal clock	100b	$V_{CC} = V_{CC}$ min	9,10,11	All		40	
TXC rising edge to data out high impedance external clock	101a					70	
TXC rising edge to data out high impedance internal clock	101b					40	
TXC falling edge to data out high impedance for gated clock mode only	101c			02	3T		
FST input (bl) setup time before TXC falling edge external clock	102a			All	15		
FST input (bl) setup time before TXC falling edge internal clock 13/	102b				35		
FST input (wl) to data out enable from high impedance 13/	103					60	
FST input (wl) setup time TXC falling edge external clock 13/	104a			01	15		
				02	20		
FST input (wl) setup time TXC falling edge internal clock 13/	104b			All	55		
FST input hold time after TXC falling edge external clock	105a				35		
FST input hold time after TXC falling edge internal clock	105b				5		

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Group A subgroups	Device	Min	Max	Unit
Flag out valid after TXC rising edge external clock	106a	See figure 4, SSI transmitter timing $V_{CC} = V_{CC}$ min	9,10,11	All		70	ns
Flag out valid after TXC rising edge internal clock	106b					40	
Delay from BR assertion to BG assertion 14/	115a	See figure 4, bus request-bus grant timing $V_{CC} = V_{CC}$ min		01	3T	9T+20	
				02	5T	9T+20	
Delay from BR assertion to BG assertion 15/	115b			All	3T	9T+2T*WS+20	
Delay from BR assertion to BG assertion 16/	115c				3T	13T+4T*WS+20	
Delay from BR assertion to BG assertion 17/	115d			All	∞		
Delay from BR assertion to BG assertion 18/	115e			01	∞		
				02	T+4	3T+30	
Delay from BR deassertion to BG deassertion	116			01	5T	9T+20	
				02	4T	8T+20	
BG deassertin duration	117			All	4T-10		
Delay from address, data, and control bus high impedance to BG assertion	118				0		
Delay from BG deassertion to address, data, and control bus enabled	119			01		-10	
				02		T-15	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Address valid to WR assertion. WS=0	120a	See figure 4, external bus timing $V_{CC} = V_{CC}$ min	9,10,11	01	T-9	T	ns
				02	T-9	T+5	
Address valid to WR assertion. WS>0	120b			01	2T-9	2T	
				02	2T-9	2T+5	
WR assertion width. WS=0	121a			All	2T-9		
WR assertion width. WS>0	121b				(2*WS +1)*T -9		
WR deassertion to address not valid	122				T-12		
WR assertion to data out valid. WS=0	123a				T-9	T+10	
WR assertion to data out valid. WS>0	123b				0	10	
Data out hold time from WR deassertion	124				T-9	T+7	
Data out setup time to WR deassertion. WS=0	125a			01	T-4		
				02	T-5		
Data out setup time to WR deassertion. WS>0	125b			01	(2*WS+ 1)*T-9		
				02	2T*WS +T-5		
RD deassertion to address not valid	126			All	T-9		
Address valid to RD deassertion. WS=0	127a				3T-8		
Address valid to RD deassertion. WS>0	127b				(2*WS +3)*T -8		
Input data hold time to RD deassertion	128				0		
RD assertion width. WS=0	129a				2T-9		
RD assertion width. WS>0	129b				(2*WS +2)*T -9		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Limits Min	Limits Max	Unit
Address valid to input data valid. WS=0	130a	See figure 4, external bus timing $V_{CC} = V_{CC}$ min	9,10,11	All		3T-18	ns
Address valid to input data valid. WS>0	130b					(2*WS +3)*T -18	
Address valid RD assertion	131			01	T-9	T	
				02	T-9 7/	T+5	
RD assertion to input data valid. WS=0	132a			All		2T-14	
RD assertion to input data valid. WS>0	132b					(2*WS +2)*T -14	
WR deassertion to RD assertion	133				2T-15		
RD deassertion to RD assertion	134				2T-10		
WR deassertion to WR assertion. WS=0	135a				2T-15		
WR deassertion to WR assertion. WS>0	135b				3T-15		
RD deassertion to WR assertion. WS=0	136a				2T-10		
RD deassertion to WR assertion. WS>0	136b				3T-10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Min	Max	Unit
CLK low Transition to address valid	140	V_{CC} = V_{CC} min See figure 4	9,10,11	02		24	ns
CLK high transition to WR*	141						
WS = 0					0	19	
WS > 0					0	T+19	
CLK high transition to WR* Deassertion	142				5	21	
CLK high transition RD* assertion	143				0	19	
CLK high transition to RD* deassertion	144				3	17	
CLK low transition to data-out-valid	145				-	25	
CLK low transition to data-out-invalid	146				5	-	
Data-In Valid to CLK high transition (Setup)	147				0	-	
CLK high transition to data-invalid (Hold)	148				15	-	
CLK Low to address invalid	149				3		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device	Min	Max	Unit
CLK low transition to BS* assertion	150	V_{CC} = V_{CC} min See figure 4	9,10,11	02	4	24	ns
WT* assertion to clk low transition (setup time)	151				4	-	
Clk low transition to WT* deassertion for minimum timing	152				14	2T-8	
WT* deassertion to clk low transition for max timing 2WS	153				8	-	
CLK high transition to BS* deassertion	154				5	26	
BS* assertion to address valid	155				-2	10 7/	
BS* assertion to WT* assertion	156				0	2T-15	
BS* assertion to WT* deassertion WS ≤ 2 WS ≥ 2	157				2T(WS -1)2T	4T-15 2T*WS -15	
WT* deassertion to BS* deassertion	158	V_{CC} = V_{CC} min See figure 4			3T	5T+23	
Min. BS* deassertion width consecutive external access	159				T-7	-	
BS* deassertion to address invalid	160				T-10	-	
Data-in valid to RD deassertion (setup)	161				16	-	

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

NOTES:

<u>1/</u>   The following pins are active low: RESET, IRQA, IRQB, RD, WR, HEN, HACK, W (of HR/W), HREQ, BG, BR, PS, DS, Y (of X/Y). For ac testing, the following conditions apply: V_{ILR} maximum = 0.5 V, V_{ILM} maximum = 1.0 V and V_{ILM} minimum = -0.5 V, unless otherwise specified.

<u>2/</u>   In order to obtain these results all inputs must be terminated, i.e., not allowed to float.

<u>3/</u>   External clock input high and clock input low are measured at 50% of the input transition.

<u>4/</u> $T = I_{CYC}/4$ is used in the electrical characteristics. The exact length of each T is affected by the duty cycle of the external clock input.

<u>5/</u>   A clock stabilization delay is required when using the on-chip crystal oscillator after power-on reset and after recovering from STOP mode.

<u>6/</u>   Circuit stabilization delay is required during reset when using an external clock after power-on reset and after recovering from STOP mode.

<u>7/</u>   Parameters are guaranteed but not tested.

<u>8/</u>   Timing parameters 17 through 22 apply only to IRQA and IRQB in level-sensitive mode using fast interrupts to prevent multiple interrupt service. To avoid these timing restrictions, the negative edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using level sensitive mode.

<u>9/</u>   Host synchronization delay, (t_{HSDL}), is the time period required for the device to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the internal clock.

<u>10/</u> Synchronous clock cycle, t_{SCC}, (for internal clock) is determined by the SCI clock control register and I_{CYC}.

<u>11/</u> Asynchronous clock cycle, t_{ACC}, (for internal clock) is determined by the SCI clock control register and I_{CYC}.

<u>12/</u> For internal clock, external clock cycle is defined by Icyc and SSI control register.

<u>13/</u> The timing waveforms in the ac electrical characteristics are tested with V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, RESET, MODA, and MODB. These four pins are tested using the input levels set forth in the dc electrical characteristics, except for V_{ILR} and V_{ILM}, which are referenced to a device input signal and are measured with respect to the 50% point of the respective input signal's transition. The device 01 output levels are measured with V_{OL} and V_{OH} reference levels set at 1.0 V dc and 2.0 V dc, respectively. WS= Number of wait states (1 WS = 1 tcyc) programmed into the external bus access using BCR (WS=0-15). t_{HSDL} = Host synchronization delay time. TXC (SCK pin) = Transmit clock. RXC (SCO and SCK pin) = Receive clock. FST (SC2 pin) = Transmit frame sync. FSR (SC1 or SC2 pin) = Receive frame sync.
bl = Bit length. wl = Word length. Device external bus timing parameters are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance.

<u>14/</u> With no external access from DSP.

<u>15/</u> During external read or write access.

<u>16/</u> During external read-write-modify access.

<u>17/</u> During STOP mode, external bus will not be released and BG will not go low.

<u>18/</u> During WAIT mode, external bus will not be released and BG will not go low.

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Case Y

INDEX AND PIN NO 1 ID AREA
SEE NOTES 1 AND 4

FIGURE 1. Case outline.

Case Y

SECTION A-A

SECTION A-A

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.18
A1	.018	.035	0.46	0.89
b	.008	.014	0.20	0.36
c	.005	.010	0.13	0.25
D/E	.940	.960	23.88	24.38
e	.025 BSC		1.27 BSC	
e1	.600 BSC		15.24 BSC	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.61	1.02
N	100			
R	.011	.034	0.28	0.86
R1	.009		0.23	

NOTES:
1/. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2/. Generic lead attach dogleg depiction.
3/. Dimension N: Number of terminals.
4/. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5/. Metric equivalents are given for general information only.
6/. Controlling dimensions are in inches.
7/. Datums X and Y to be determined where center leads exit the body.
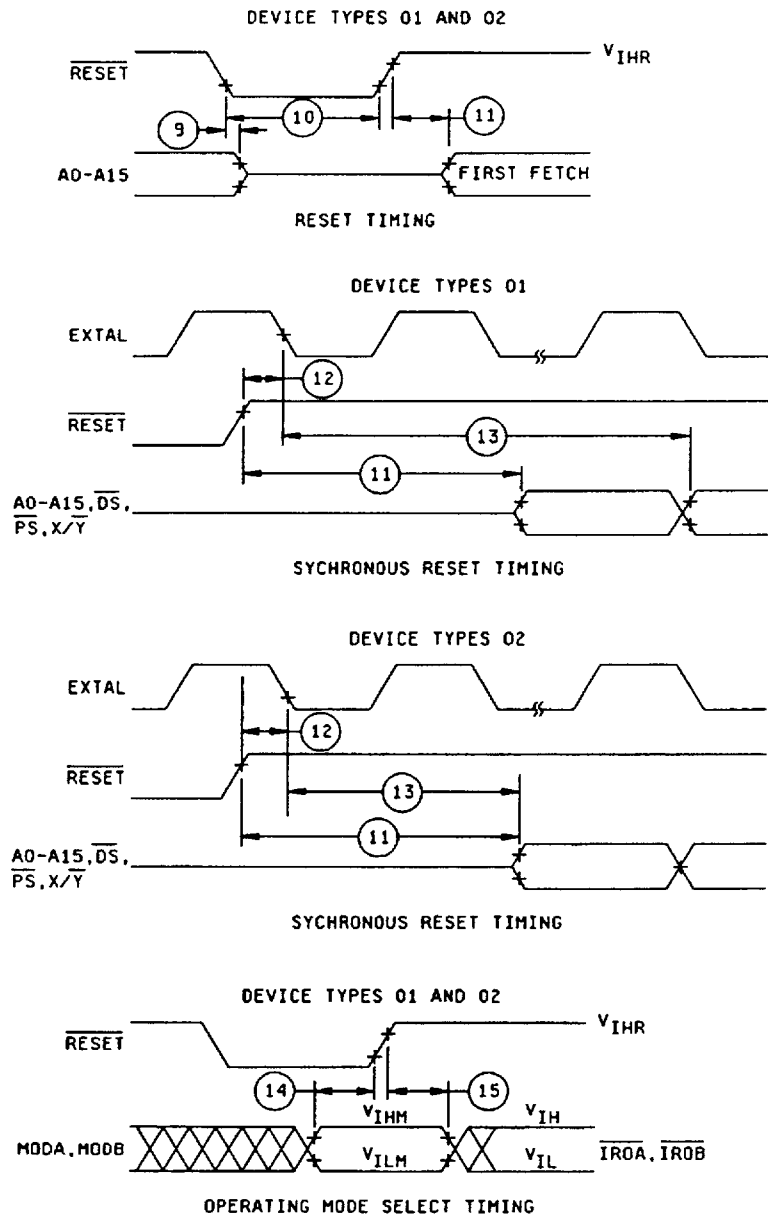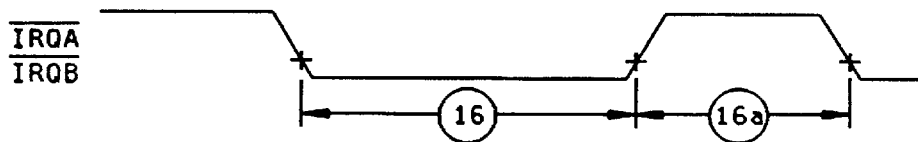8/. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

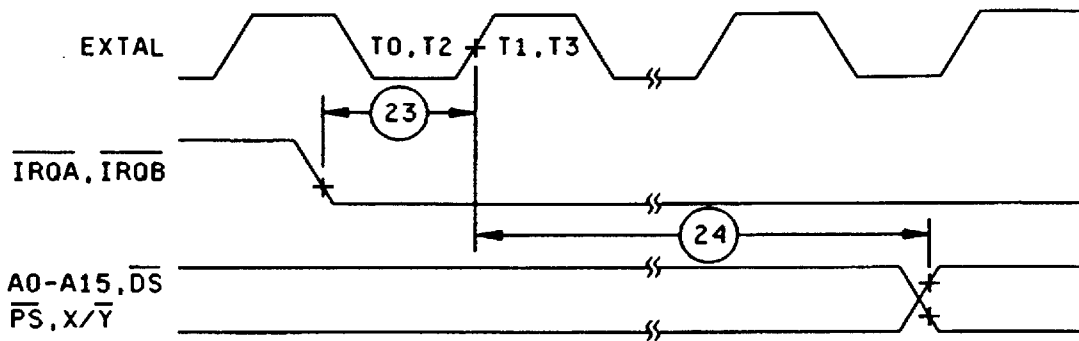| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89512
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Device type 01, 02

FIGURE 2. Terminal connections.

	1	2	3	4	5	6	7	8	9	10	11	12	13
N	D0	A14	A13	A12	A10	A8	A7	A6	A4	A2	A1	$\overline{PS}$	$X/\overline{Y}$
M	D3	D1	A15		A11	A9		A5	A3		A0	$\overline{DS}$	$\overline{WR}$
L	D4	D2			GND		V_{CC}	GND				$\overline{RD}$	$\overline{BR}$
K	D6	D5										$\overline{BG}$	SC1
J	D8	D7	GND									SRD	STD
H	D9												SC2
G	D10		V_{CC}							GND	V_{CC}	SCK	
F	D11	D12										SCO	SCLK
E	D13										GND		TXD
D	D14	D16	GND									HO	RXD
C	D15	D18			V_{CC}			V_{CC}				H2	H1
B	D17	D20		D23	$\overline{IRQA}$	EXTAL	GND	HAO		$\overline{HREQ}$	H7	H4	H3
A	D19	D21	D22	$\overline{IRQB}$	$\overline{RESET}$	XTAL	HA2	HA1	$\overline{HACK}$	$\overline{HEN}$	$HR/\overline{W}$	H6	H5

CASE X
BOTTOM VIEW

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MILITARY DRAWING
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DAYTON, OHIO 45444

SIZE A

5962-89512

REVISION LEVEL C

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DESC FORM 193A
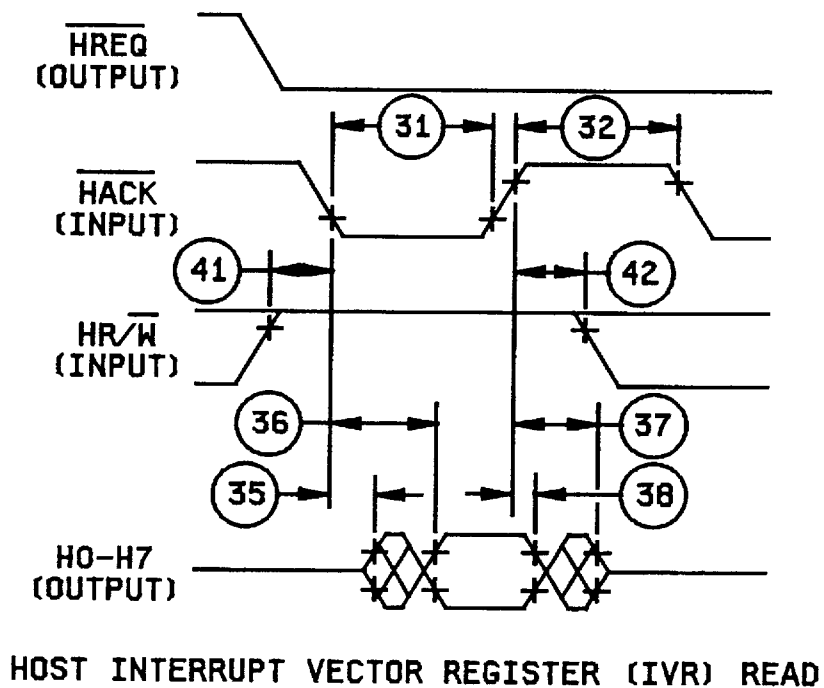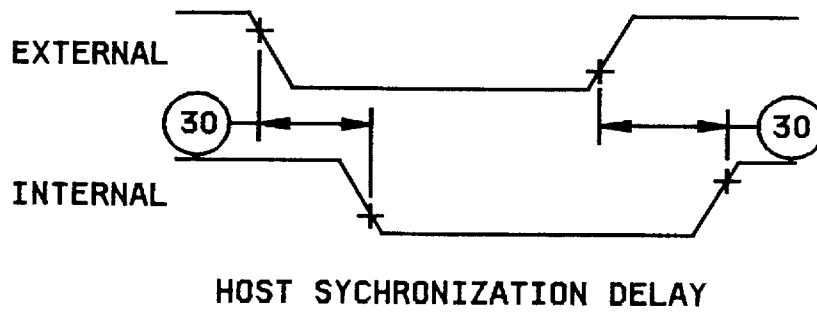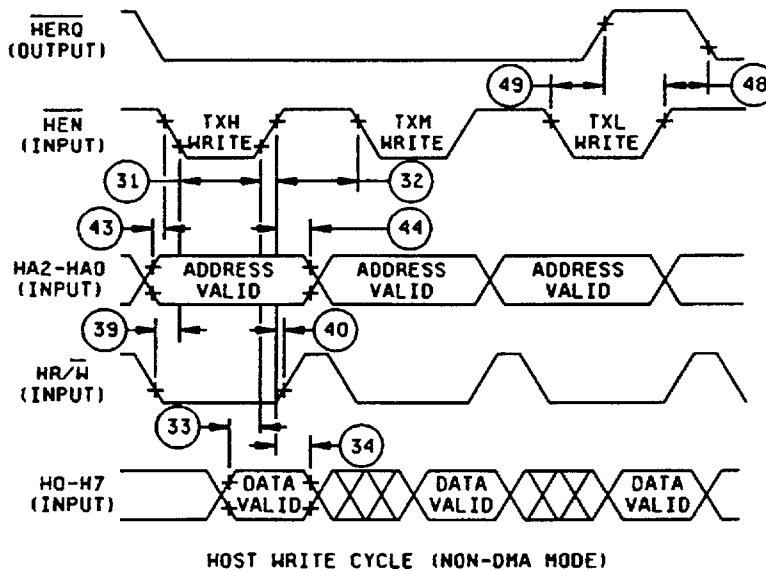JUL 91

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Device type 01, 02

CASE Y

TOP VIEW
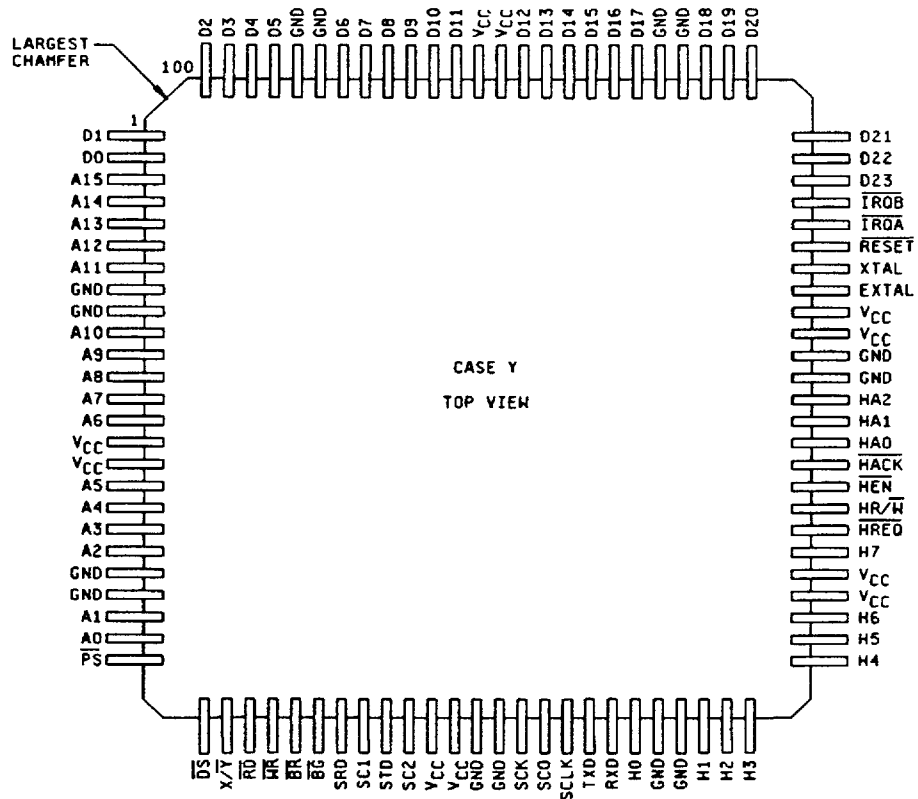
FIGURE 2. Terminal connections. - Continued

FIGURE 3. Block diagram

XTAL   EXTAL

Rf

f_OSC

C   C

Recommended component values		
f_{OSC} (MHz)	C (pF)	Rf (K ohm)
4	82 ±20%	680 ±10%
20	47 ±20%	680 ±10%

Crystal oscillator test circuit

V_{IHC}

EXTAL

V_{ILC}

① ②

③

④

MIDPOINT (SEE NOTE)

EXTERNAL CLOCK TIMING
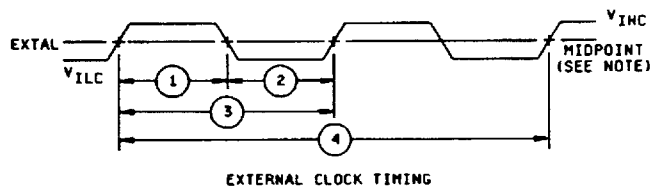
NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} - V_{ILC})$.

External clock timing

FIGURE 4. Switching test circuit and waveforms.

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DEVICE TYPES 01 AND 02

RESET TIMING

DEVICE TYPES 01

SYCHRONOUS RESET TIMING

DEVICE TYPES 02

SYCHRONOUS RESET TIMING

DEVICE TYPES 01 AND 02
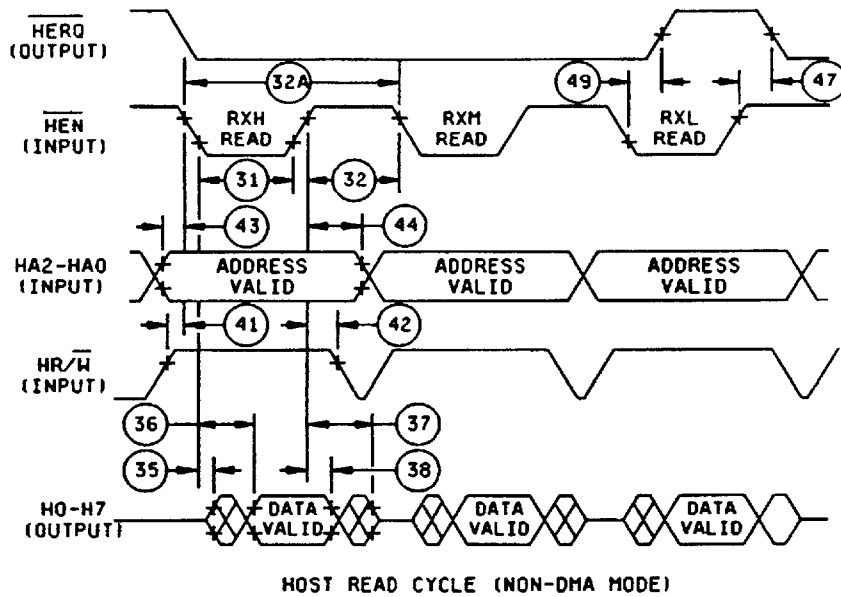
OPERATING MODE SELECT TIMING

FIGURE 4.   Switching test circuit and waveforms - Continued.

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EXTERNAL INTERRUPT TIMING (NEGATIVE EDGE-TRIGGERED)
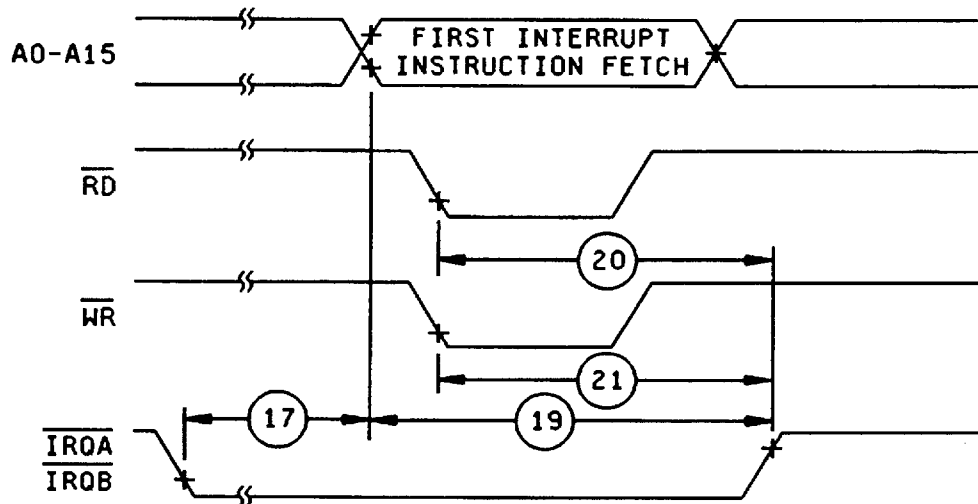
FIRST INTERRUPT INSTRUCTION FETCH
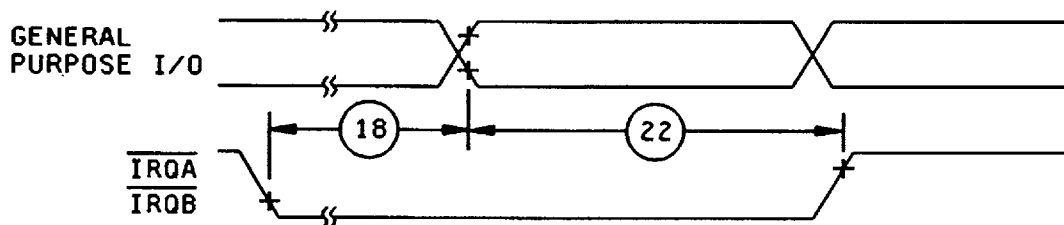
GENERAL PURPOSE I/O
EXTERNAL LEVEL SENSITIVE FAST INTERRUPT TIMING

FIGURE 4.   Switching test circuit and waveforms - Continued.

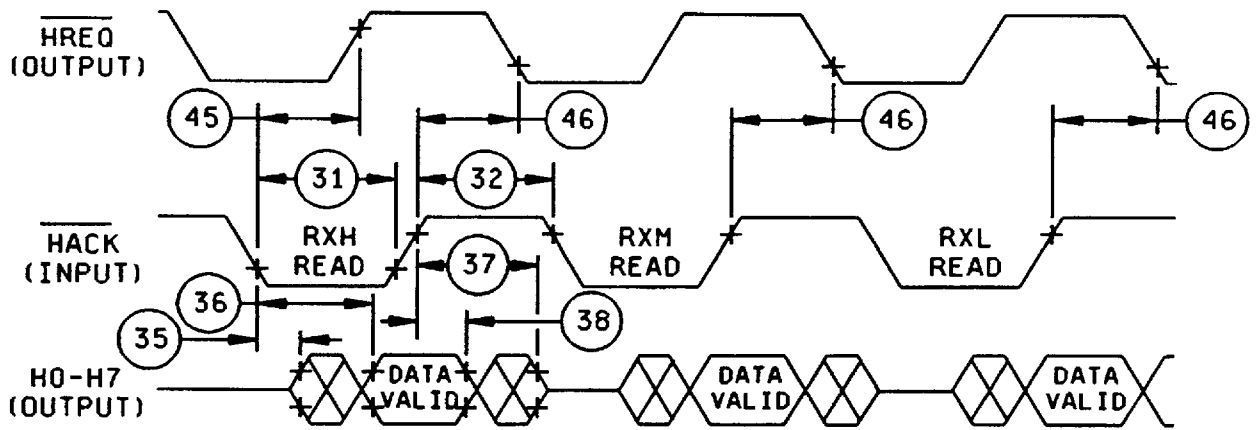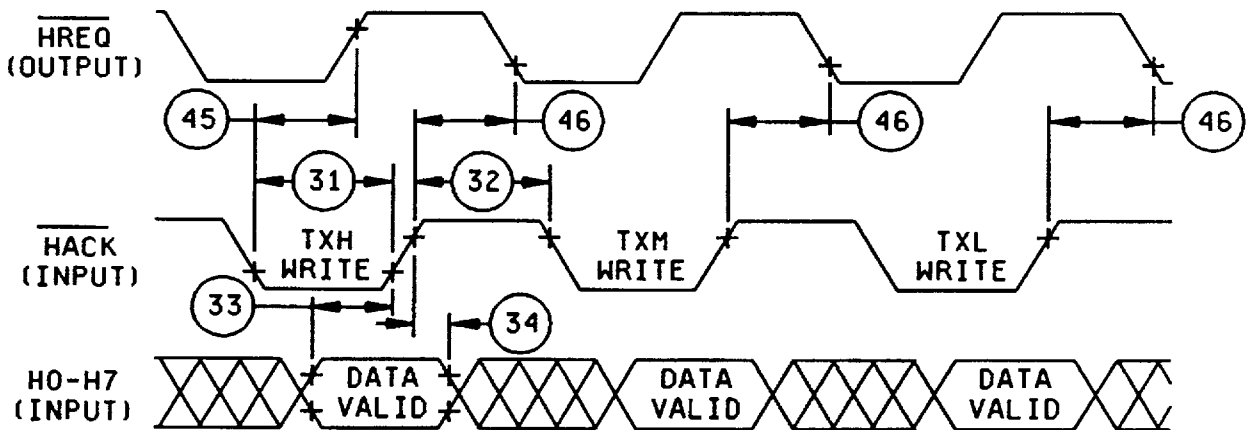| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89512
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SYNCHRONOUS INTERRUPT FROM WAIT STATE TIMING
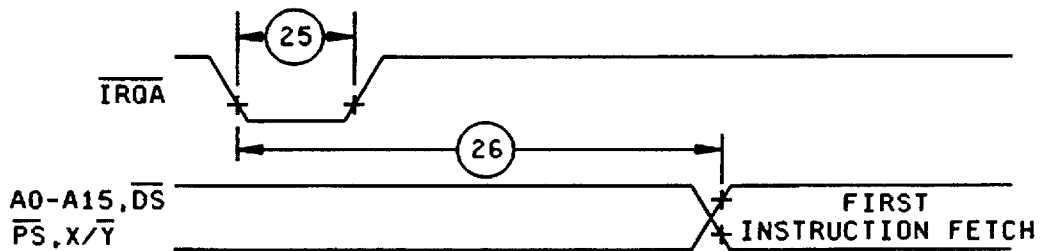
RECOVERY FROM STOP STATE USING $\overline{\text{IRQA}}$
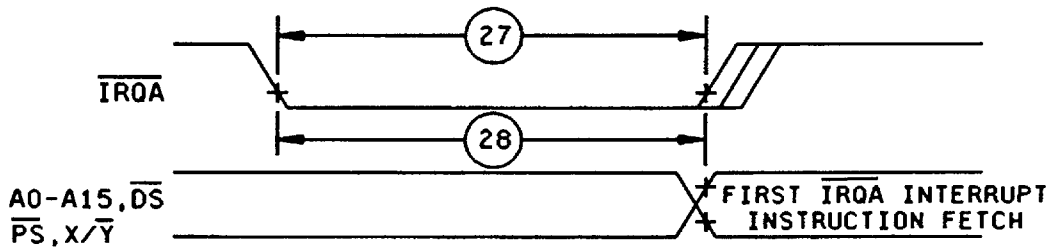
RECOVERY FROM STOP STATE USING $\overline{\text{IRQA}}$ INTERRUPT SERVICE

FIGURE 4. Switching test circuit and waveforms - Continued.

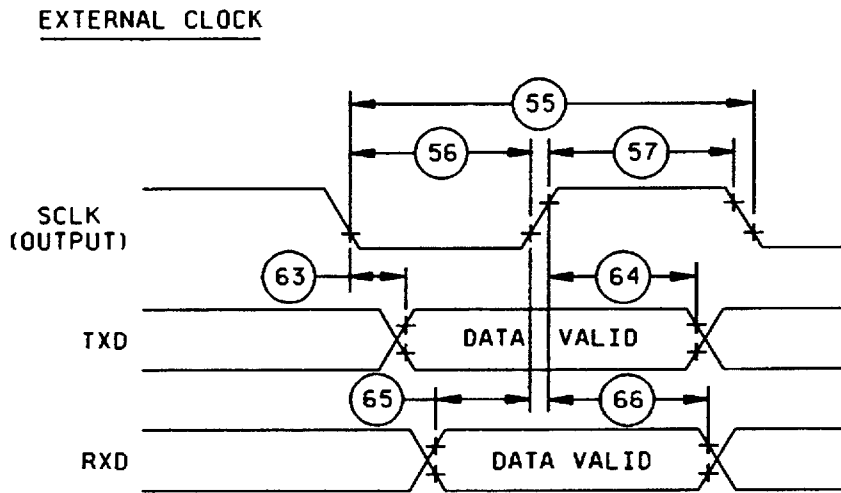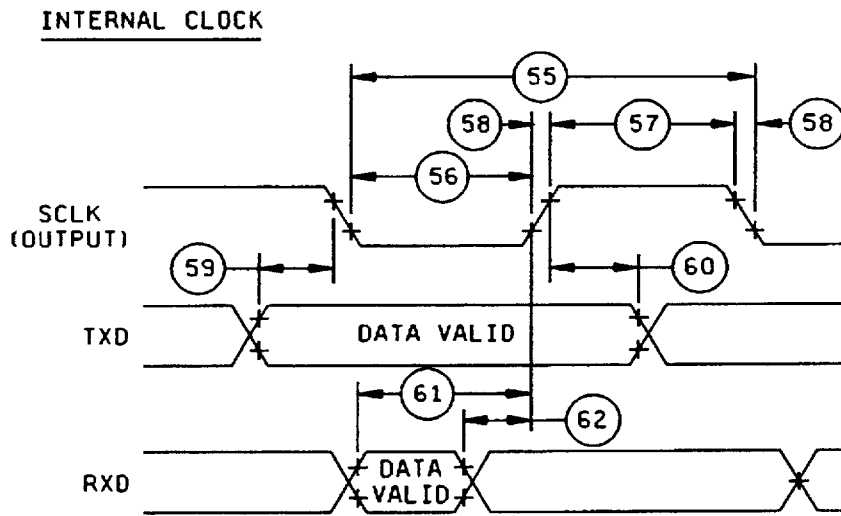| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89512
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EXTERNAL

INTERNAL

(30)   (30)

HOST SYCHRONIZATION DELAY

$\overline{HREQ}$
(OUTPUT)

(31)   (32)

$\overline{HACK}$
(INPUT)

(41)   (42)

HR/$\overline{W}$
(INPUT)

(36)   (37)

(35)   (38)

H0-H7
(OUTPUT)

HOST INTERRUPT VECTOR REGISTER (IVR) READ
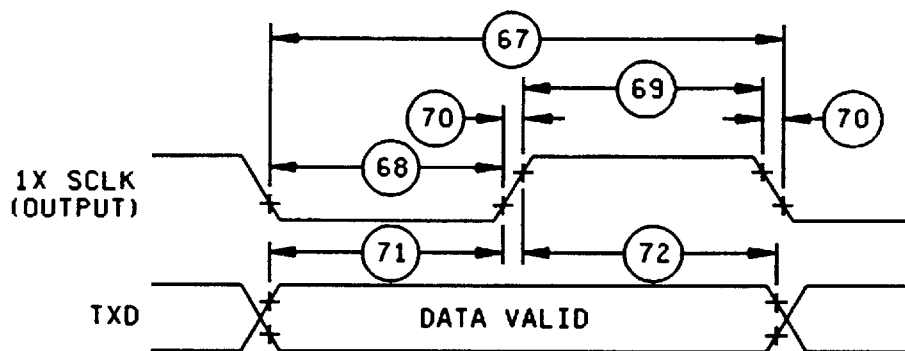
FIGURE 4. Switching test circuit and waveforms - Continued.

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HOST READ CYCLE (NON-DMA MODE)

HOST WRITE CYCLE (NON-DMA MODE)

FIGURE 4. Switching test circuit and waveforms - Continued.

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HOST DMA READ CYCLE

HOST DMA WRITE CYCLE

FIGURE 4. Switching test circuit and waveforms - Continued.

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INTERNAL CLOCK

SCLK
(OUTPUT)

TXD   DATA VALID

RXD   DATA
           VALID

EXTERNAL CLOCK

SCLK
(OUTPUT)

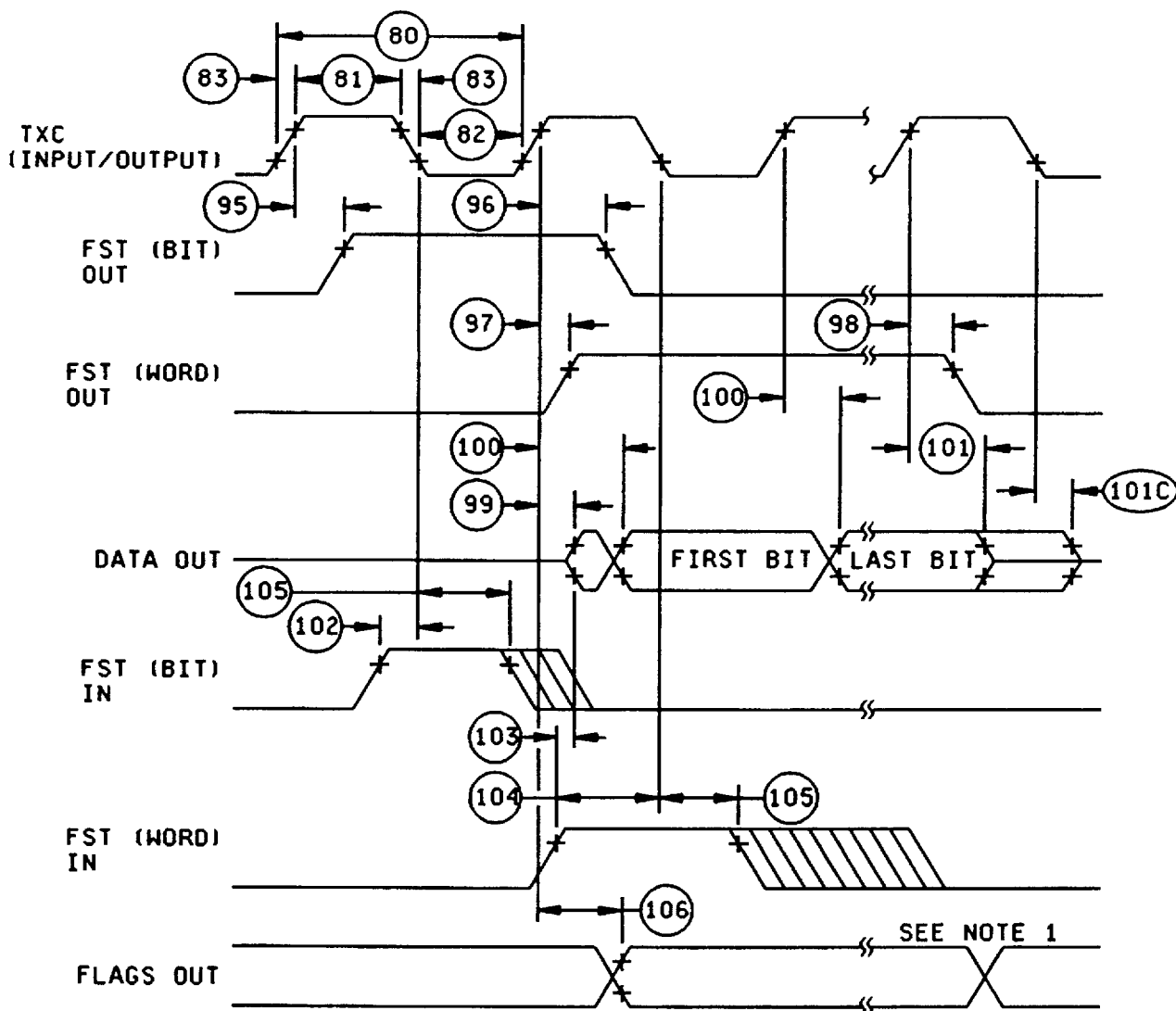TXD   DATA VALID

RXD   DATA VALID

SCI SYNCHRONOUS MODE TIMING

FIGURE 4. Switching test circuit and waveforms - Continued.

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SCI ASYCHRONOUS MODE TIMING

NOTE: In the wire-OR mode TXD can be pulled up by 1 kΩ.

FIGURE 4. Switching test circuit and waveforms - Continued.

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FIGURE 4. Switching test circuit and waveforms - Continued.

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SSI TRANSMITTER TIMING

NOTE: In the network mode, output flag transitions can occur at the start of each time slot within the frame. In the normal mode, the output flag state is asserted for the entire frame period.

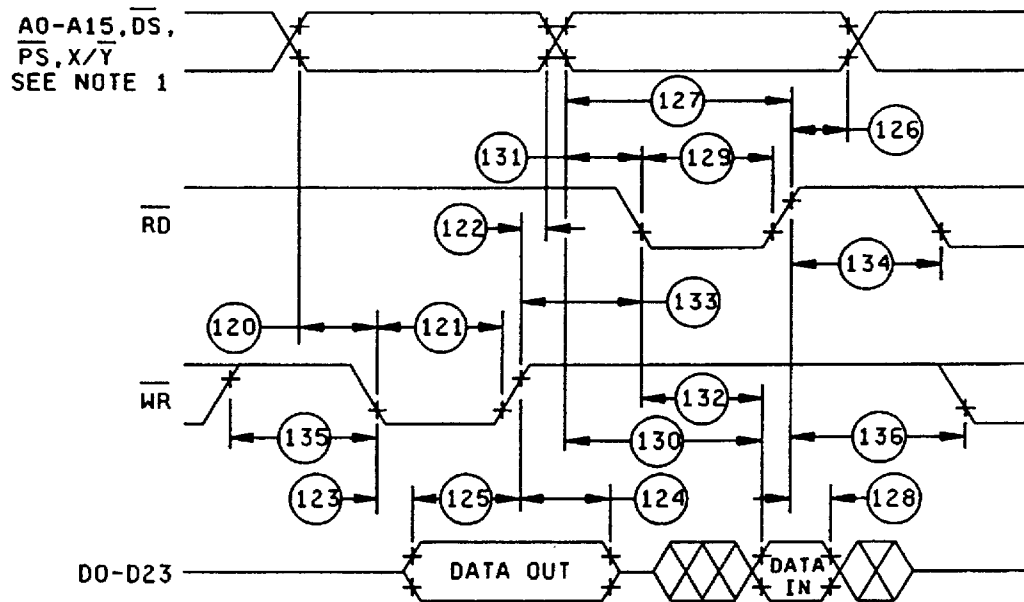FIGURE 4. Switching test circuit and waveforms - Continued.

BUS REQUEST BUS GRANT TIMING

EXTERNAL BUS TIMING

NOTE: During read-modify-write instructions, these address lines do not change state.
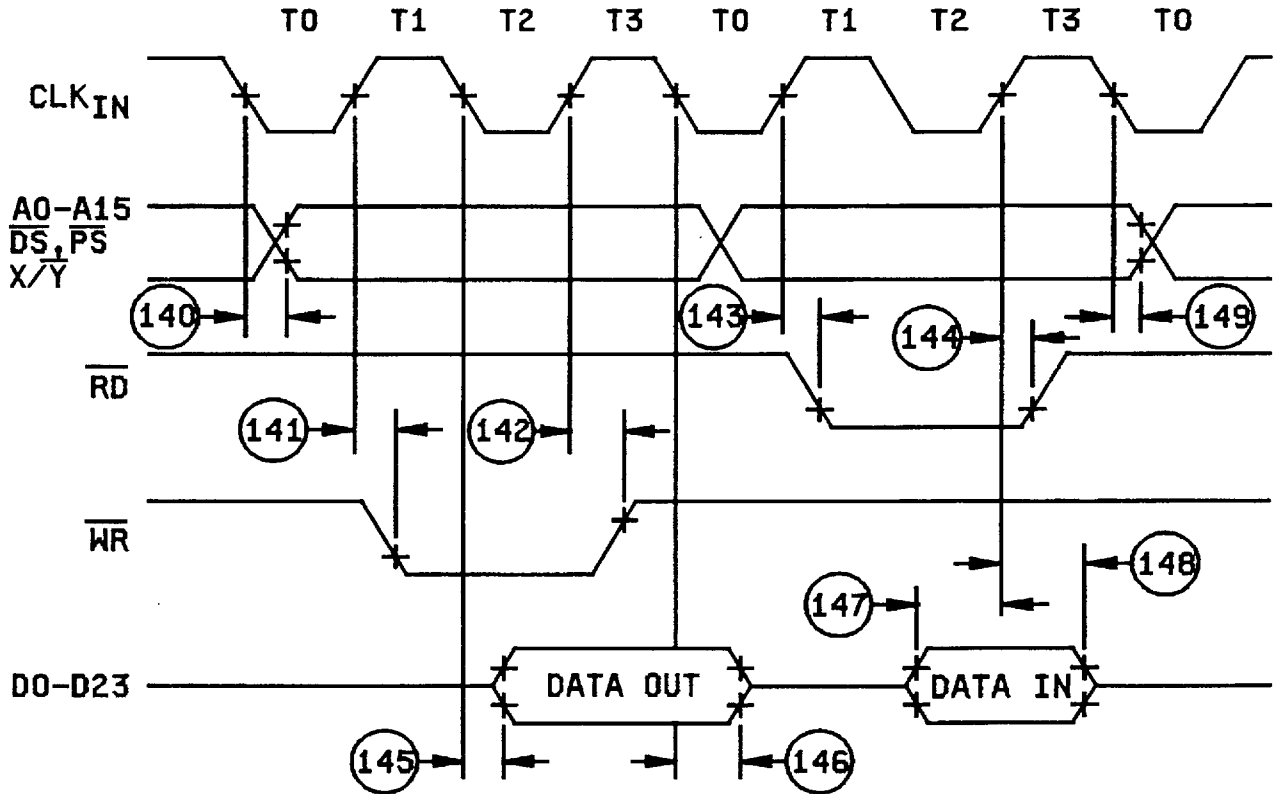
FIGURE 4. Switching test circuit and waveforms - Continued.

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Synchronous bus timing

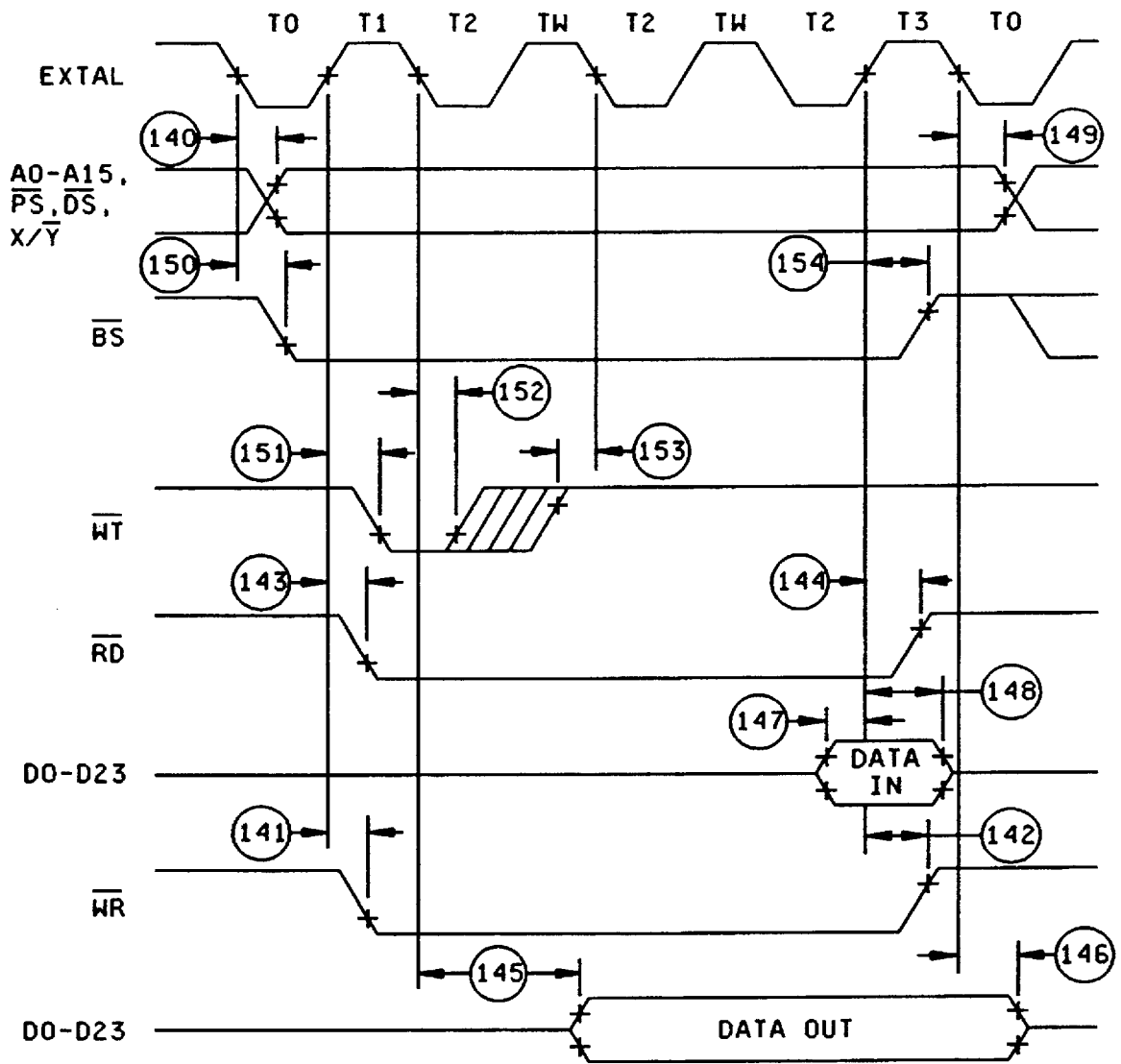Note: During Read-Modify-Write instructions, the address lines do not change states.

FIGURE 4. Switching test circuit and waveforms - Continued.

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Device type 02

Synchronous $\overline{BS}/\overline{WT}$ timings

Note: During Read-Modify-Write instructions, the address lines do not change state. However, BS will deassert before asserting again for the write cycle.

FIGURE 4. Switching test circuit and waveforms - Continued.

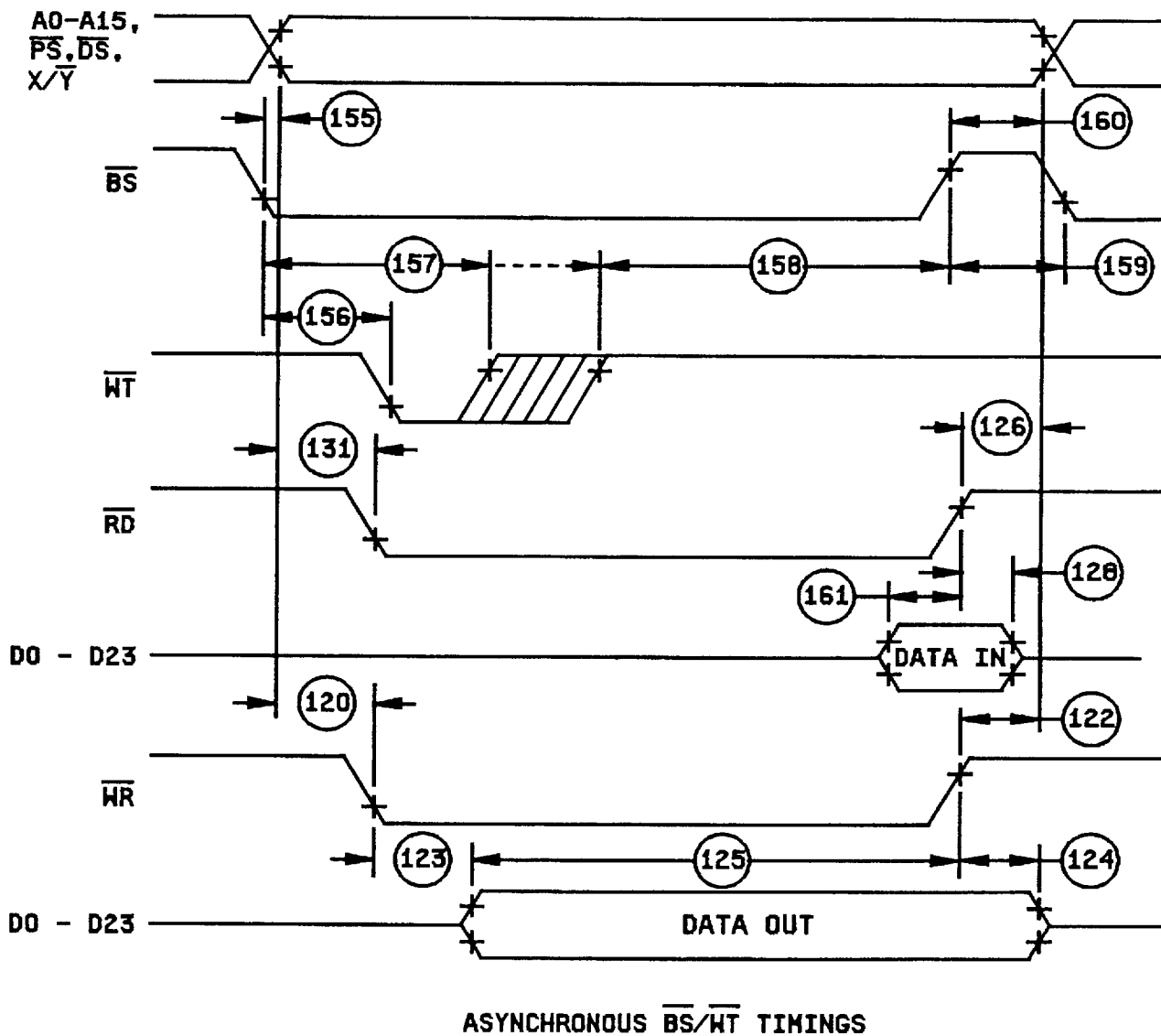| STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89512
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FIGURE 4. Switching test circuit and waveforms - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9
Final electrical test parameters (method 5004)	*1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 functional testing shall include verification of instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

   (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

   (2) T_A = +125°C, minimum.

   (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

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6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 <u>Symbols and definitions</u>. Symbols and definitions are listed as follows:

Pin descriptions	
Pin name	Description
A0 - A15	These three state output pins specify the address for external program and data memory accesses. To minimize power dissipation A0 - A15 do not change state when external memory spaces are not being accessed.
D0 - D23	These pins provide the bidirectional data bus for external program and data memory accesses. D0 - D23 are in the high-impedance state when the bus grant signal is asserted.
$\overline{PS}$	Program memory select is a three state output asserted only when external program memory is referenced.
$\overline{DS}$	Data memory select is a three state output asserted only when external data memory is referenced.
$X/\overline{Y}$	This three state output selects which external data memory space (X or Y) is referenced by data memory select (DS).

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Pin descriptions	
Pin name	Description
$\overline{RD}$	Read enable is a three state output asserted to read external memory on the data bus D0 - D23.
$\overline{WR}$	Write enable is a three state output asserted to write external memory on the data bus D0 - D23.
$\overline{BR}$	The bus request input $\overline{BR}$ allows another device such as a processor or controller to become the master of the data and address buses. When BR is asserted, device 01 will always release the external data bus D0 - D23, address bus A0 - A15 and bus control pins PS, DS, X/Y, RD and WR(i.e., port A), by placing these pins in the high impedance state after the execution of the current instruction has been completed.
$\overline{BG}$	Bus grant is a three state output asserted to acknowledge an external bus request after port A has been released.
MODA/$\overline{IRQA}$ MODB/IRQB	The interrupt and mode control inputs have dual functions: 1) To select the initial chip operating mode. 2) To receive an interrupt request from an external source. MODA and MODB are read and internally latched in the DSP when the processor exits the RESET state. After leaving the RESET state, the MODA and MODB pins automatically change to external interrupt requests IRQA and IRQB. After leaving the RESET state, the chip operating mode can be changed by software. IRQA and IRQB may be programmed to be level sensitive or negative edge triggered. When edge triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal, however, the probability of noise on IRQA or IRQB generating multiple interrupts increases with increasing fall time of the interrupt signal.
$\overline{RESET}$	This Schmitt trigger input pin is used to reset device 01. When RESET is asserted, device 01 is initialized and placed in the reset state. When the RESET signal is negated, the initial ship operating mode is latched from MODA and MODB pins. When coming out of reset, negation occurs at a voltage level and is not directly related to the rise time of the reset signal, however, the probability of noise on RESET generating multiple resets increases with increasing rise time of the reset signal.
V_{CC} G_{ND}	There are five sets of power and ground pins, two pairs for internal logic, one power and two ground for Port A address and control pins, one power and two ground for Port A data pins, and one pair for peripherals.

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Pin descriptions	
Pin name	Description
EXTAL	External clock/crystal input (EXTAL) may be used to interface the crystal oscillator input to an external crystal or an external clock. The maximum clock rate is 20.5 MHz.
XTAL	The crystal output (XTAL) connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL should not be connected.
H0 - H7	The host data bus is used to transfer data between the host processor and device 01. This bus is an input unless enabled by a host processor read. H0 - H7 may be programmed as general purpose parallel I/O pins called PB0 - PB7 when the host interface is not being used.
HA0 - HA2	Host address inputs provide the address selection for each host interface register. HA0 - HA2 may be programmed as general purpose parallel I/O pins called PB0 - PB10 when the host interface is not being used.
HR/$\overline{\text{W}}$	Host read/write input selects the direction of data transfer for each host processor access. HR/W may be programmed as a general purpose I/O pin called PB11 when the host interface is not being used.
$\overline{\text{HEN}}$	Host enable input enables a data transfer on the host data bus When HEN is asserted and HR/W is high, H0 - H7 become outputs and device 01 data may be read by the host processor. When HEN is asserted and HR/W is low, H0 - H7 become inputs and host data is latched inside device 01 when HEN is negated. Normally a chip select signal, derived from host address decoding and an enable clock is used to generate HEN. HEN may be programmed as general purpose I/O pin called PB12 when the host interface is not being used.
$\overline{\text{HREQ}}$	Host request is an open drain output signal used by device 01 interface to request service from the host processor, DMA controller or simple external controller. HREQ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the host interface is not being used.
$\overline{\text{HACK}}$	Host acknowledge input has two functions: 1) To receive a host acknowledge handshake signal for DMA transfers. 2) To receive a host acknowledge compatible with other family processors. HACK may be programmed as a general purpose I/O pin called PB14 when the host interface is not being used.

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Pin descriptions	
Pin name	Description
RXD	Receive data input receives byte oriented serial data into the SCI receive shift register. Input data is sampled on the positive edge of the receive clock. RXD may be programmed as a general purpose I/O pin called PCO when the SCI is not being used.
TXD	Transmit data output transmits serial data from the SCI transmit shift register. Data changes on the negative edge of the transmit clock. This output is stable on the positive edge of the transmit clock. TXD may be programmed as a general purpose I/O pin called PC1 when the SCI is not being used.
SCLK	SCI Serial clock is a bidirectional pin which provides an input or output clock from which the transmit and/or receive baud rate is derived in the asynchronous mode and from which data is transferred in the synchronous mode. SCLK may be programmed as a general purpose I/O pin called PC2 when the SCI is not being used.
SC0	Serial control zero bidirectional pin is used for control by the SSI. SC0 may be programmed as a general purpose I/O pin called PC3 when the SSI is not being used.
SC1	Serial control one bidirectional pin is used for control by the SSI. SC1 may be programmed as a general purpose I/O pin called PC4 when the SSI is not being used.
SC2	Serial control two bidirectional pin is used for control by the SSI. SC2 may be programmed as a general purpose I/O pin called PC5 when the SSI is not being used.
SCK	SSI serial clock bidirectional pin provides the serial bit rate clock for the SSI when only one clock is used. SCK may be programmed as a general purpose I/O pin called PC6 when the SSI is not being used.
SRD	SSI receive data input pin receives data into the SSI receive shift register. SRD may be programmed as a general purpose I/O pin called PC7 when the SSI is not being used.
STD	SSI transmit data output pin transmits serial data from the SSI transmit shift register STD may be programmed as a general purpose I/O pin called PC8 when the SSI is not being used.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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