NEC

NEC Electronics Inc.

μPD27C256
32,768 x 8-BIT
CMOS UV/OTP EPROM

Revision 1 **January 1986**

Description

The μPD27C256 is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory utilizing CMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5 V power supply. All inputs and outputs are TTL-compatible. The μPD27C256 has single location programming, three-state outputs and is pin-compatible with the 27256 EPROM. It is available as a 28-pin DIP.

The μPD27C256 is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

The μPD27C256 has a V_{PP} of 21 V.

Features

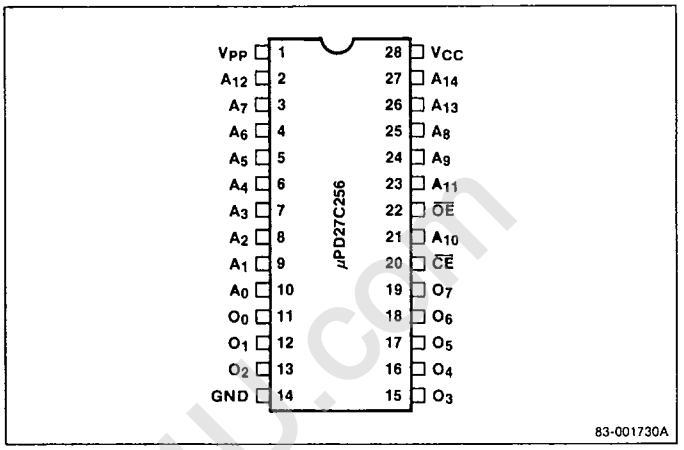
- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation:
  - 165 mW (active)
  - 550 μW (standby)
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5 V power supply
- ☐ JEDEC vendor identification mode
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27256 EPROM
- ☐ CMOS double-polysilicon technology
- ☐ 28-pin DIP

Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C256-15	150 ns	30 mA	100 μA
μPD27C256-20[1]	200 ns	30 mA	100 μA
μPD27C256-25[1]	250 ns	30 mA	100 μA

Note: [1] Available as either UV or OTP. OTP version is *preliminary*.

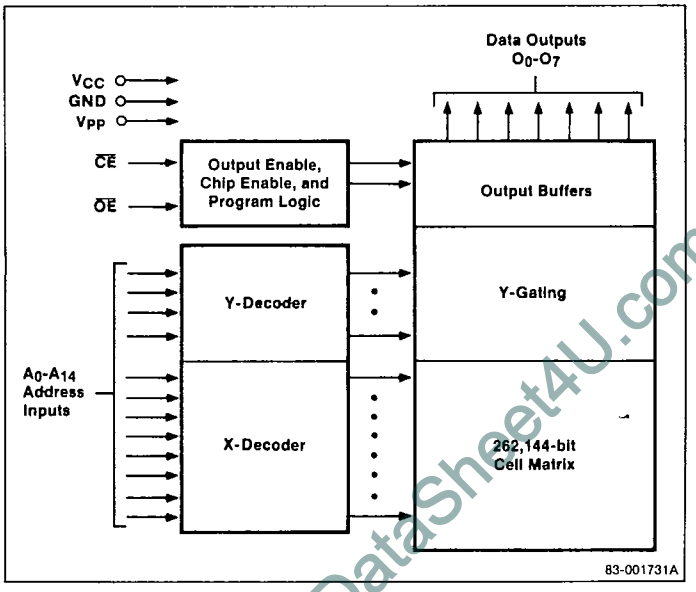
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{PP}	Program voltage
2-10, 21, 23-27	A_0-A_{14}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
28	V_{CC}	+5 V power supply

Block Diagram



μPD27C256

NEC

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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 V to +7.0 V
Input voltage, V_{IN}[1]	−0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	−0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	−10°C to 80°C
Storage temperature, T_{STG}	−65°C to 125°C
Program voltage, V_{PP}	−0.6 V to +22 V
ID read voltage on pin 24, V_{ID}	−0.6 V to +13.5 V

Note: [1] V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz [Note 1]

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			12	pF	V_{OUT} = 0 V

Note: [1] This parameter is sampled and not 100% tested.

DC Characteristics

Read and Standby Modes

T_A = 0°C to +70°C, V_{CC} = +5 V ±10%(1); V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
Standby supply current	I_{SB2}			100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}			100	μA	V_{PP} = V_{CC}

Note: [1] For μPD27C256-15: V_{CC} = 5 V ±5%

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ±5°C, V_{CC} = +6 V ±0.25 V, V_{PP} = +21 V ±0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}

AC Characteristics

Read and Standby Modes

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5\ V \pm 10\%$(3); $V_{PP} = V_{CC}$

Parameter	Symbol	Limits μPD27C256-15 Min	Limits μPD27C256-15 Max	Limits μPD27C256-20[1] Min	Limits μPD27C256-20[1] Max	Limits μPD27C256-25[1] Min	Limits μPD27C256-25[1] Max	Unit	Test Conditions[2]
Address to output delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200		250	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ low to data output delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to data output float delay	t_{DF}		60		60		85	ns	$\overline{CE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes: [1] Available in either UV or OTP.
[2] Output load: see figure 1.
Input rise and fall times: 20 ns.
Input pulse levels: 0.45 V to 2.4 V.
Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.
[3] For μPD27C256-15: $V_{CC} = 5\ V \pm 5\%$

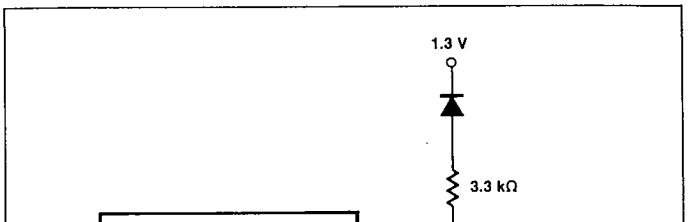
Program, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +6\ V \pm 0.25\ V$, $V_{PP} = +21\ V \pm 0.5\ V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	[Notes 2, 3, 4]
Data setup time	t_{DS}	2			μs	[Notes 2, 3, 4]
Address hold time	t_{AH}	2			μs	[Notes 2, 3, 4]
Data hold time	t_{DH}	2			μs	[Notes 2, 3, 4]
Chip enable to output float delay	t_{DF}			130	ns	[Notes 2, 3, 4]
Supply current setup time	t_{VS}	2			μs	[Notes 2, 3, 4]
Program pulse width	t_{PW}	0.95	1	1.05	ms	[Notes 2, 3, 4]
$\overline{CE}$ setup time	t_{CES}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ setup time	t_{OES}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ hold time[1]	t_{OEH}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ recovery time[1]	t_{OR}	2			μs	[Notes 2, 3, 4]
$\overline{CE}$ to output valid	t_{DV}			1	μs	[Notes 2, 3, 4]

Notes: [1] $t_{OEH} + t_{OR} \geq 50\ \mu s$.
[2] Input pulse levels = 0.45 V to 2.4 V.
[3] Input and output timing reference levels = 0.8 V and 2.0 V.
[4] Input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	Hi-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Note: [1] X can be either V_{IL} or V_{IH}.

Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to +6 V ± 0.25 V; then raise V_{PP} to +21 V ± 0.5 V. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 20 times. If the bit is programmed within 20 tries, apply an additional overprogram pulse of (1 × number of tries) ms and input the next address. If the bit is not programmed in 20 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ± 5% and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C256 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with the $\overline{CE}$ and $\overline{OE}$ at low levels (0).

Erasure

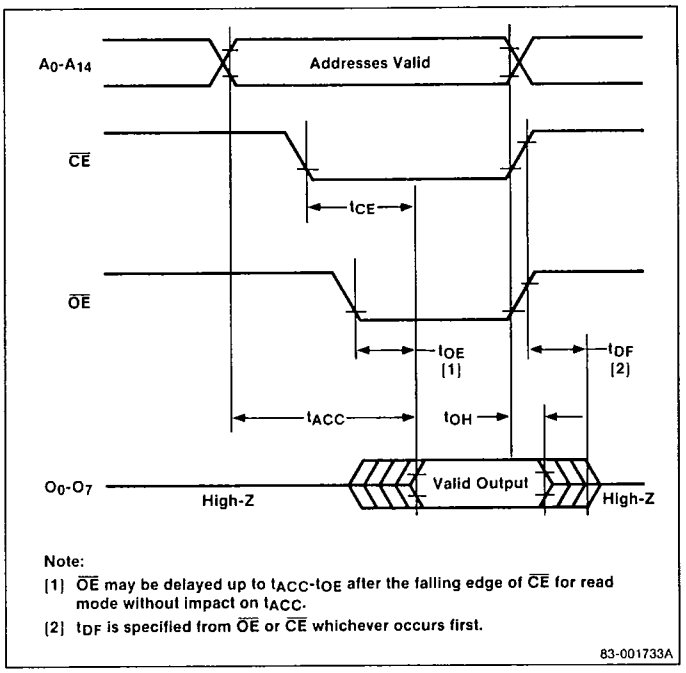
Erase data on the μPD27C256 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity × exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Read Mode



Note:
[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

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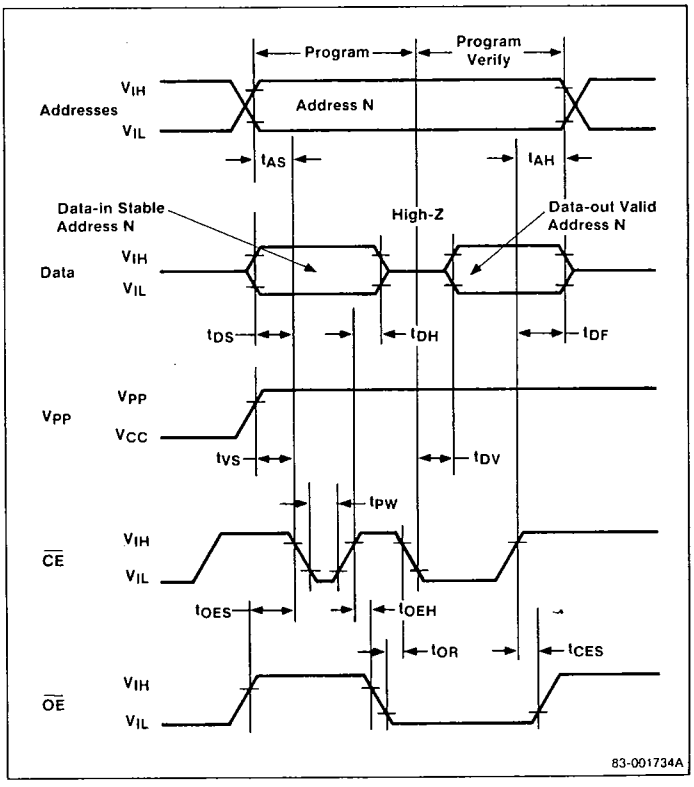
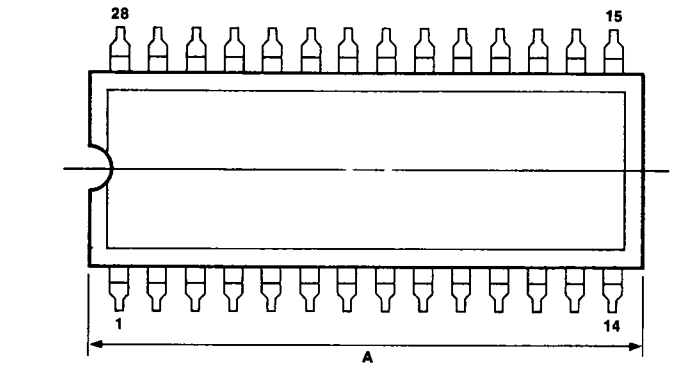
Program Mode

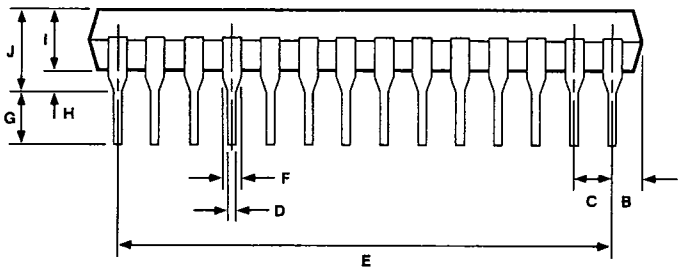


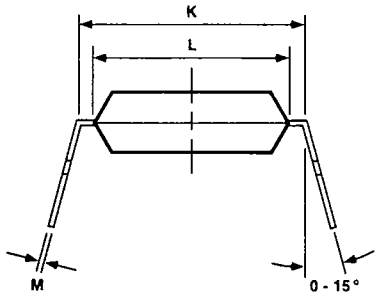
83-001734A

Packaging Information

28-Pin Plastic DIP Package (600 mil)







Item	Millimeters	Inches
A	38.10 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.1 [TP]
D	.5 ± .1	.02 ± .004
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24[TP]	.6[TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.002}$

Note:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

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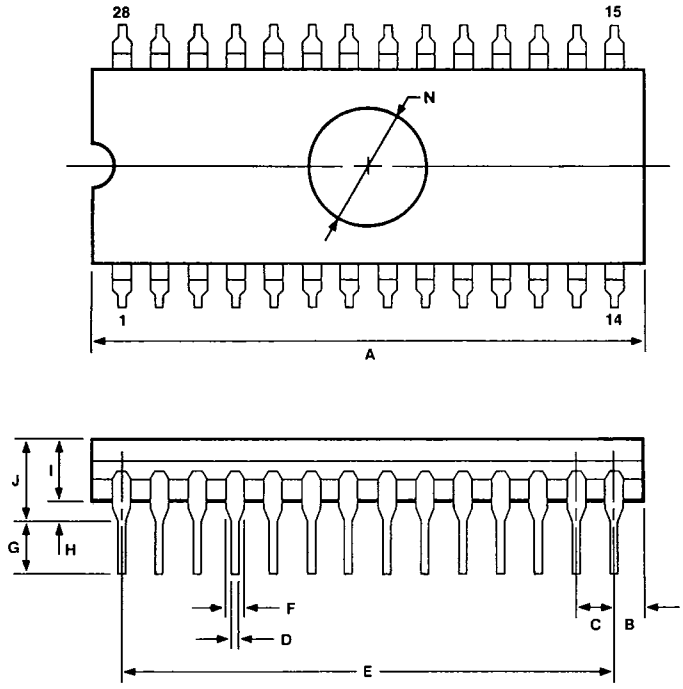
Packaging Information (cont)

28-Pin Cerdip Package



Item	Millimeters	Inches
A	38.10 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.1 [TP]
D	.5 ± .1	.020 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.2 max
K	15.24[TP]	.60[TP]
L	14.66	.577
M	.25 ± .05	.01 $^{+.002}_{-.003}$
N	8.89	.35

Note:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

83-001795B

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