Ultra Low Noise, Precision Voltage Reference

ISL21090

The ISL21090 is a ultra low noise, high DC accuracy precision voltage reference with wide input voltage range. The ISL21090 uses the new Intersil Advanced Bipolar technology to achieve sub 1.0µV_{P-P} (1.25V option) 0.1Hz to10Hz noise with an initial voltage accuracy of 0.02% (2.5V option).

The ISL21090 offers 1.25V, 2.5V, and 5.0V output voltage options with 7ppm/°C temperature coefficient and also provides excellent line and load regulation. These devices are offered in an 8 Ld SOIC package.

The ISL21090 is ideal for high-end instrumentation, data acquisition and processing applications requiring high DC precision where low noise performance is critical.

Applications

- High-End Instrumentation
- Precision Voltage Sources for Data Acquisition System, Industrial Control, Communication Infrastructure
- Process Control and Instrumentations
- Active Source for Sensors

Features

- Reference Output Voltage Option
  - 1.25V, 2.5V, and 5.0V (Released)
  - 7.5V (Coming Soon)
- Initial Accuracy:
  - ISL21090-12 . . . .±0.03%
  - ISL21090-25 . . . .±0.02%
  - ISL21090-50 . . . .±0.025%
- Output Voltage Noise (0.1Hz to 10Hz). . . . . .1.0µV_{P-P}Typ (1.25V Option)
- Supply Current .750µA (1.25V Option)
- Temperature Coefficient . . . . 7ppm/°C Max
- Output Current Capability 20mA
- Line Regulation . . . . 6ppm/V (1.25V Option)
- Load Regulation. . . . . .2.5ppm/mA (1.25V Option)
- Operating Temperature Range. . . . .-40°C to +125°C

Related Literature

See AN1764, "ISL21090XXEV1Z User's Guide"

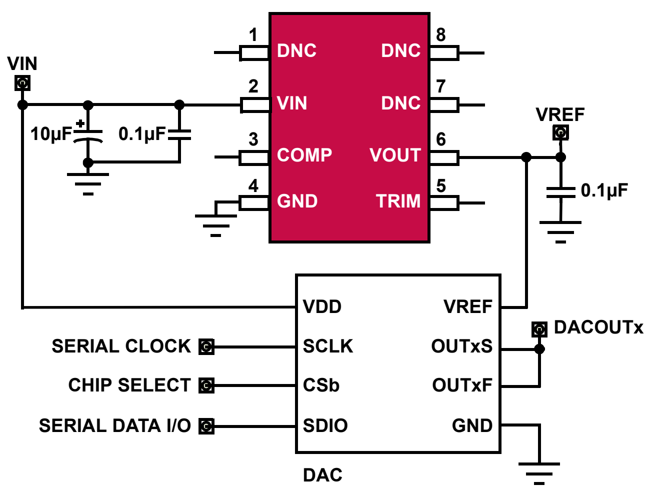


FIGURE 1. ISL21090 TYPICAL APPLICATION DIAGRAM

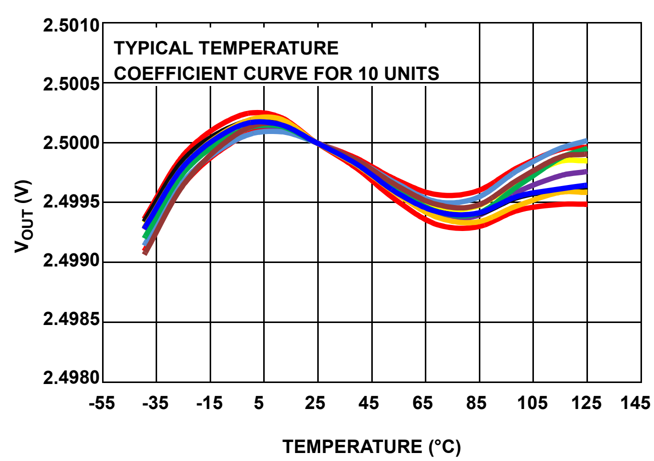
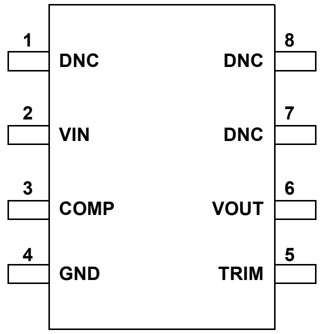


FIGURE 2. V_{OUT} vs TEMPERATURE (2.5V OPTION)

Pin Configuration

ISL21090
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 7, 8	DNC	Do Not Connect
2	VIN	Input Voltage Connection
3	COMP	Compensation and Noise Reduction Capacitor
4	GND	Ground Connection
5	TRIM	Voltage Reference Trim input
6	VOUT	Voltage Reference Output

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} OPTION (V)	GRADE (%)	TEMPCO (ppm/°C)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-Free)	PKG. DWG. #
ISL21090BFB812Z-TK	21090 BFZ12	1.25	0.03	7	-40 to +125	8 Ld SOIC	M8.15E
ISL21090BFB825Z-TK	21090 BFZ25	2.5	0.02	7	-40 to +125	8 Ld SOIC	M8.15E
ISL21090BFB850Z-TK	21090 BFZ50	5.0	0.02	7	-40 to +125	8 Ld SOIC	M8.15E
Coming Soon ISL21090BFB875Z-TK	21090 BFZ75	7.5	0.02	7	-40 to +125	8 Ld SOIC	M8.15E

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL21090B12, ISL21090B25, ISL21090B50. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

Max Voltage
- V_{IN} to GND . . . . -0.5V to +40V
- V_{OUT} to GND (10s) . . . . -0.5V to V_{OUT} + 0.5V

Voltage on any Pin to Ground . . . . -0.5V to +V_{OUT} + 0.5V
Voltage on DNC pins . . . . No connections permitted to these pins
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
- Human Body Model (Tested per JESD22-A114F) 3kV
- Machine Model (Tested per JESD22-A115-C) 200V
- Charged Device Model (Tested per JESD22-C110D) 2kV

Latch-up (Tested per JESD-78B; Class 2, Level A) . . . . at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5)	110	60

Continuous Power Dissipation (T_A = +125°C) 217mW
Maximum Junction Temperature (T_{JMAX}) . . . . +150°C
Storage Temperature Range . . . . -65°C to +150°C

Recommended Operating Conditions

Temperature Range (Industrial) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. Post-reflow drift for the ISL21090 devices can exceed 100µV to 1.0mV based on experimental results with devices on FR4 double sided boards. The system engineer must take this into account when considering the reference voltage after assembly.

Electrical Specifications

V_{IN} = 5V (1.25V option), I_{OUT} = 0, C_L = 0.1µF and Cc = 0.01µF, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{OUT}	Output Voltage	V_{IN} = 5V,		1.25		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C (Note 6)	V_{OUT} = 1.25V	-0.03		+0.03	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 8)	ISL21090 B grade			**7**	ppm/°C
V_{IN}	Input Voltage Range	V_{OUT} = 1.25V	**3.7**		**36**	V
I_{IN}	Supply Current			0.750	**1.28**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.7V to 36V, V_{OUT} = 1.25V		6	**17**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		2.5	**17**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		2.5	**17**	ppm/mA
V_D	Dropout Voltage (Note 9)	V_{OUT} = 1.25V @ 10mA		1.7	**2.15**	V
I_{SC+}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		53		mA
I_{SC-}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-23		mA
t_R	Turn-on Settling Time	90% of final value, C_L = 1.0µF, C_C = open		150		µs
	Ripple Rejection	f = 120Hz		90		dB
e_{np-p}	Voltage Noise	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 1.25V		1.0		μV_{P-P}
V_n	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz, V_{OUT} = 1.25V		1.2		μV_{RMS}
e_n	Noise Voltage Density	f = 1kHz, V_{OUT} = 1.25V		35.4		nV/√Hz
$\Delta V_{OUT}/\Delta t$	Long Term Stability	T_A = +25°C		20		ppm

Electrical Specifications

V_{IN} = 5V (2.5V option), I_{OUT} = 0 unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{OUT}	Output Voltage	V_{IN} = 5V		2.5		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C	All V_{OUT} options	-0.02		+0.02	%
TC V_{OUT}	Output Voltage Temperature Coefficient	ISL21090 B grade			**7**	ppm/°C
V_{IN}	Input Voltage Range	V_{OUT} = 2.5V	**3.7**		**36**	V
I_{IN}	Supply Current			0.930	**1.28**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.7V to 36V, V_{OUT} = 2.5V		8	**18**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		2.5	**17**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		2.5	**17**	ppm/mA
V_D	Dropout Voltage (Note 9)	V_{OUT} = 2.5V @ 10mA		1.1	**1.7**	V
I_{SC+}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		55		mA
I_{SC-}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-61		mA
t_R	Turn-on Settling Time	90% of final value, C_L = 1.0µF, C_C = open		150		µs
	Ripple Rejection	f = 120Hz		90		dB
e_{np-p}	Noise Voltage	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 2.5V		1.9		$µV_{P-P}$
V_n	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz, V_{OUT} = 2.5V		1.6		$µV_{RMS}$
e_n	Noise Voltage Density	f = 1kHz, V_{OUT} = 2.5V		50		nV/√Hz

Electrical Specifications

V_{IN} = 10.0V (5.0V option), I_{OUT} = 0unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{OUT}	Output Voltage	V_{IN} = 10.0V,		5.0		V
V_{OA}	V_{OUT} Accuracy @ T_A = +25°C (Note 6)	V_{OUT} = 5.0V	0.025		0.025	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 8)	ISL21090 B grade			**7**	ppm/°C
V_{IN}	Input Voltage Range	V_{OUT} = 5.0V	**7**		**36**	V
I_{IN}	Supply Current			0.930	**1.33**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 7.0V to 36V, V_{OUT} = 5.0V		8	**18**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		2.5	**17**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		2.5	**17**	ppm/mA
V_D	Dropout Voltage (Note 9)	V_{OUT} = 5.0V @ 10mA		1.1	**1.7**	V
I_{SC+}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to GND		61		mA
I_{SC-}	Short Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-75		mA
t_R	Turn-on Settling Time	90% of final value, C_L = 1.0µF, C_C = open		150		µs
	Ripple Rejection	f = 120Hz		90		dB

Electrical Specifications

V_{IN} = 10.0V (5.0V option), I_{OUT} = 0unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
e_{np-p}	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 5.0V		4.2		μV_{P-P}
V_n	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz, V_{OUT} = 5.0V		3.2		μV_{RMS}
e_n	Noise Voltage Density	f = 1kHz, V_{OUT} = 5.0V		100		nV/√Hz

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in VOUT is divided by the temperature range; in this case, -40°C to +125°C = +165°C.
9. Dropout Voltage is the minimum VIN - VOUT differential voltage measured at the point where VOUT drops 1mV from VIN = nominal at T_A = +25°C.

Typical Performance Curves (ISL21090-1.25V)

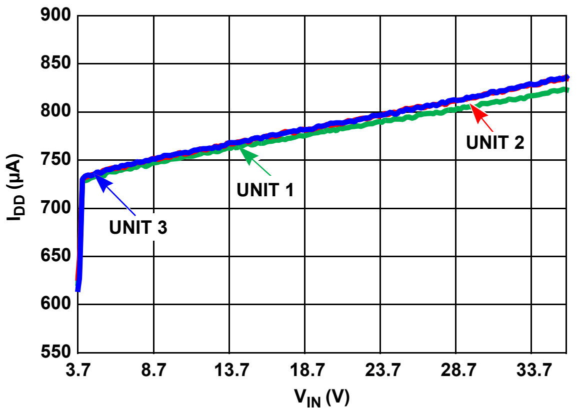


FIGURE 3. I_{IN} vs V_{IN}, THREE UNITS

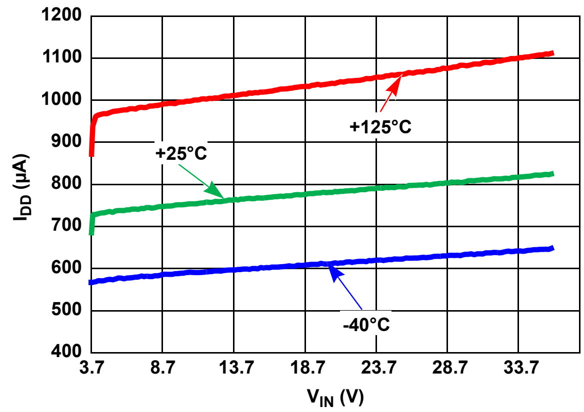


FIGURE 4. I_{IN} vs V_{IN}, THREE TEMPERATURES

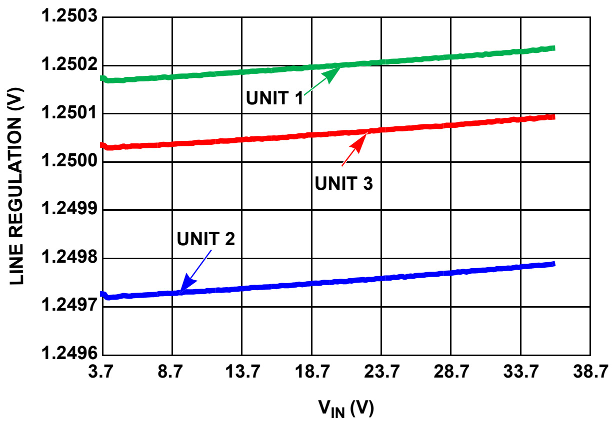


FIGURE 5. LINE REGULATION, THREE UNITS

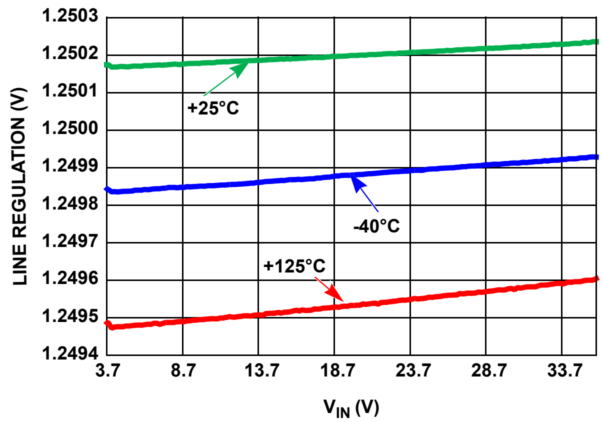


FIGURE 6. LINE REGULATION, THREE TEMPERATURES

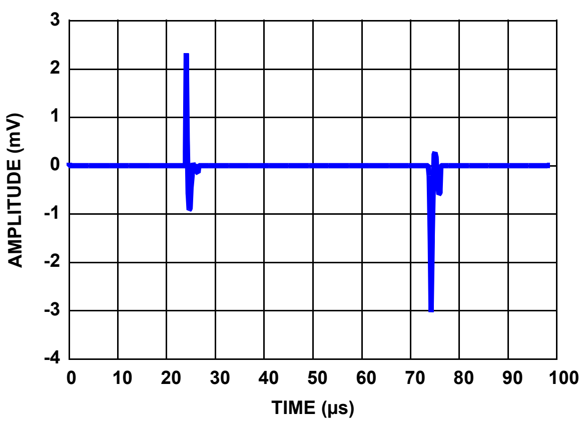


FIGURE 7. LINE TRANSIENT WITH 10nF LOAD (ΔV_{IN} = ±500mV)

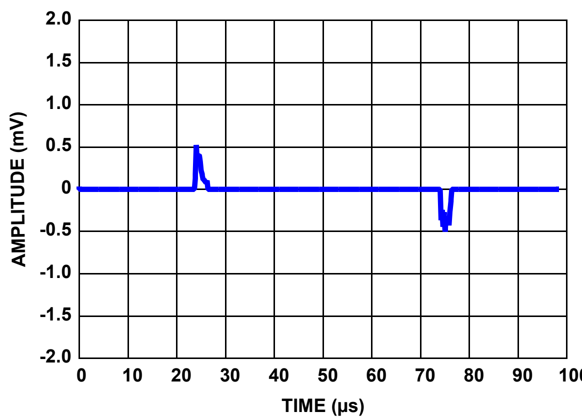


FIGURE 8. LINE TRANSIENT WITH 100nF LOAD (ΔV_{IN} = ±500mV)

Typical Performance Curves (ISL21090-1.25V) (Continued)

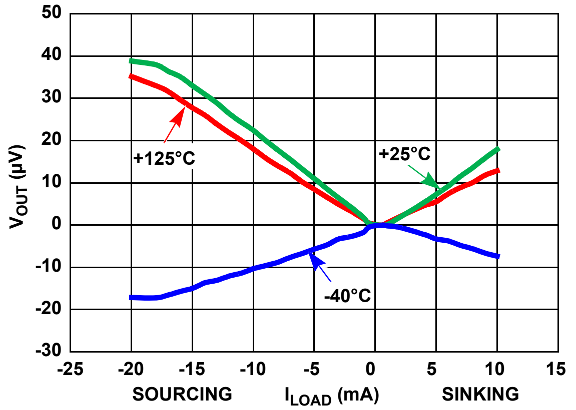


FIGURE 9. LOAD REGULATION, THREE TEMPERATURE

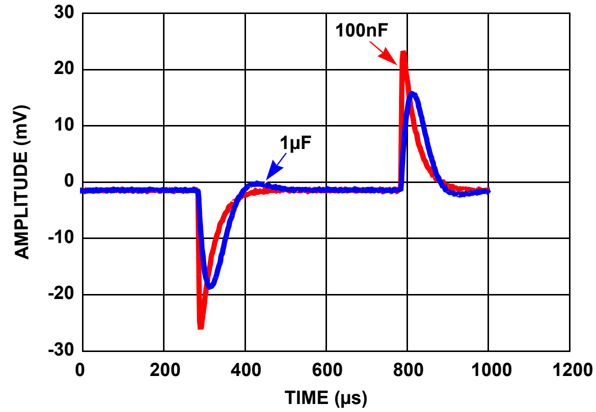


FIGURE 10. LOAD TRANSIENT (ΔI_{LOAD} = ±1mA)

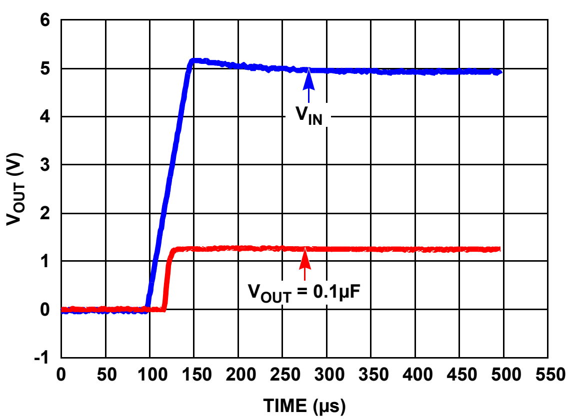


FIGURE 11. TURN ON TIME WITH 0.1µF

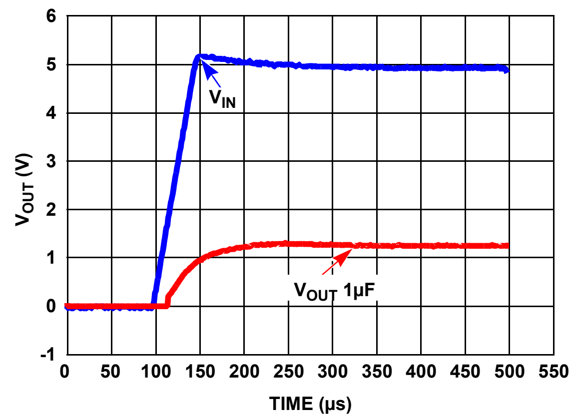


FIGURE 12. TURN ON TIME WITH 1µF

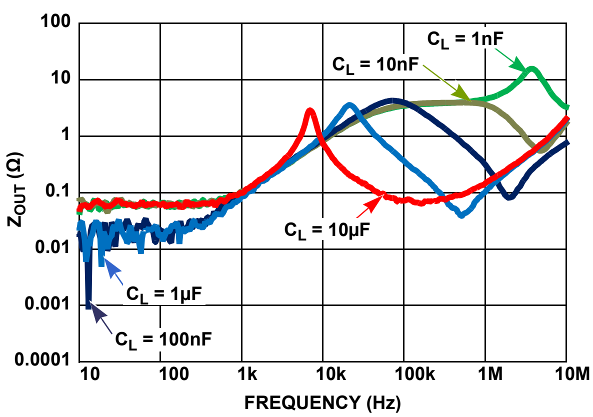


FIGURE 13. Z_{OUT} vs FREQUENCY (COMP = 0.01µF)

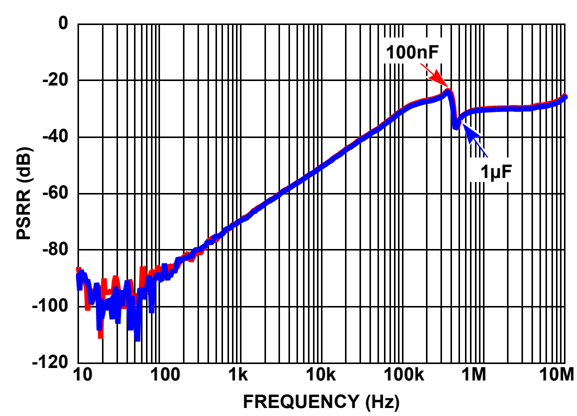


FIGURE 14. PSRR AT DIFFERENT CAPACITIVE LOADS

Typical Performance Curves (ISL21090-1.25V) (Continued)

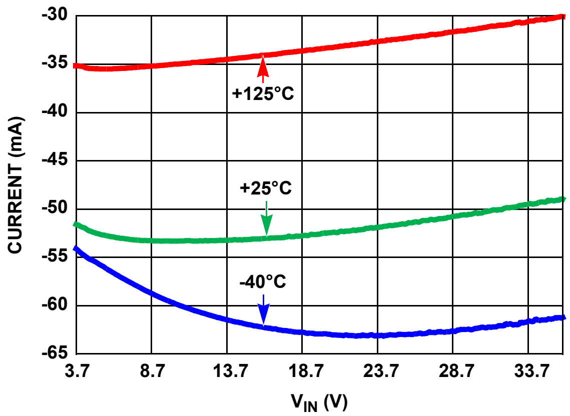


FIGURE 15. SHORT CIRCUIT TO GND

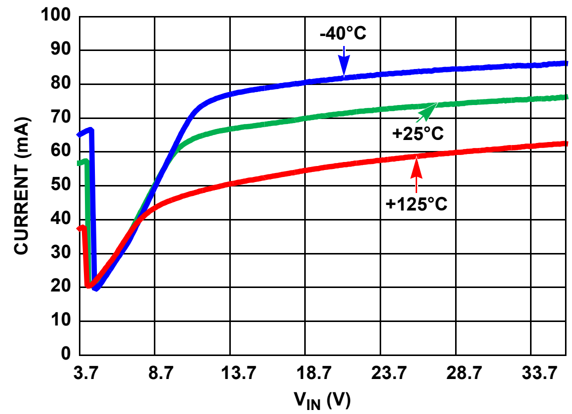


FIGURE 16. SHORT CIRCUIT TO V_{IN}

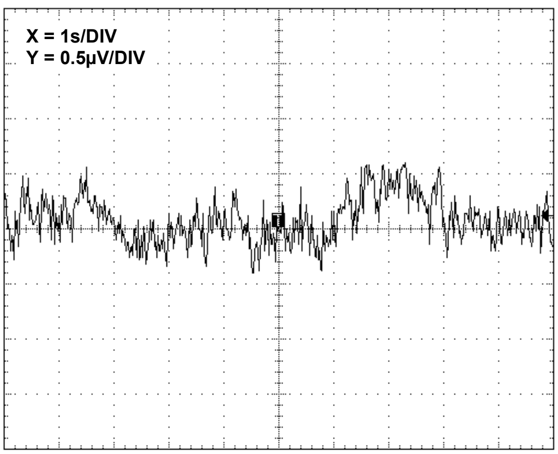


FIGURE 17. V_{OUT} vs NOISE, 0.1Hz TO 10Hz

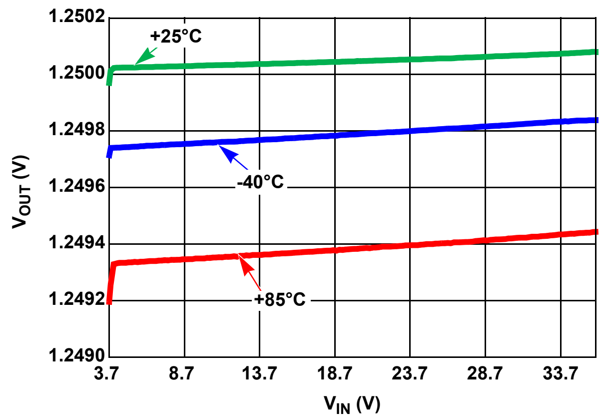


FIGURE 18. DROPOUT WITH -10mA LOAD

Typical Performance Curves (ISL21090-2.5)

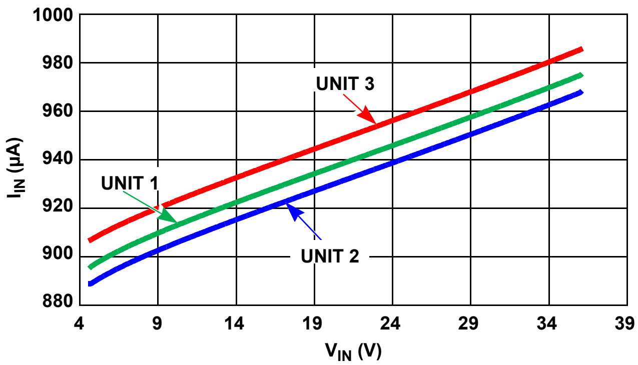


FIGURE 19. I_{IN} vs V_{IN}, THREE UNITS

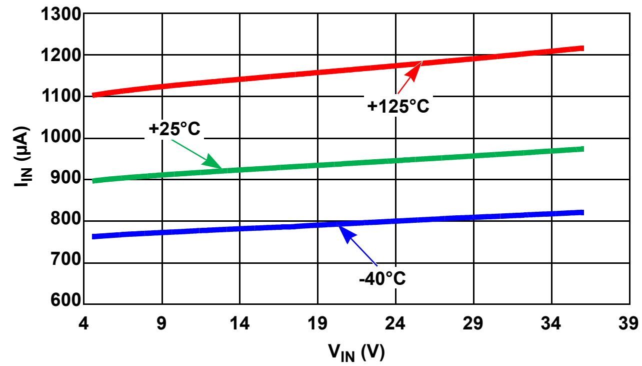


FIGURE 20. I_{IN} vs V_{IN}, THREE TEMPERATURES

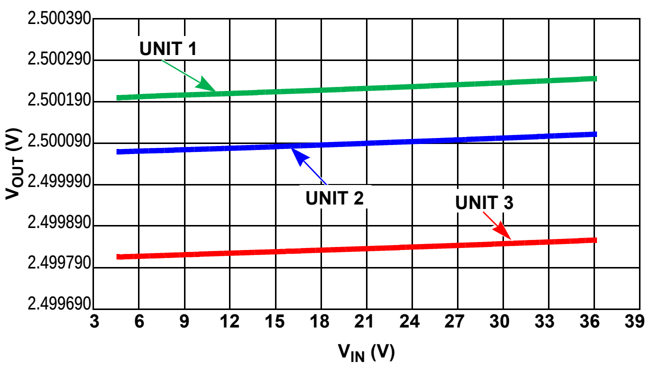


FIGURE 21. LINE REGULATION, THREE UNITS

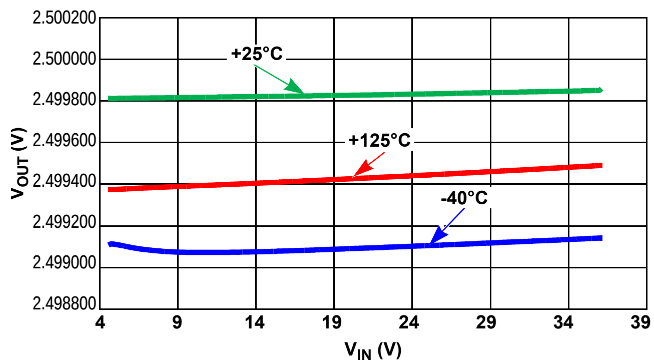


FIGURE 22. LINE REGULATION, THREE TEMPERATURES

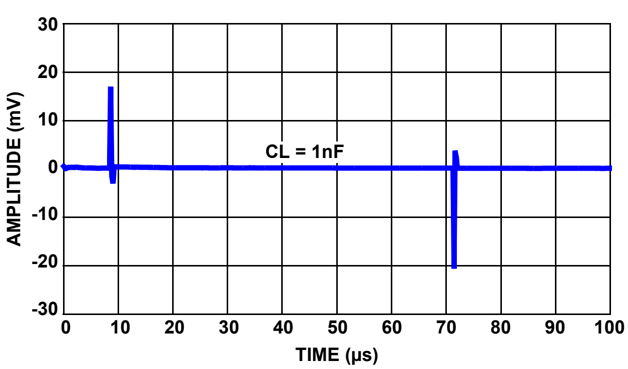


FIGURE 23. LINE TRANSIENT WITH 1nF LOAD (ΔV_{IN} = ±500mV)

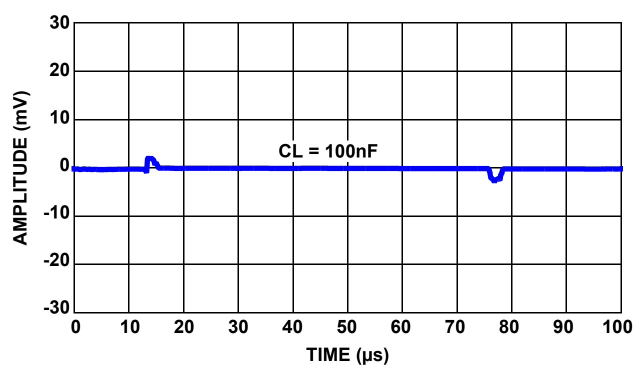


FIGURE 24. LINE TRANSIENT WITH 100nF LOAD (ΔV_{IN} = ±500mV)

Typical Performance Curves (ISL21090-2.5) (Continued)

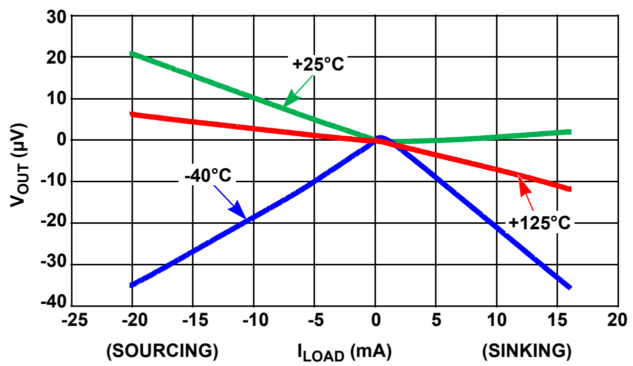


FIGURE 25. LOAD REGULATION, THREE TEMPERATURES

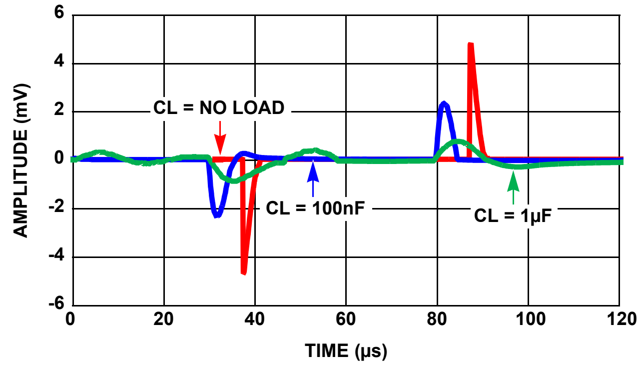


FIGURE 26. LOAD TRANSIENT (ΔI_{LOAD} = ±1mA)

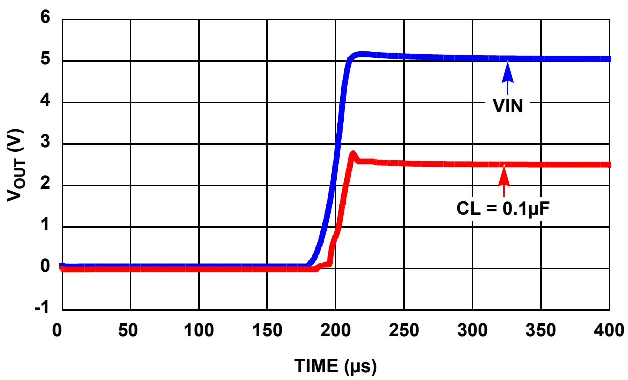


FIGURE 27. TURN-ON TIME WITH 0.1µF

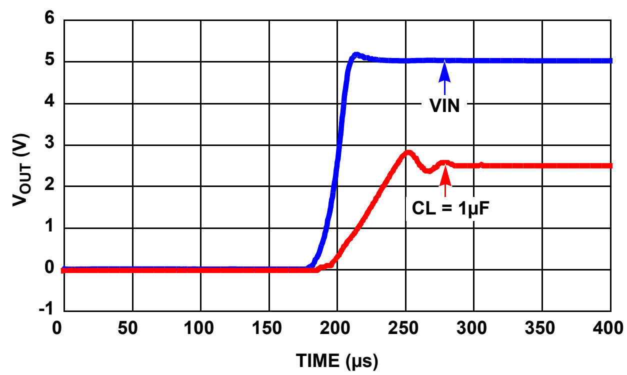


FIGURE 28. TURN-ON TIME WITH 1µF

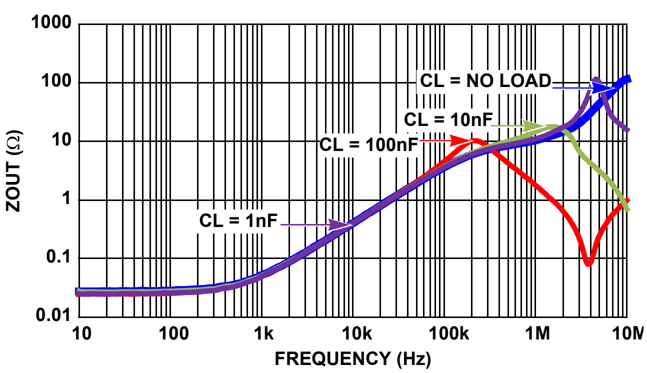


FIGURE 29. Z_{OUT} vs FREQUENCY

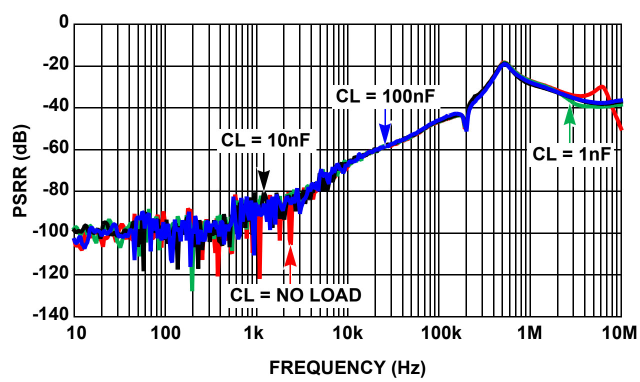


FIGURE 30. PSRR AT DIFFERENT CAPACITIVE LOADS

Typical Performance Curves (ISL21090-2.5) (Continued)

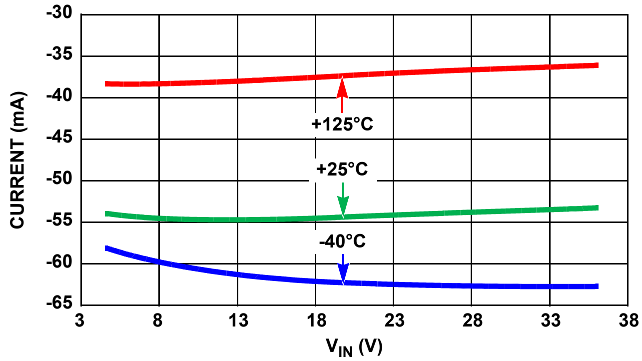


FIGURE 31. SHORT-CIRCUIT TO GND

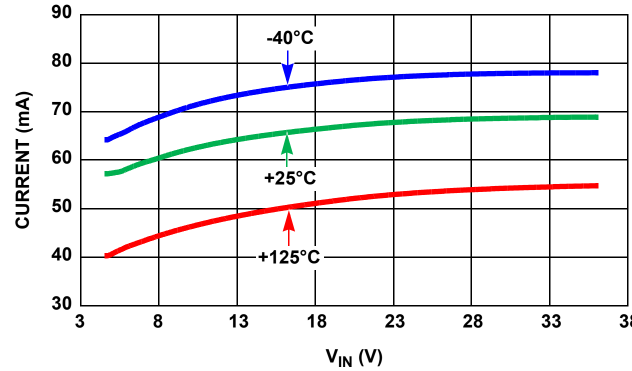


FIGURE 32. SHORT-CIRCUIT TO V_{IN}

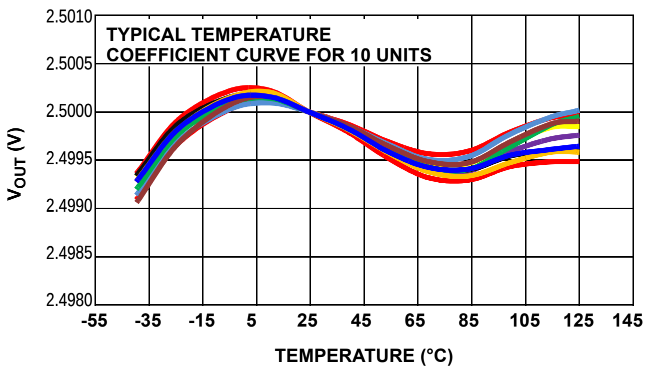


FIGURE 33. V_{OUT} vs TEMPERATURE, 10 UNITS

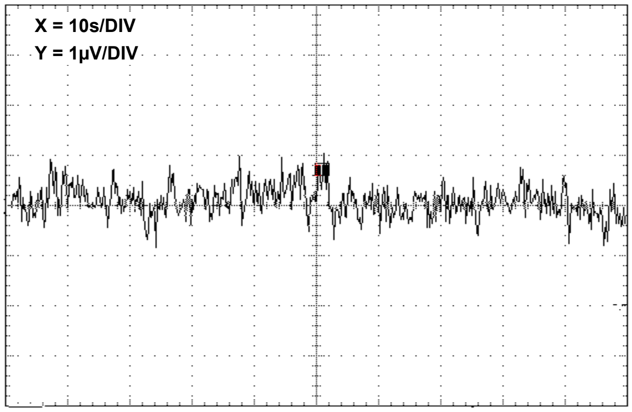


FIGURE 34. V_{OUT} vs NOISE, 0.1Hz TO 10Hz

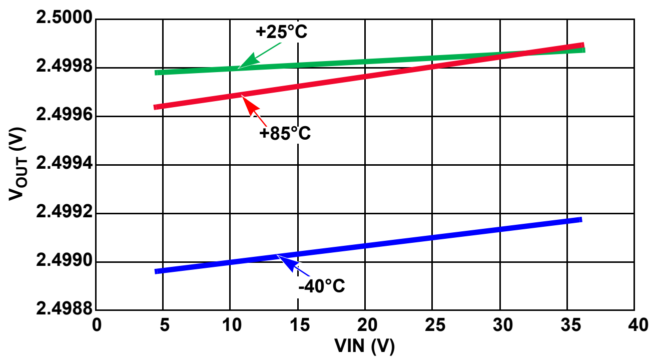


FIGURE 35. DROPOUT WITH -10mA LOAD

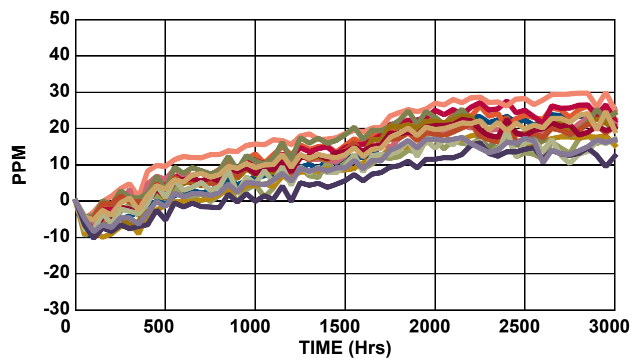


FIGURE 36. LONG TERM STABILITY

Typical Performance Curves (ISL21090-5.0)

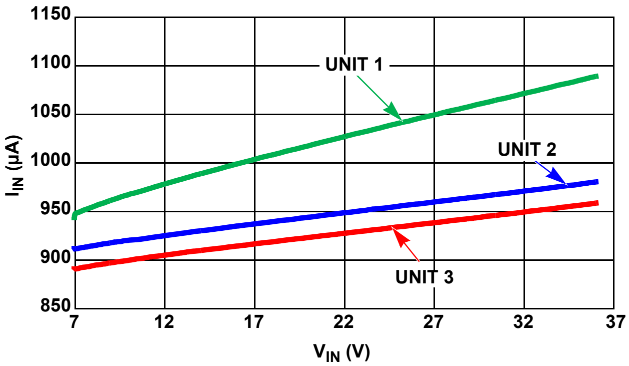


FIGURE 37. I_{IN} vs V_{IN}, THREE UNITS

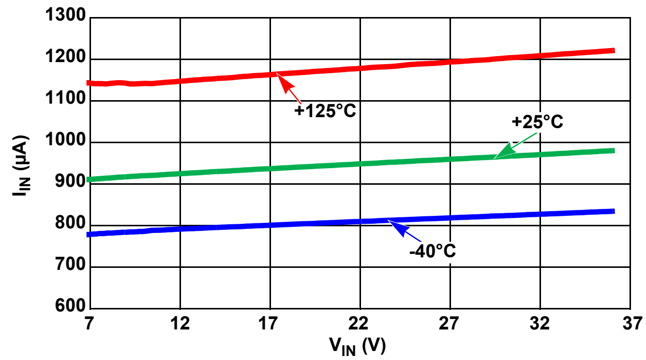


FIGURE 38. I_{IN} vs V_{IN}, THREE TEMPERATURES

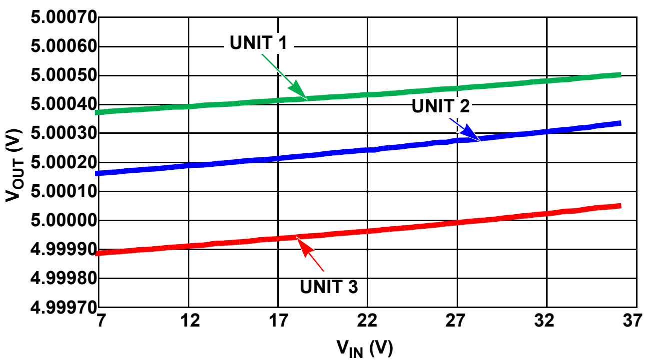


FIGURE 39. LINE REGULATION, THREE UNITS

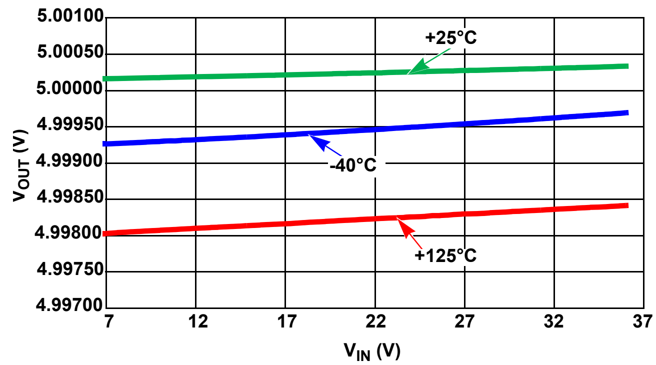


FIGURE 40. LINE REGULATION, THREE TEMPERATURES

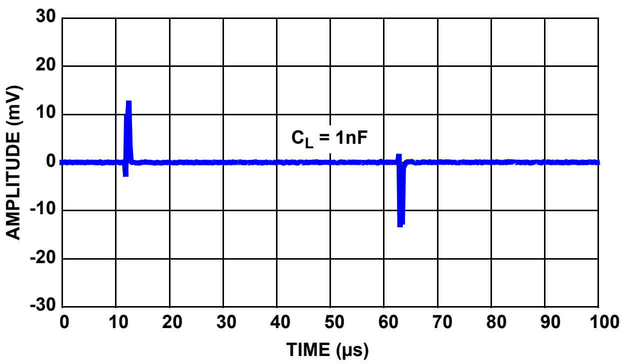


FIGURE 41. LINE TRANSIENT WITH 1nF LOAD (ΔV_{IN} = ±500mV)

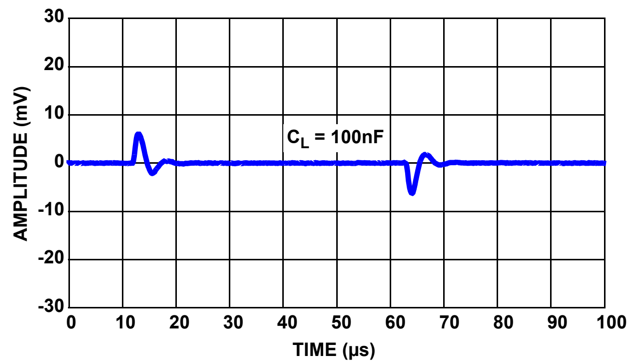


FIGURE 42. LINE TRANSIENT WITH 100nF LOAD (ΔV_{IN} = ±500mV)

Typical Performance Curves (ISL21090-5.0) (Continued)

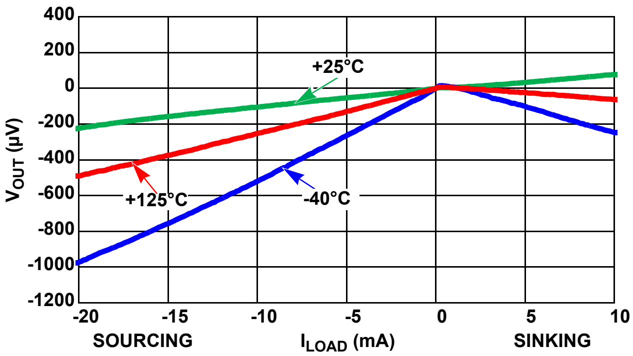


FIGURE 43. LOAD REGULATION, THREE TEMPERATURES

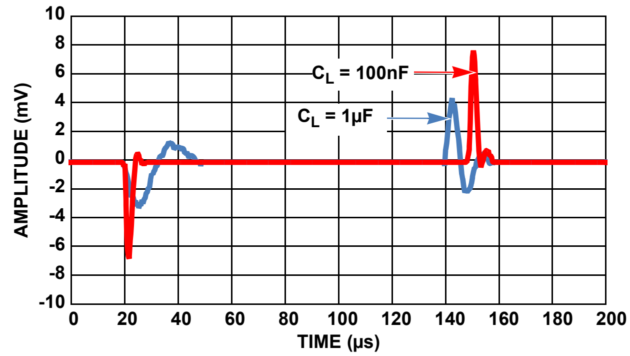


FIGURE 44. LOAD TRANSIENT (ΔI_{LOAD} = ±1mA)

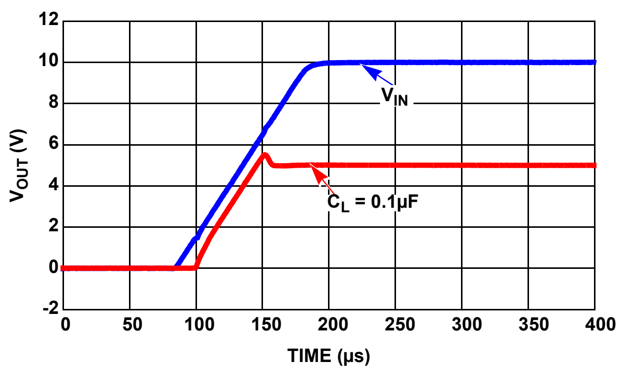


FIGURE 45. TURN-ON TIME WITH 0.1µF

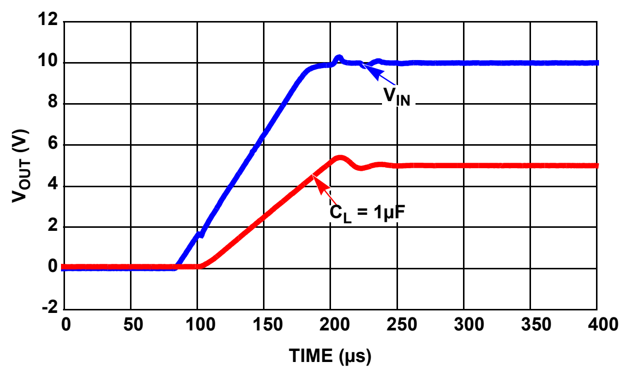


FIGURE 46. TURN-ON TIME WITH 1µF

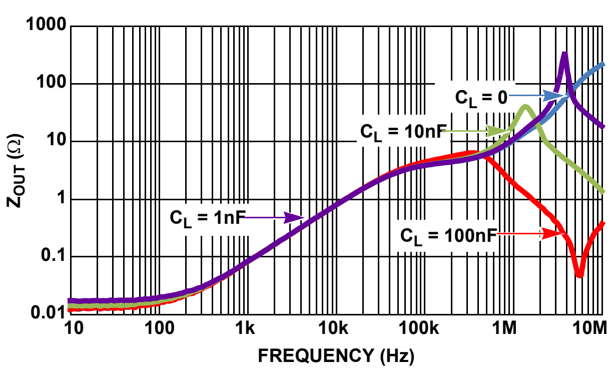


FIGURE 47. Z_{OUT} vs FREQUENCY

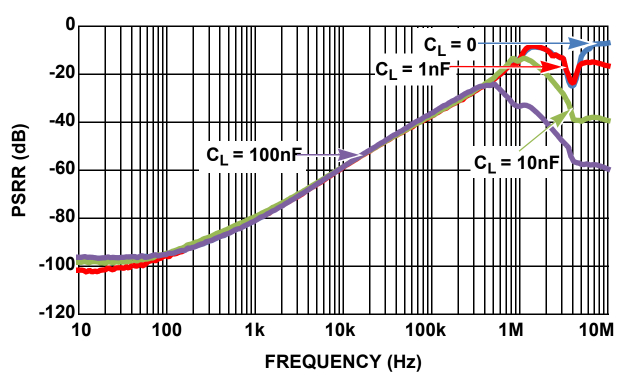


FIGURE 48. PSRR AT DIFFERENT CAPACITIVE LOADS

Typical Performance Curves (ISL21090-5.0) (Continued)

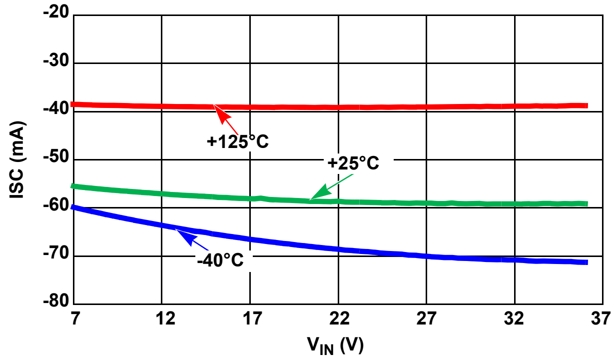


FIGURE 49. SHORT-CIRCUIT TO GND

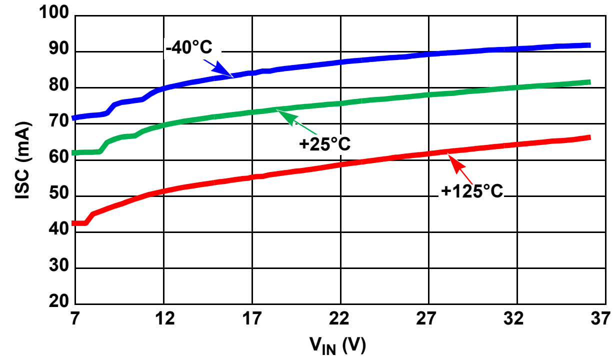


FIGURE 50. SHORT-CIRCUIT TO V_{IN}

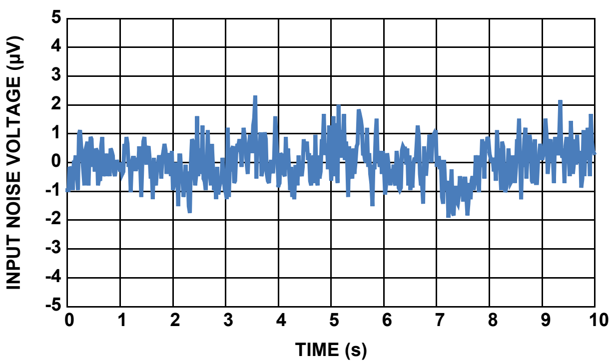


FIGURE 51. V_{OUT} vs NOISE, 0.1Hz TO 10Hz

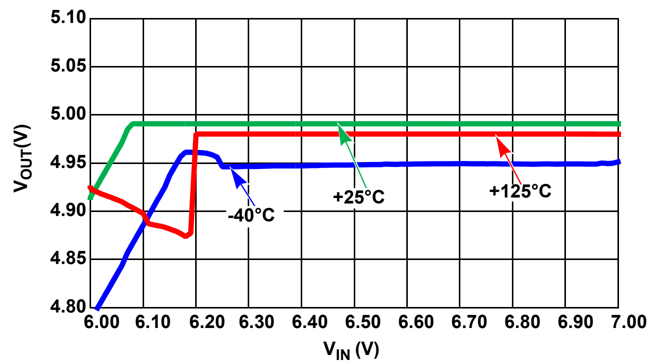


FIGURE 52. DROPOUT WITH -10mA LOAD

Device Operation

Precision Bandgap Reference

The ISL21090 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive. Low noise performance is achieved using optimized biasing techniques. Key features for precision low noise portable applications, such as handheld meters and instruments are supply current (900µA) and noise (0.1Hz to 10Hz bandwidth) $1.0µV_{P-P}$ to $4.6µV_{P-P}$. Data Converters in particular can utilize the ISL21090 as an external voltage reference. Low power DAC and ADC circuits will realize maximum resolution with lowest noise. The device maintains output voltage during conversion cycles with fast response, although it is helpful to add an output capacitor, typically 1µF. In case of the 1.25V option, a 0.01µF capacitor must be added to the COMP (pin 3) for stabilization purposes. and a minimum of 0.1µF capacitor must be added at the output.

Applications Information

Board Mounting Considerations

For applications requiring the highest accuracy, the board mounting location should be reviewed. The device uses a plastic SOIC package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of 100µV to 500µV can be expected with Pb-free reflow profiles or wave solder on multi-layer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically $1.9µV_{P-P}$ (V_{OUT} = 2.5V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately $1.6µV_{RMS}$ (V_{OUT} = 2.5V), with 0.1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added but will result in only marginal improvements in output noise and transient response.

Turn-On Time

Normal turn-on time is typically 150µs, as shown in Figure 28. The circuit designer must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, ($V_{HIGH} - V_{LOW}$), and divide by the temperature extremes of measurement ($T_{HIGH} - T_{LOW}$). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The positive input of the amplifier is about 1.216V, and in feedback, so will be the trim voltage. The trim terminal has a 5000Ω resistor to ground internally, and in the case of the 2.5V output version, there is a feedback resistor of approximately 5000Ω from V_{OUT} to trim.

The suggested method to adjust the output is to connect a very high value external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a much lower total resistance and whose outer terminals connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. It is important to minimize the capacitance on the trim terminal to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 22, 2012	FN6993.3	Added 5.0V option "Typical Performance Curves" table to page 12. Removed 7.5V and 10V option Electrical Specs
May 1, 2012	FN6993.2	Added 5.0V option "Electrical Specifications" table to page 4. Added 7.5V option "Electrical Specifications" table to page 5. Added 10.0V option "Electrical Specifications" table to page 5.
March 5, 2012	FN6993.1	Added 1.25V option "Electrical Specifications" table to page 3. Added 1.25V Typical Performance Curves section on page 6. Changed MIN limit for V_{IN} 2.5V option on page 4.
June 8, 2011	FN6993.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL21090B12, ISL21090B25, ISL21090B50

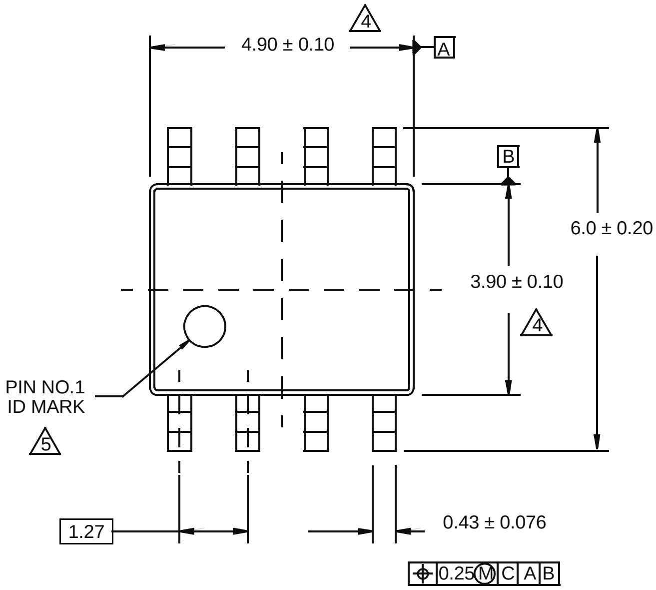
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

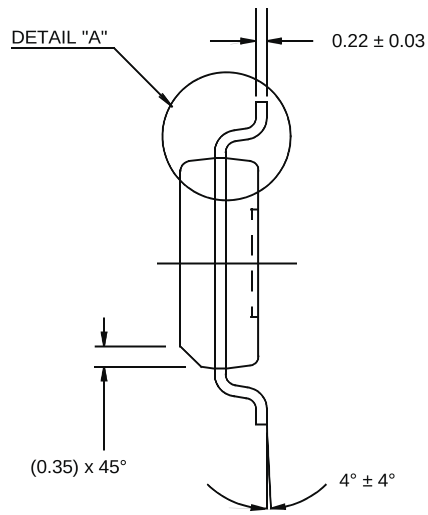
Package Outline Drawing

M8.15E

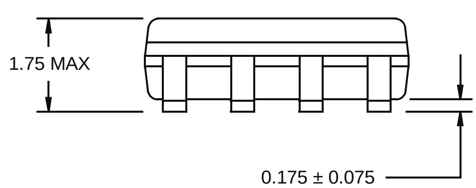
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



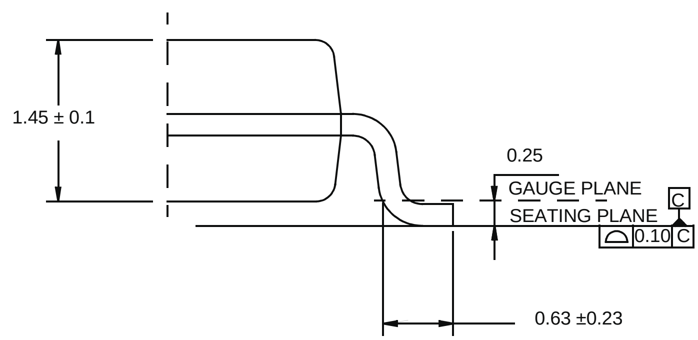
TOP VIEW



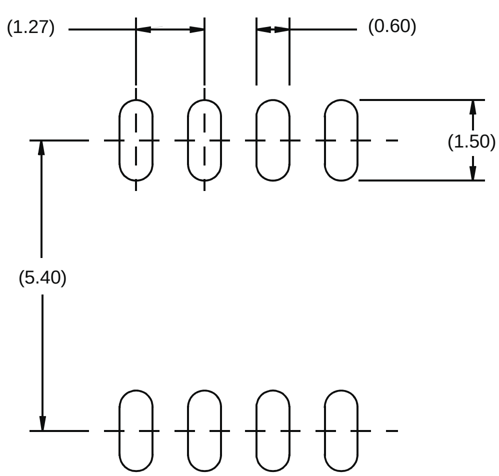
SIDE VIEW "B"



SIDE VIEW "A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.