

### General Description

The AOD3N40 has been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications.

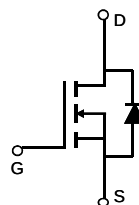
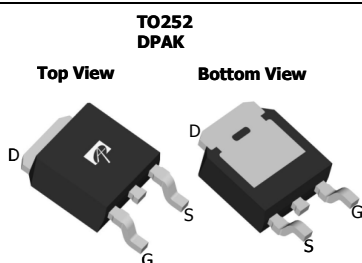
By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability this device can be adopted quickly into new and existing offline power supply designs.

### Product Summary

|                                 |            |
|---------------------------------|------------|
| $V_{DS}$                        | 500V@150°C |
| $I_D$ (at $V_{GS}=10V$ )        | 2.6A       |
| $R_{DS(ON)}$ (at $V_{GS}=10V$ ) | < 3.1Ω     |

100% UIS Tested!

100%  $R_g$  Tested!



AOD3N40

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter                                                                    | Symbol         | Maximum    | Units |
|------------------------------------------------------------------------------|----------------|------------|-------|
| Drain-Source Voltage                                                         | $V_{DS}$       | 400        | V     |
| Gate-Source Voltage                                                          | $V_{GS}$       | $\pm 30$   | V     |
| Continuous Drain Current <sup>B</sup>                                        | $I_D$          | 2.6        | A     |
| $T_C=25^\circ\text{C}$                                                       |                | 1.6        |       |
| $T_C=100^\circ\text{C}$                                                      |                |            |       |
| Pulsed Drain Current <sup>C</sup>                                            | $I_{DM}$       | 5.6        |       |
| Avalanche Current <sup>C</sup>                                               | $I_{AR}$       | 1.5        | A     |
| Repetitive avalanche energy <sup>C</sup>                                     | $E_{AR}$       | 34         | mJ    |
| Single pulsed avalanche energy <sup>H</sup>                                  | $E_{AS}$       | 68         | mJ    |
| Peak diode recovery dv/dt                                                    | dv/dt          | 5          | V/ns  |
| Power Dissipation <sup>B</sup>                                               | $P_D$          | 50         | W     |
|                                                                              |                | 0.4        | W/°C  |
| $T_C=25^\circ\text{C}$                                                       |                |            |       |
| Derate above 25°C                                                            |                |            |       |
| Junction and Storage Temperature Range                                       | $T_J, T_{STG}$ | -50 to 150 | °C    |
| Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds | $T_L$          | 300        | °C    |

### Thermal Characteristics

| Parameter                                  | Symbol          | Typical | Maximum | Units |
|--------------------------------------------|-----------------|---------|---------|-------|
| Maximum Junction-to-Ambient <sup>A,G</sup> | $R_{\theta JA}$ | 46      | 55      | °C/W  |
| Maximum Case-to-sink <sup>A</sup>          | $R_{\theta CS}$ | -       | 0.5     | °C/W  |
| Maximum Junction-to-Case <sup>D,F</sup>    | $R_{\theta JC}$ | 2.1     | 2.5     | °C/W  |

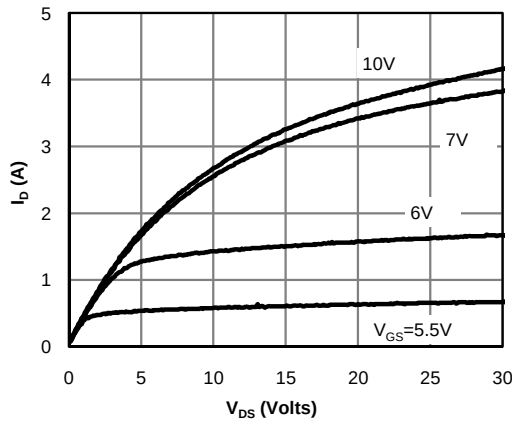
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

| Symbol                                | Parameter                             | Conditions                                                                                | Min | Typ  | Max  | Units |
|---------------------------------------|---------------------------------------|-------------------------------------------------------------------------------------------|-----|------|------|-------|
| <b>STATIC PARAMETERS</b>              |                                       |                                                                                           |     |      |      |       |
| BV <sub>DSS</sub>                     | Drain-Source Breakdown Voltage        | I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C                          | 400 |      |      | V     |
|                                       |                                       | I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C                         |     | 500  |      |       |
| BV <sub>DSS</sub><br>/ΔT <sub>J</sub> | Zero Gate Voltage Drain Current       | I <sub>D</sub> =250μA, V <sub>GS</sub> =0V                                                |     | 0.4  |      | V/°C  |
| I <sub>DSS</sub>                      | Zero Gate Voltage Drain Current       | V <sub>DS</sub> =400V, V <sub>GS</sub> =0V                                                |     |      | 1    | μA    |
|                                       |                                       | V <sub>DS</sub> =320V, T <sub>J</sub> =125°C                                              |     |      | 10   |       |
| I <sub>GSS</sub>                      | Gate-Body leakage current             | V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V                                                |     |      | ±100 | nA    |
| V <sub>GS(th)</sub>                   | Gate Threshold Voltage                | V <sub>DS</sub> =5V, I <sub>D</sub> =250μA                                                | 3.4 | 4    | 4.5  | V     |
| R <sub>DS(ON)</sub>                   | Static Drain-Source On-Resistance     | V <sub>GS</sub> =10V, I <sub>D</sub> =1A                                                  |     | 2.5  | 3.1  | Ω     |
| g <sub>FS</sub>                       | Forward Transconductance              | V <sub>DS</sub> =40V, I <sub>D</sub> =1A                                                  |     | 1.7  |      | S     |
| V <sub>SD</sub>                       | Diode Forward Voltage                 | I <sub>S</sub> =1A, V <sub>GS</sub> =0V                                                   |     | 0.8  | 1    | V     |
| I <sub>S</sub>                        | Maximum Body-Diode Continuous Current |                                                                                           |     |      | 2.6  | A     |
| I <sub>SM</sub>                       | Maximum Body-Diode Pulsed Current     |                                                                                           |     |      | 5.6  | A     |
| <b>DYNAMIC PARAMETERS</b>             |                                       |                                                                                           |     |      |      |       |
| C <sub>iss</sub>                      | Input Capacitance                     | V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz                                         | 145 | 186  | 225  | pF    |
| C <sub>oss</sub>                      | Output Capacitance                    |                                                                                           | 15  | 26   | 37   | pF    |
| C <sub>rss</sub>                      | Reverse Transfer Capacitance          |                                                                                           | 1.2 | 2.1  | 4.1  | pF    |
| R <sub>g</sub>                        | Gate resistance                       | V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz                                          | 2.2 | 4.4  | 6.6  | Ω     |
| <b>SWITCHING PARAMETERS</b>           |                                       |                                                                                           |     |      |      |       |
| Q <sub>g</sub>                        | Total Gate Charge                     | V <sub>GS</sub> =10V, V <sub>DS</sub> =320V, I <sub>D</sub> =2.6A                         | 3.3 | 4.2  | 5.1  | nC    |
| Q <sub>gs</sub>                       | Gate Source Charge                    |                                                                                           | 1.2 | 1.7  | 2.1  | nC    |
| Q <sub>gd</sub>                       | Gate Drain Charge                     |                                                                                           | 0.5 | 1.0  | 1.5  | nC    |
| t <sub>D(on)</sub>                    | Turn-On DelayTime                     | V <sub>GS</sub> =10V, V <sub>DS</sub> =200V, I <sub>D</sub> =2.6A,<br>R <sub>G</sub> =25Ω |     | 14   |      | ns    |
| t <sub>r</sub>                        | Turn-On Rise Time                     |                                                                                           |     | 10   |      | ns    |
| t <sub>D(off)</sub>                   | Turn-Off DelayTime                    |                                                                                           |     | 18   |      | ns    |
| t <sub>f</sub>                        | Turn-Off Fall Time                    |                                                                                           |     | 8    |      | ns    |
| t <sub>rr</sub>                       | Body Diode Reverse Recovery Time      | I <sub>F</sub> =2.6A, dI/dt=100A/μs, V <sub>DS</sub> =100V                                | 110 | 140  | 170  | ns    |
| Q <sub>rr</sub>                       | Body Diode Reverse Recovery Charge    | I <sub>F</sub> =2.6A, dI/dt=100A/μs, V <sub>DS</sub> =100V                                | 0.5 | 0.64 | 0.8  | μC    |

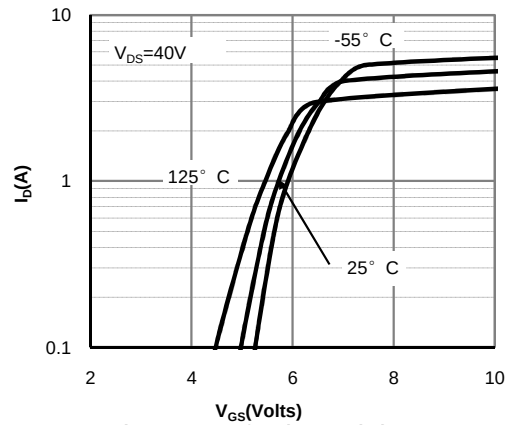
- A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25° C.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.
- G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.
- H. L=60mH, I<sub>AS</sub>=1.5A, V<sub>DD</sub>=150V, R<sub>G</sub>=10Ω, Starting T<sub>J</sub>=25° C

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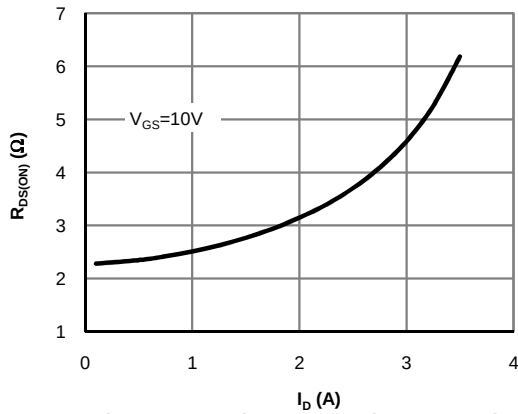
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



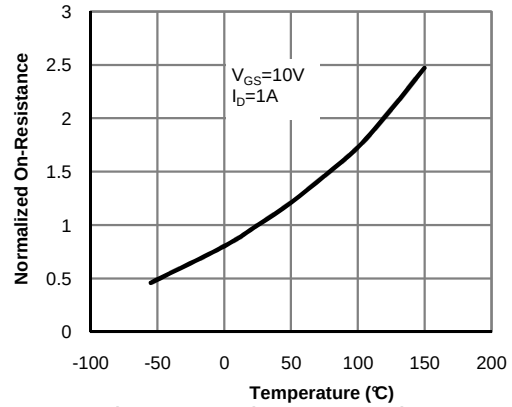
**Fig 1: On-Region Characteristics**



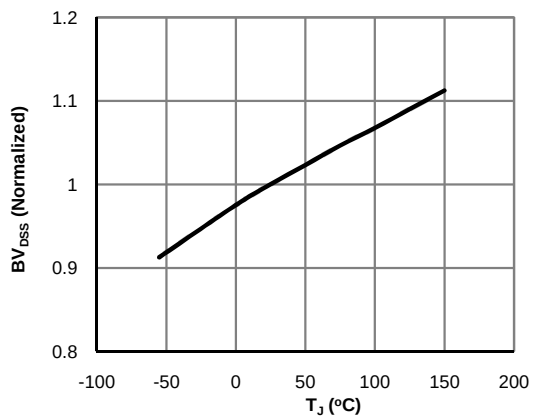
**Figure 2: Transfer Characteristics**



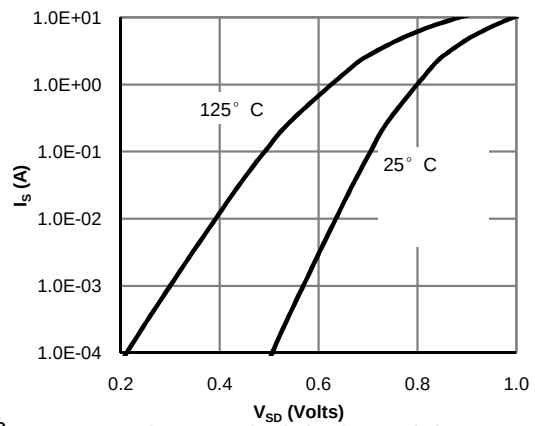
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

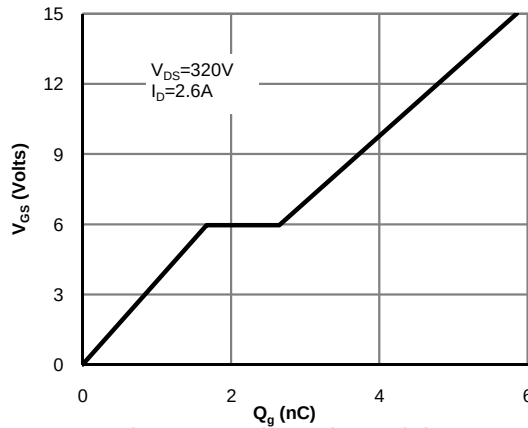


**Figure 5: Break Down vs. Junction Temperature**

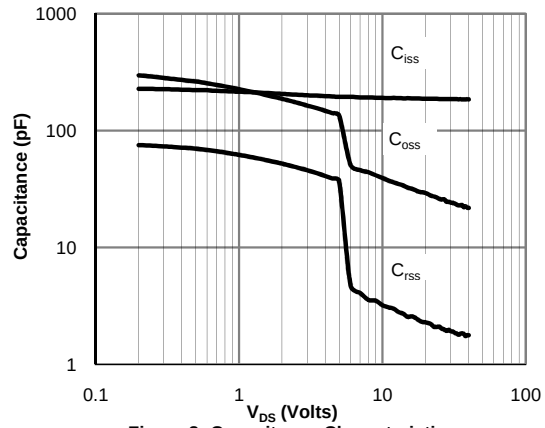


**Figure 6: Body-Diode Characteristics**

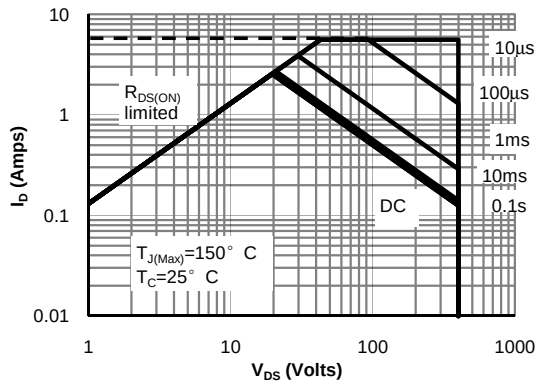
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



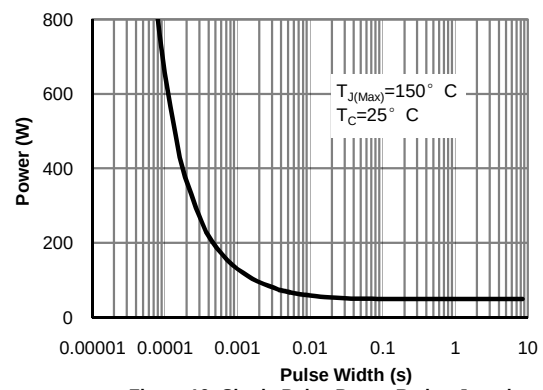
**Figure 7: Gate-Charge Characteristics**



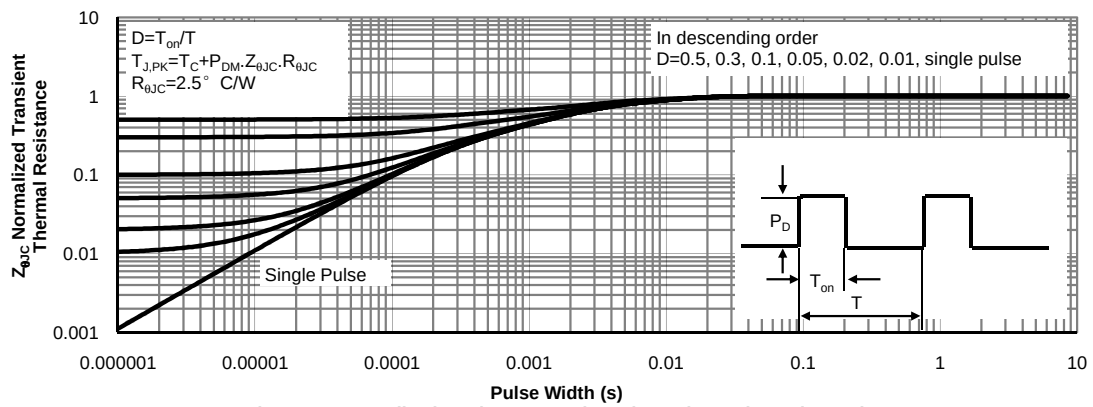
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

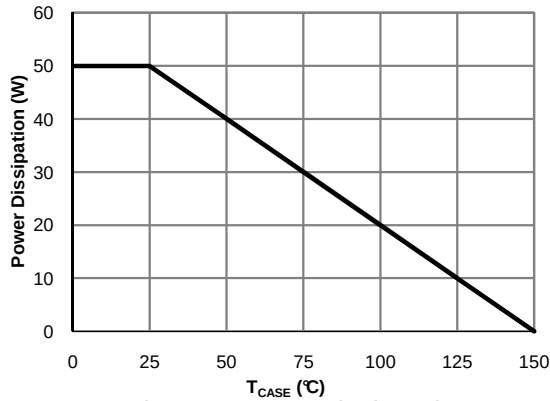


Figure 12: Power De-rating (Note B)

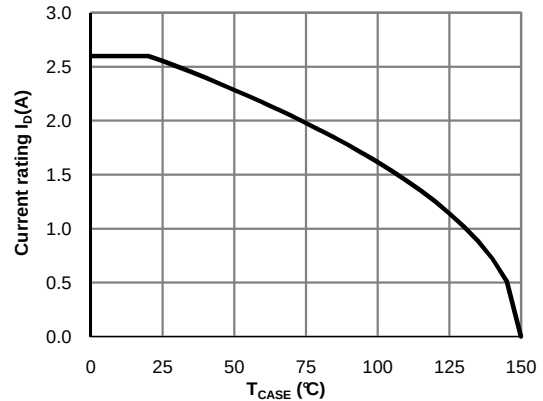


Figure 13: Current De-rating (Note B)

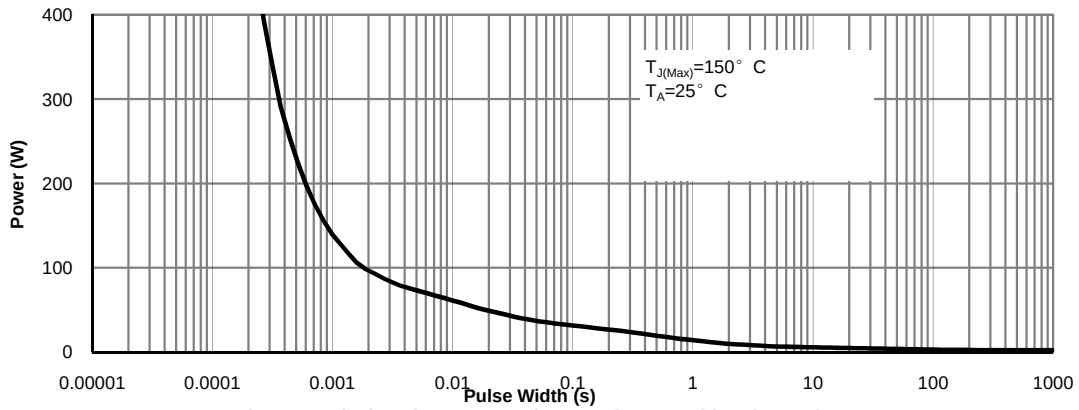


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

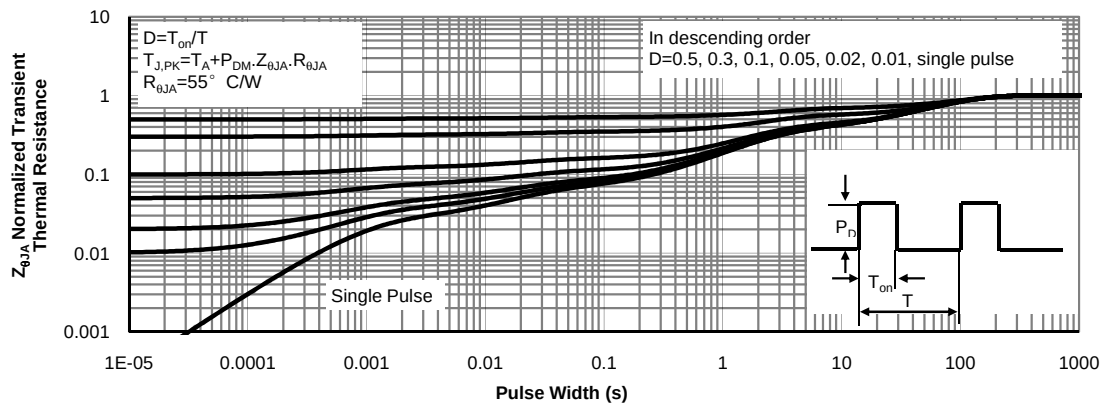
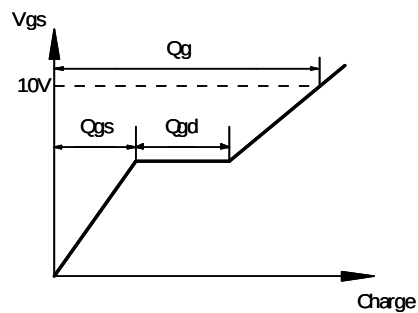
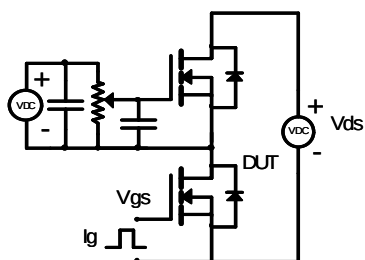
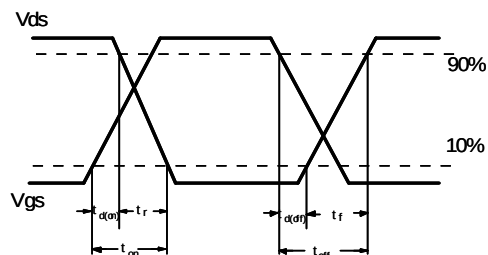
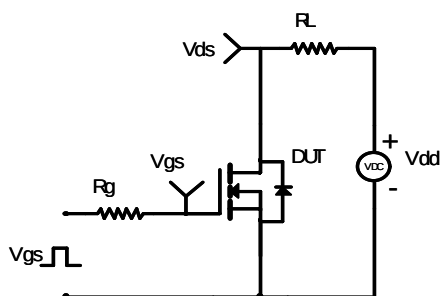


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

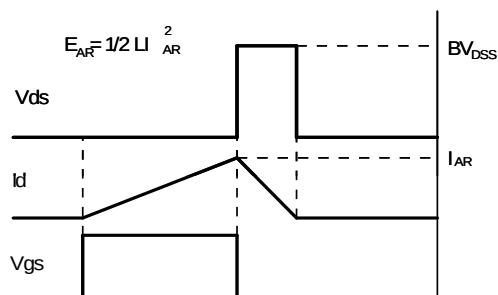
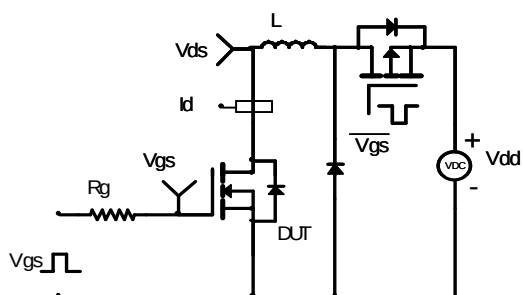
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

