Totally Logical

Z86D73

40/44-PIN LOW-VOLTAGE IR OTP

FEATURES

Device	OTP (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86D73	32	236	31	2.0V to 3.6V

Note: *General-Purpose

- Low Power Consumption–40 mW (Typical)
- Three Standby Modes
  - STOP—2µA
  - HALT—0.8mA
  - Low Voltage
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers and Two Load Registers
  - One Programmable 16-Bit Counter/Timer with One 16-Bit Capture Register Pair and One 16-Bit Load Register Pair
  - Programmable Input Glitch Filter for Pulse Reception
- Six Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
  - One Low Voltage Detection
- Low Voltage Detection with Flag
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- Mask Selectable 200 ±50% KΩ Pull-Up Transistors on Ports 0, 1, 2, 3
- Programmable Mask Options:
  - Oscillator Selection: RC Oscillator vs. Crystal or Other Clock Source
  - Oscillator Operational Mode: Normal High Frequency Operation Enabled or 32KHz Operation Enabled
  - Port 0: 0–3 Pull-Ups
  - Port 0: 4–7 Pull-Ups
  - Port 1: 0–3 Pull-Ups
  - Port 1: 4–7 Pull-Ups
  - Port 2: 0–7 Pull-Ups
  - Port 3: Pull-Ups
  - Port 0: 0–3 Mouse Mode: Normal Mode (.5V_{DD} Input Threshold) vs. Mouse Mode (.4V_{DD} Input Threshold)

GENERAL DESCRIPTION

The Z86D73 is an OTP-based member of the Z8 MCU family of IR (infrared) microcontrollers. With 237 bytes of general-purpose RAM and 32 KB of OTP memory, ZiLOG's CMOS microcontrollers offers fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86D73 architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many

GENERAL DESCRIPTION (Continued)

consumer, automotive, computer peripheral, and battery operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers and 236 General Purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86D73 offer a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 13).

Note: All Signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low), and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

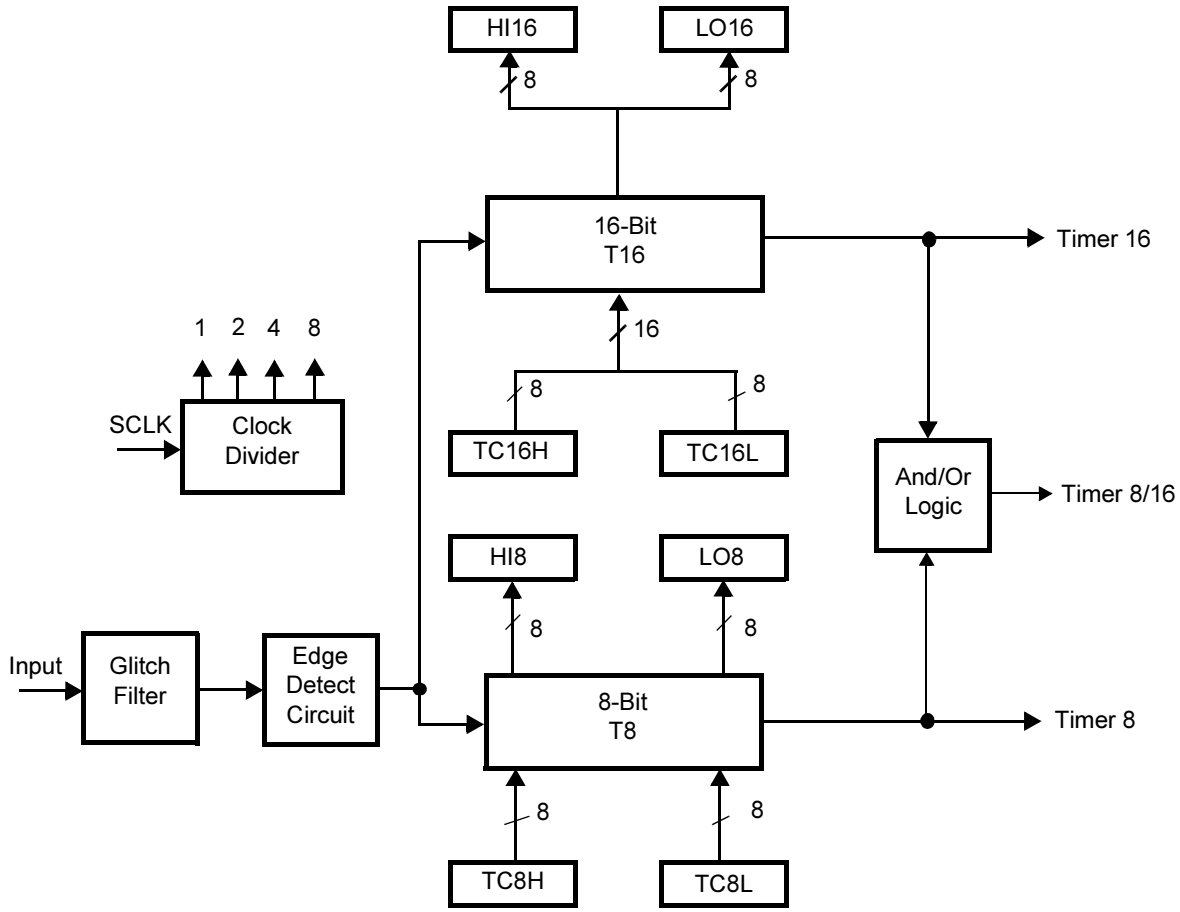

Figure 1. Counter/Timers Diagram

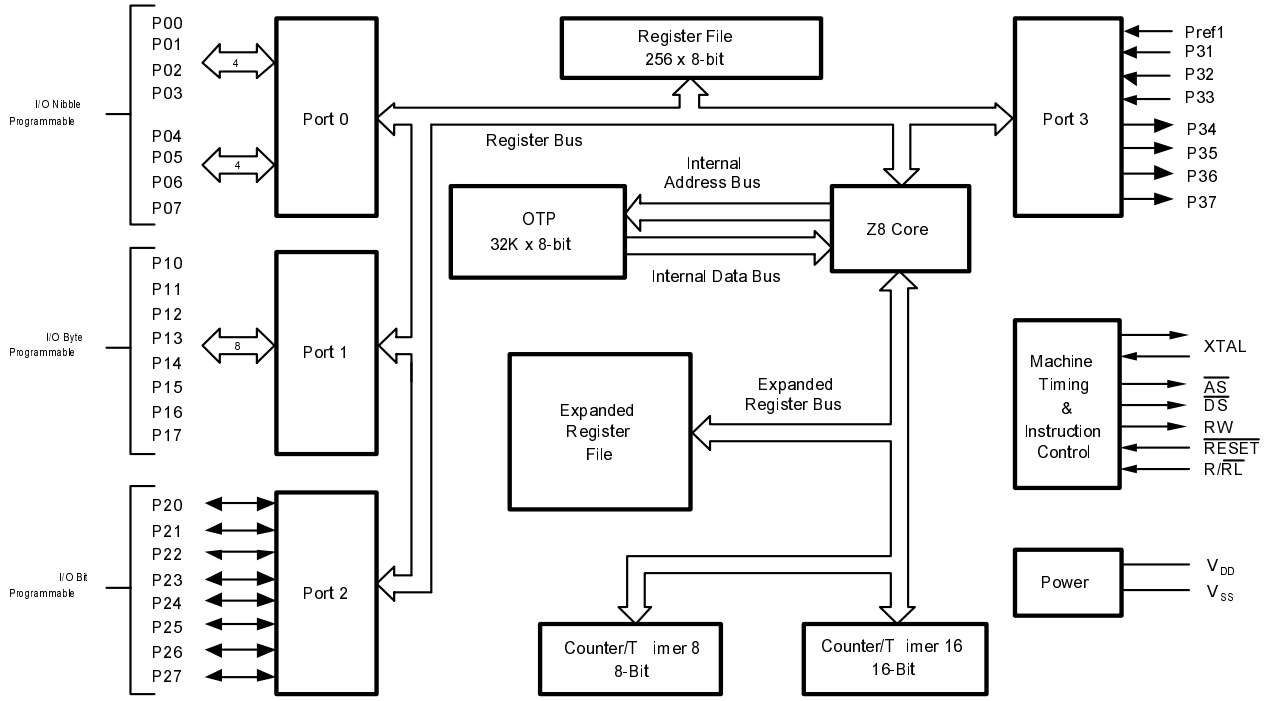

Figure 2. Functional Block Diagram

PIN DESCRIPTION

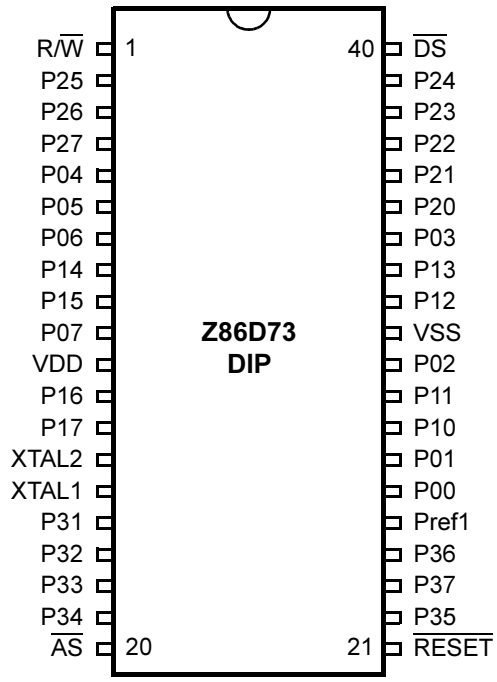

Figure 3. 40-pin DIP/SOIC Pin Assignment

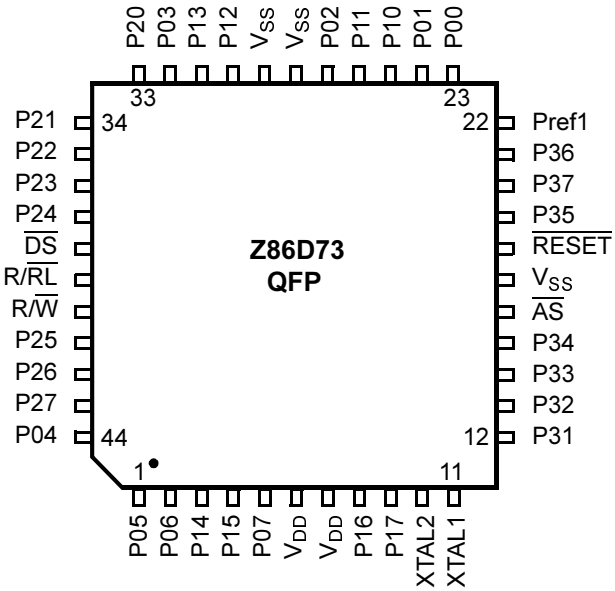

Figure 4. 44-pin QFP Pin Assignment

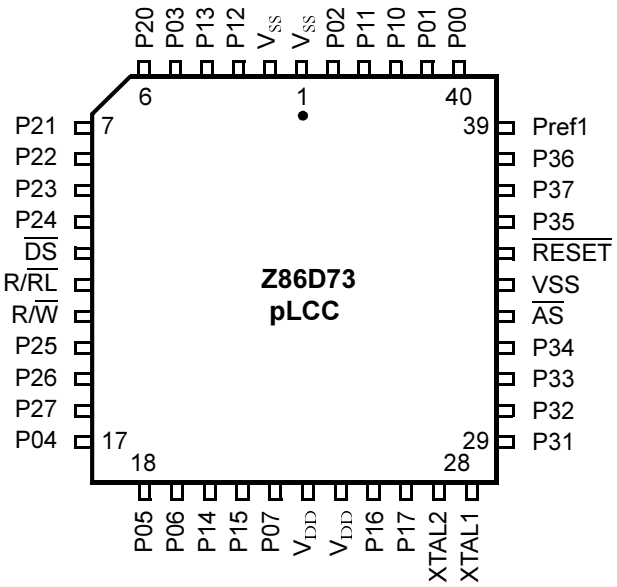

Figure 5. 44-Pin QFP Pin Assignment

Table 1. Pin Identification

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	Symbol
26	40	23	P00
27	41	24	P01
30	44	27	P02
34	5	32	P03
5	17	44	P04
6	18	1	P05
7	19	2	P06
10	22	5	P07
28	42	25	P10
29	43	26	P11
32	3	30	P12
33	4	31	P13
8	20	3	P14
9	21	4	P15
12	25	8	P16
13	26	9	P17
35	6	33	P20
36	7	34	P21
37	8	35	P22
38	9	36	P23
39	10	37	P24

PIN DESCRIPTION (Continued)

Table 1. Pin Identification (Continued)

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	Symbol
2	14	41	P25
3	15	42	P26
4	16	43	P27
16	29	12	P31
17	30	13	P32
18	31	14	P33
19	32	15	P34
22	36	19	P35
24	38	21	P36
23	37	20	P37
20	33	16	$\overline{AS}$
40	11	38	$\overline{DS}$
1	13	40	R/$\overline{W}$
21	35	18	$\overline{RESET}$
15	28	11	XTAL1
14	27	10	XTAL2
11	23,24	6,7	V_{DD}
31	1,2, 34	17,28,29	V_{SS}
25	39	22	Pref1
	12	39	R/$\overline{RL}$

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes:
*Voltage on all pins with respect to GND.
†See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 6).

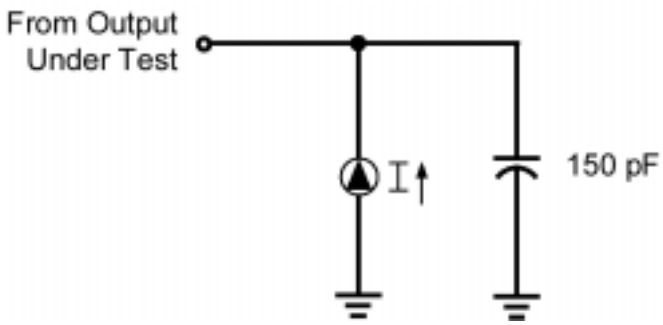

Figure 6. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS

Table 2. DC Characteristics

			T_A = 0°C to +70°C				
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
	Max Input Voltage	2.0V		7	V	I_{IN} <250 µA	
		3.6V		7	V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
		3.6V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
		3.6V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	V		
		3.6V	0.7 V_{CC}	V_{CC} + 0.3	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS}–0.3	0.2 V_{CC}	V		
		3.6V	V_{SS}–0.3	0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
		3.6V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0V	V_{CC}–0.8		V	I_{OH} = –7 mA	
		3.6V	V_{CC}–0.8		V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0V		0.4	V	I_{OL} = 1.0 mA	
		3.6V		0.4	V	I_{OL} = 4.0 mA	
V_{OL2}*	Output Low Voltage	2.0V		0.8	V	I_{OL} = 5.0 mA	
		3.6V		0.8	V	I_{OL} = 7.0 mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0V		0.8	V	I_{OL} = 10 mA	
		3.6V		0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	mV		
		3.6V		25	mV		
V_{REF}	Comparator Reference Voltage	2.0V	0	V_{DD}–1.75	mV		
		3.6V	0	V_{DD}–1.75	mV		
I_{IL}	Input Leakage	2.0V	–1	1	µA	V_{IN} = O_V, V_{CC}	
		3.6V	–1	1	µA	V_{IN} = O_V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1	1	µA	V_{IN} = O_V, V_{CC}	
		3.6V	–1	1	µA	V_{IN} = O_V, V_{CC}	
I_{CC}	Supply Current	2.0V		10	mA	@ 8.0 MHz	1,2
		3.6V		15	mA	@ 8.0 MHz	1,2
		2.0V		250	µA	@ 32 kHz	1,2,3
		3.6V		850	µA	@ 32 kHz	1,2,3

Table 2. DC Characteristics (Continued)

		T_A = 0°C to +70°C					
Sym	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current (HALT Mode)	2.0V		3	mA	V_{IN} = O_V, V_{CC} @ 8.0 MHz	1,2
		3.6V		5	mA	Same as above	1,2
		2.0V		2	mA	Clock Divide-by-16 @ 8.0 MHz	1,2
		3.6V		4	mA	Same as above	1,2
I_{CC2}	Standby Current (STOP Mode)	2.0V		8	µA	V_{IN} = O_V, V_{CC} WDT is not Running	4,5
		3.6V		10	µA	Same as above	4,5
		2.0V		500	µA	V_{IN} = O_V, V_{CC} WDT is Running	4,5
		3.6V		800	µA	Same as above	4,5
I_{LV}	Standby Current (Low Voltage)			25	µA	V_{CC} < V_{BO}	6
					µA		
T_{POR}	Power-On Reset	2.0V	12	75	ms		
		3.6V	5	20	ms		
V_{BO}	V_{CC} Low Voltage Protection			2.15	V	8 MHz max Ext. CLK Freq.	7
V_{LVD}	V_{CC} Low Voltage Protection			V_{BO} + 0.4		V_{LVD} = V_{BO} +0.4V	8

Notes:
*All Outputs excluding P00, P01, P36, and P37.

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. 32 kHz clock driver input.
4. The V_{BO} increases as the temperature decreases, except inputs at V_{CC}.
5. Oscillator stopped.
6. Oscillator stops when V_{CC} falls below $_{VLV}$ limit.
7. The V_{BO} increases as the temperature decreases.
8. Variance is 300 mV.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

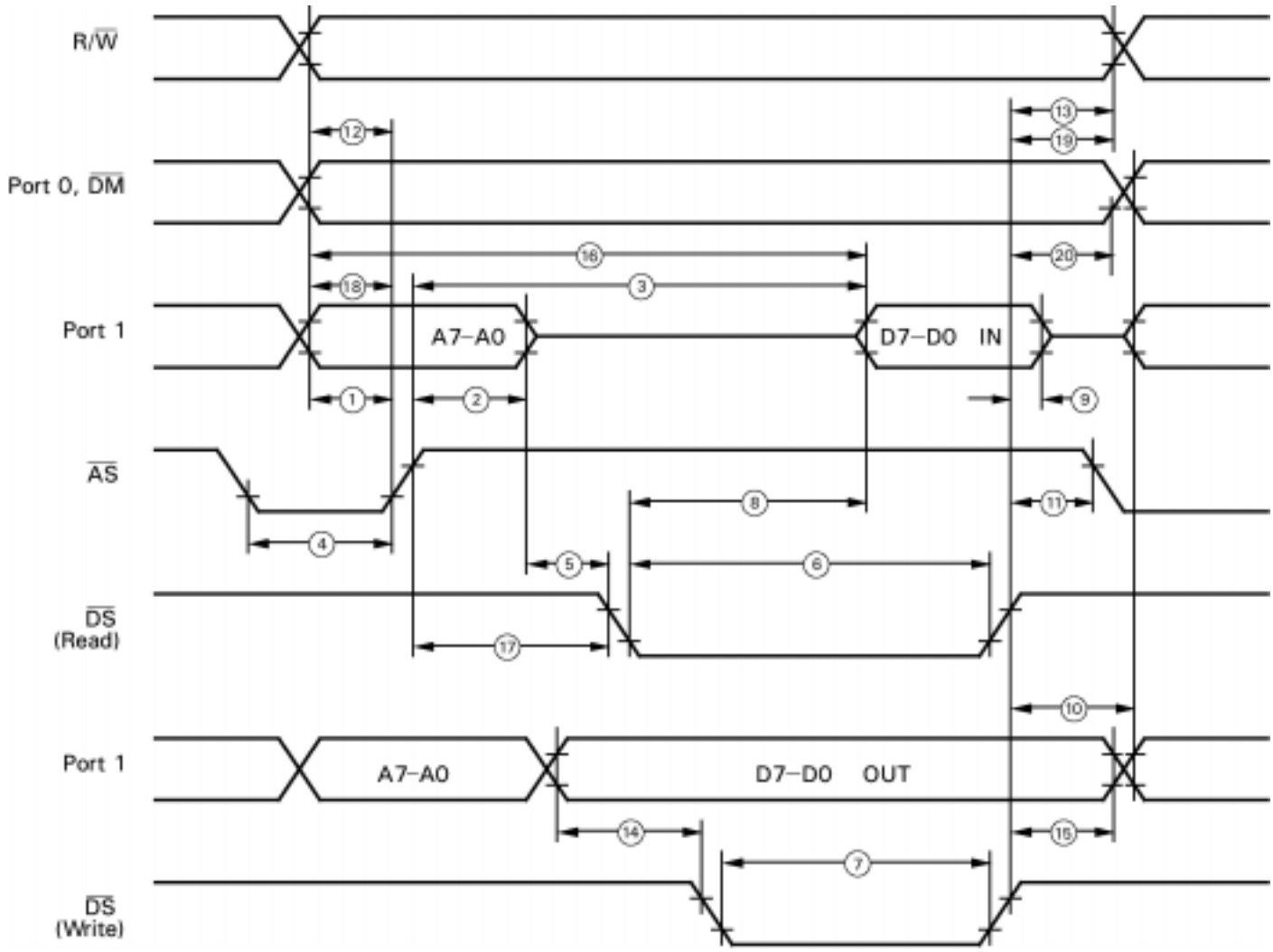

Figure 7. External I/O or Memory Read/Write Timing

Preliminary
External I/O or Memory Read and Write Timing Table

				T_A = 0°C to +70°C 8.0MHz*			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to	2.0V	55		ns	2
		$\overline{AS}$ Rising Delay	3.6V	55		ns	
2	TdAS(A)	$\overline{AS}$ Rising to Address	2.0V	70		ns	2
		Float Delay	3.6V	70		ns	2
3	TdAS(DR)	$\overline{AS}$ Rising to Read	2.0V		400	ns	1,2
		Data Required Valid	3.6V		400	ns	
4	TwAS	$\overline{AS}$ Low Width	2.0V	80		ns	2
			3.6V	80		ns	
5	Td	Address Float to	2.0V	0		ns	
		$\overline{DS}$ Falling	3.6V	0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	2.0V	300		ns	1,2
			3.6V	300		ns	
7	TwDSW	$\overline{DS}$ (Write) Low Width	2.0V	165		ns	1,2
			3.6V	165		ns	
8	TdDSR(DR)	$\overline{DS}$ Falling to Read	2.0V		260	ns	1,2
		Data Required Valid	3.6V		260	ns	
9	ThDR(DS)	Read Data to $\overline{DS}$ Rising	2.0V	0		ns	2
		Hold Time	3.6V	0		ns	
10	TdDS(A)	$\overline{DS}$ Rising to Address	2.0V	85		ns	2
		Active Delay	3.6V	95		ns	
11	TdDS(AS)	$\overline{DS}$ Rising to $\overline{AS}$	2.0V	60		ns	2
		Falling Delay	3.6V	70		ns	
12	TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$	2.0V	70		ns	2
		Rising Delay	3.6V	70		ns	
13	TdDS(R/W)	$\overline{DS}$ Rising to	2.0V	70		ns	2
		R/$\overline{W}$ Not Valid	3.6V	70		ns	
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$	2.0V	80		ns	2
		Falling (Write) Delay	3.6V	80		ns	
15	TdDS(DW)	$\overline{DS}$ Rising to Write	2.0V	70		ns	2
		Data Not Valid Delay	3.6V	80		ns	
16	TdA(DR)	Address Valid to Read	2.0V		475	ns	1,2
		Data Required Valid	3.6V		475	ns	
17	TdAS(DS)	$\overline{AS}$ Rising to	2.0V	100		ns	2
		$\overline{DS}$ Falling Delay	3.6V	100		ns	
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$	2.0V	55		ns	2
		Falling Delay	3.6V	55		ns	
19	TdDS(DM)	$\overline{DS}$ Rise to	2.0V	70		ns	
		$\overline{DM}$ Valid Delay	3.6V	70		ns	
20	ThDS(A)	$\overline{DS}$ Rise to Address	2.0V	70		ns	
		Valid Hold Time	3.6V	70			

Notes:
*Standard Test Load: All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
1. When using extended memory timing add 2 TpC.
2. Timing numbers provided are for minimum TpC.

AC CHARACTERISTICS (Continued)

Additional Timing

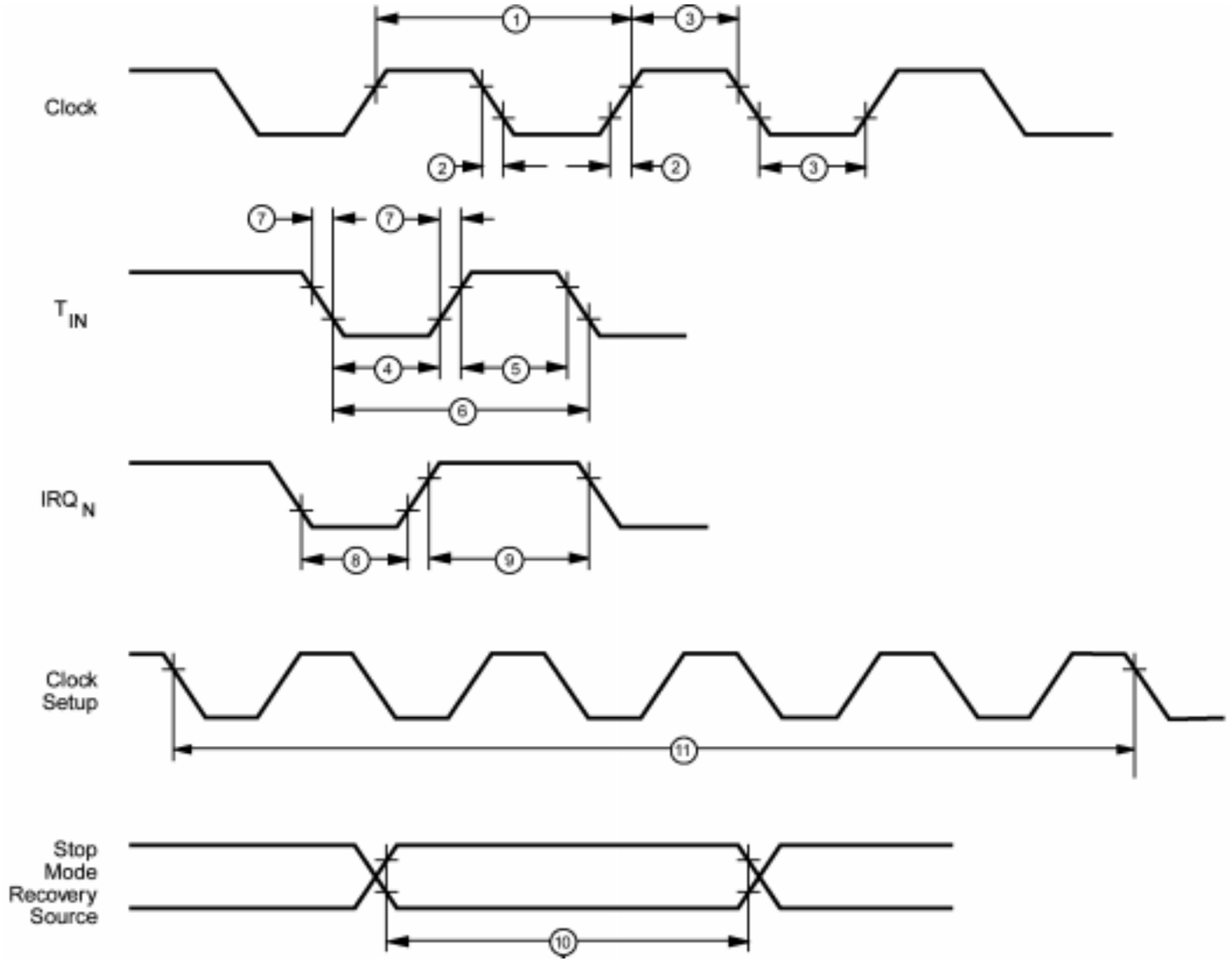

Figure 8. Additional Timing

Table 3. Additional Timing

No	Sym	Parameter	T_A = 0°C to +70°C 8.0 MHz V_{CC}	Min	Max	Units	Notes	Stop-Mode Recovery (D1,D0)
1	TpC	Input Clock Period	2.0V	121	DC	ns	1	
			3.6V	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	1	
			3.6V		25	ns	1	
3	TwC	Input Clock Width	2.0V	37		ns	1	
			3.6V	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0V	100		ns	1	
			3.6V	70		ns	1	
5	TwTinH	Timer Input High Width	2.0V	3TpC			1	
			3.6V	3TpC			1	
6	TpTin	Timer Input Period	2.0V	8TpC			1	
			3.6V	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0V		100	ns	1	
			3.6V		100	ns	1	
8A	TwIL	Interrupt Request Low Time	2.0V	100		ns	1,2	
			3.6V	70		ns	1,2	
8B	TwIL	Interrupt Request Low Time	2.0V	5TpC			1,3	
			3.6V	5TpC			1,3	
9	TwIH	Interrupt Request Input High Time	2.0V	5TpC			1,2	
			3.6V	5TpC			1,2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0V	12		ns		
			3.6V	12		ns		
11	Tost	Oscillator Start-Up Time	2.0V		5TpC		4	
			3.6V		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time						
			2.0V	12		ms	5	0, 0
			3.6V	5		ms	5	
			2.0V	25		ms	5	0, 1
			3.6V	10		ms	5	
			2.0V	50		ms	5	1, 0
			3.6V	20		ms	5	
			2.0V	225		ms	5	1, 1
			3.6V	80		ms	5	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0.
5. For internal RC oscillator.

PIN DESCRIPTION

$\overline{DS}$ (Output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of $\overline{DS}$. For WRITE operations, the falling edge of $\overline{DS}$ indicates that output data is valid.

$\overline{AS}$ (Output, active Low). Address Strobe is pulsed one time at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coed to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R/$\overline{W}$ Read/Write (output, write Low). The R/$\overline{W}$ signal is Low when the CCP is writing to the external program or data memory.

R/$\overline{RL}$ (input). This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

Note: When left unconnected or pulled High to V_{CC}, the part functions normally as a Z8 ROM version.

Port 0 (P07–P00). Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble), depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are necessary for I/O operation, they must be configured by writing to the Port 0 Mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode (if selected as an address output), along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$ through P3M bits D4 and D3 (Figure 9).

A ROM mask option is available to program 0.4 V_{DD} CMOS trip inputs on P00–P03. This option allows direct interface to mouse/trackball IR sensors.

An optional 200 ±50% KΩ pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

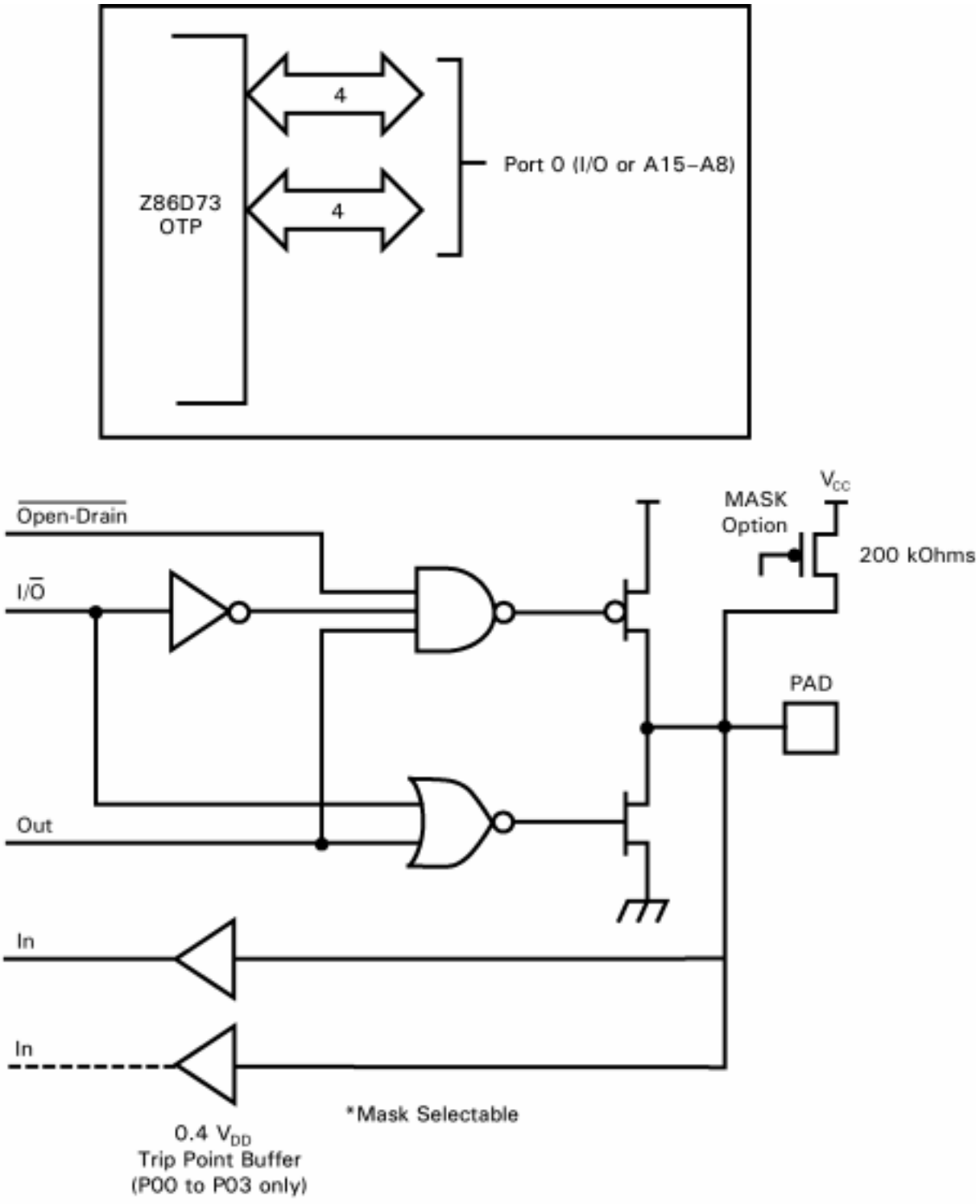

Figure 9. Port 0 Configuration

PIN DESCRIPTION (Continued)

Port 1 (P17–P10). Port 1 is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe ($\overline{AS}$) and Data Strobe ($\overline{DS}$) lines, and by the Read/Write (R/$\overline{W}$) and Data Memory ($\overline{DM}$) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$, and R/$\overline{W}$, allowing the Z86D73 to share common resources in multiprocessor and DMA applications. Port1 can also be configured for standard port output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain, and are controlled by bit D1 in the PCON register.

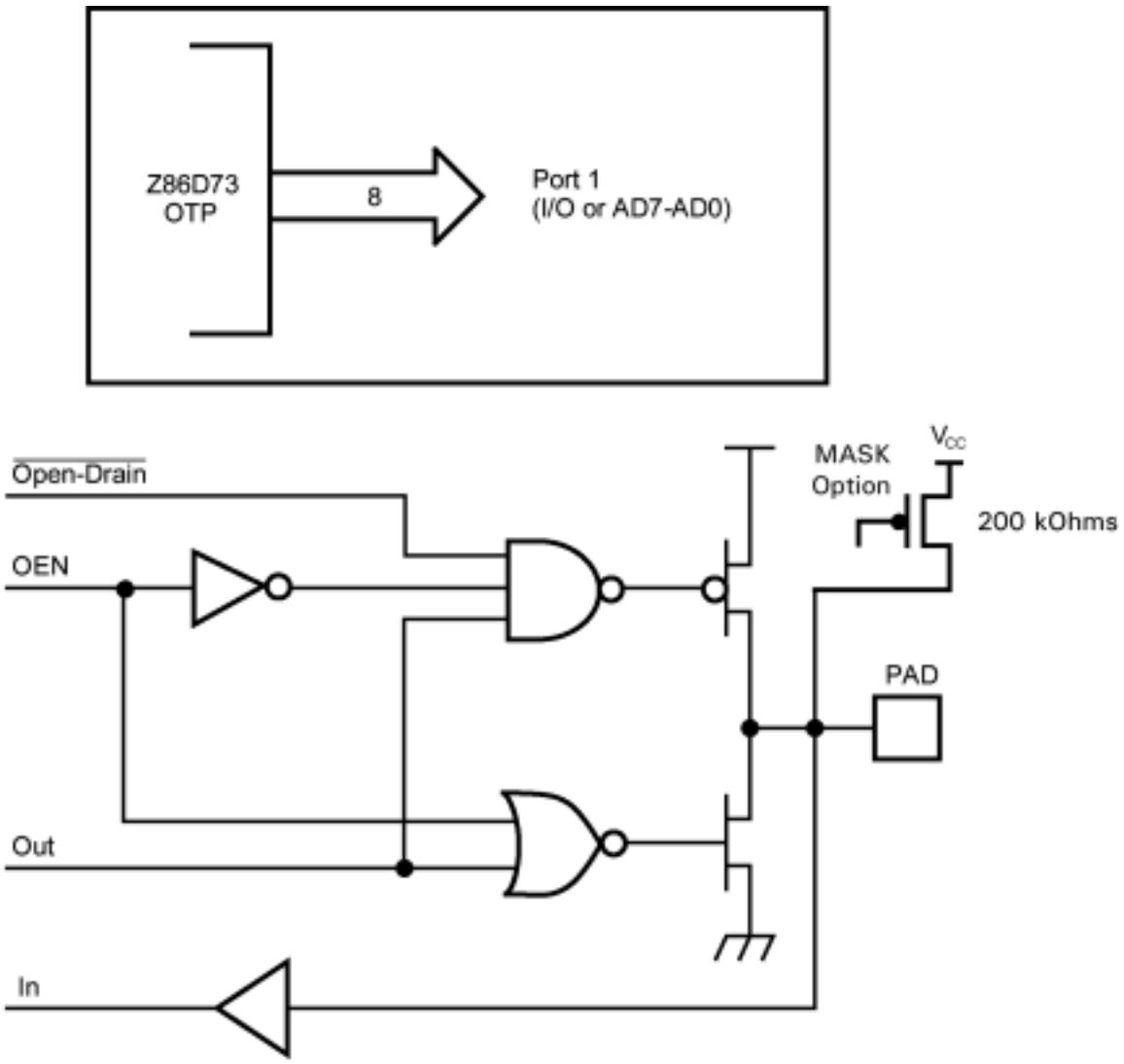

Figure 10. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 KΩ (±50%) pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge detection circuitry in demodulation mode.

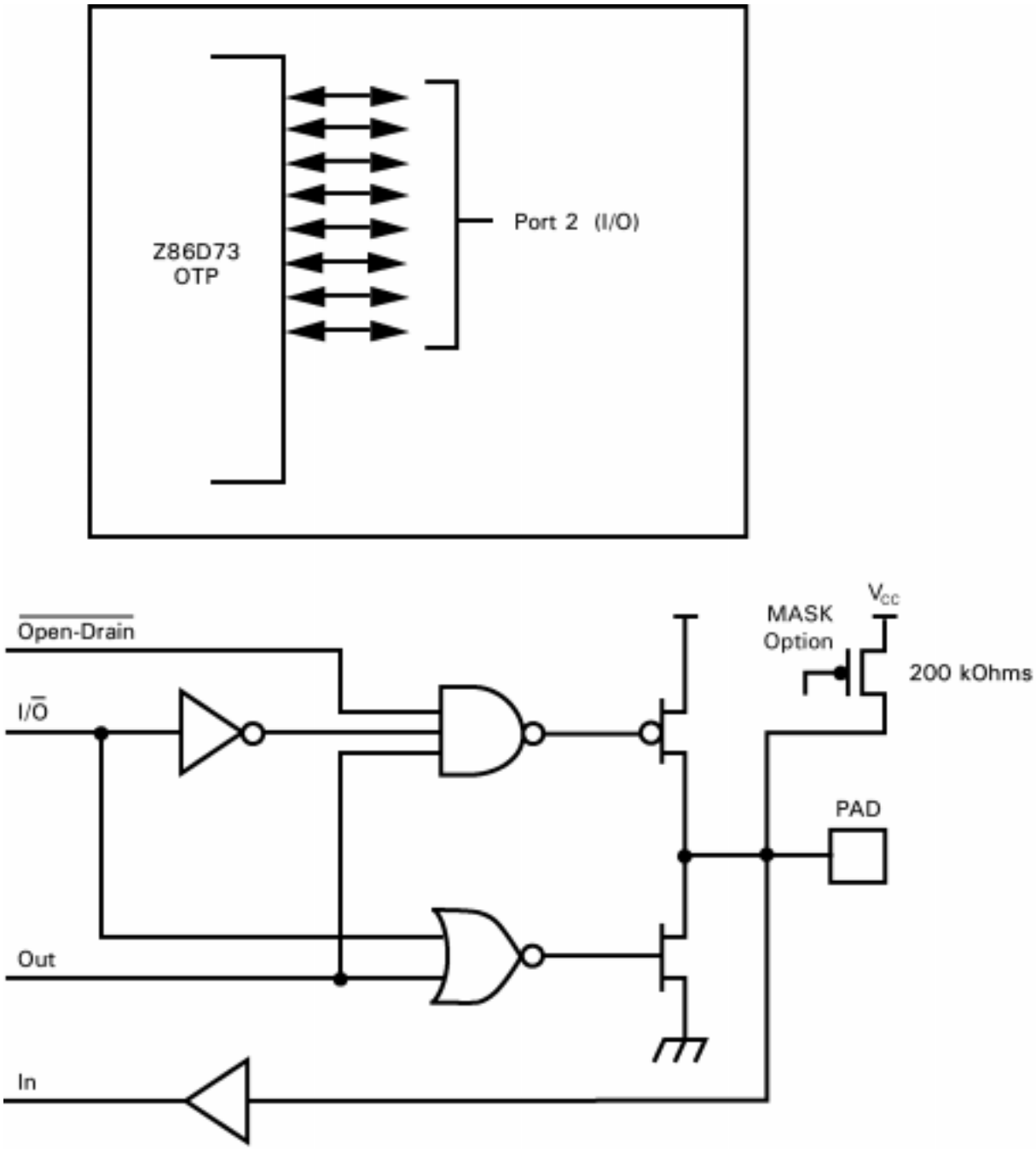

Figure 11. Port 2 Configuration

PIN DESCRIPTION (Continued)

Port 3 (P37–P31). Port 3 is a 7-bit, CMOS-compatible I/O port. Port 3 consists of three fixed inputs (P33–P31) and four fixed outputs (P37–P34), which can be configured under software control for interrupt, and as output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; P34, P35, P36 and P37 are push-pull outputs.

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge detection circuit is through P31 or P20 (see CTR1 description). Other edge detect and IRQ modes are described in Table 4.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

Comparator Inputs. In Analog Mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12. In digital mode, P33 is used as D3 of the Port 3 input register which then generates IRQ1.

Table 4. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Comparator Outputs. These channels may be programmed to be outputted on P34 and P37 through the PCON register.

$\overline{\text{RESET}}$ (Input, active Low). Reset initializes the MCU, and is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line should be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

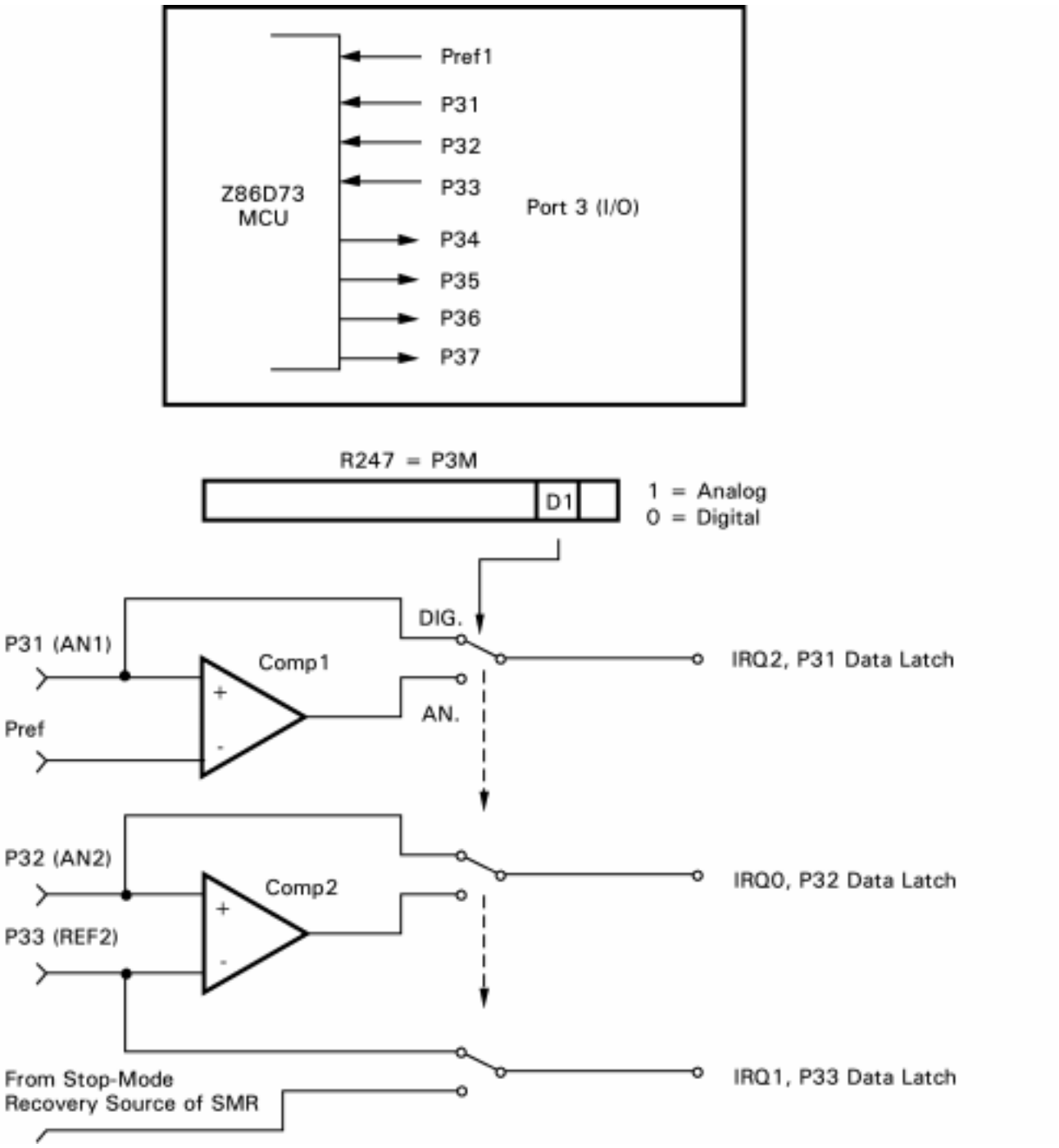

Figure 12. Port 3 Configuration

PIN DESCRIPTION (Continued)

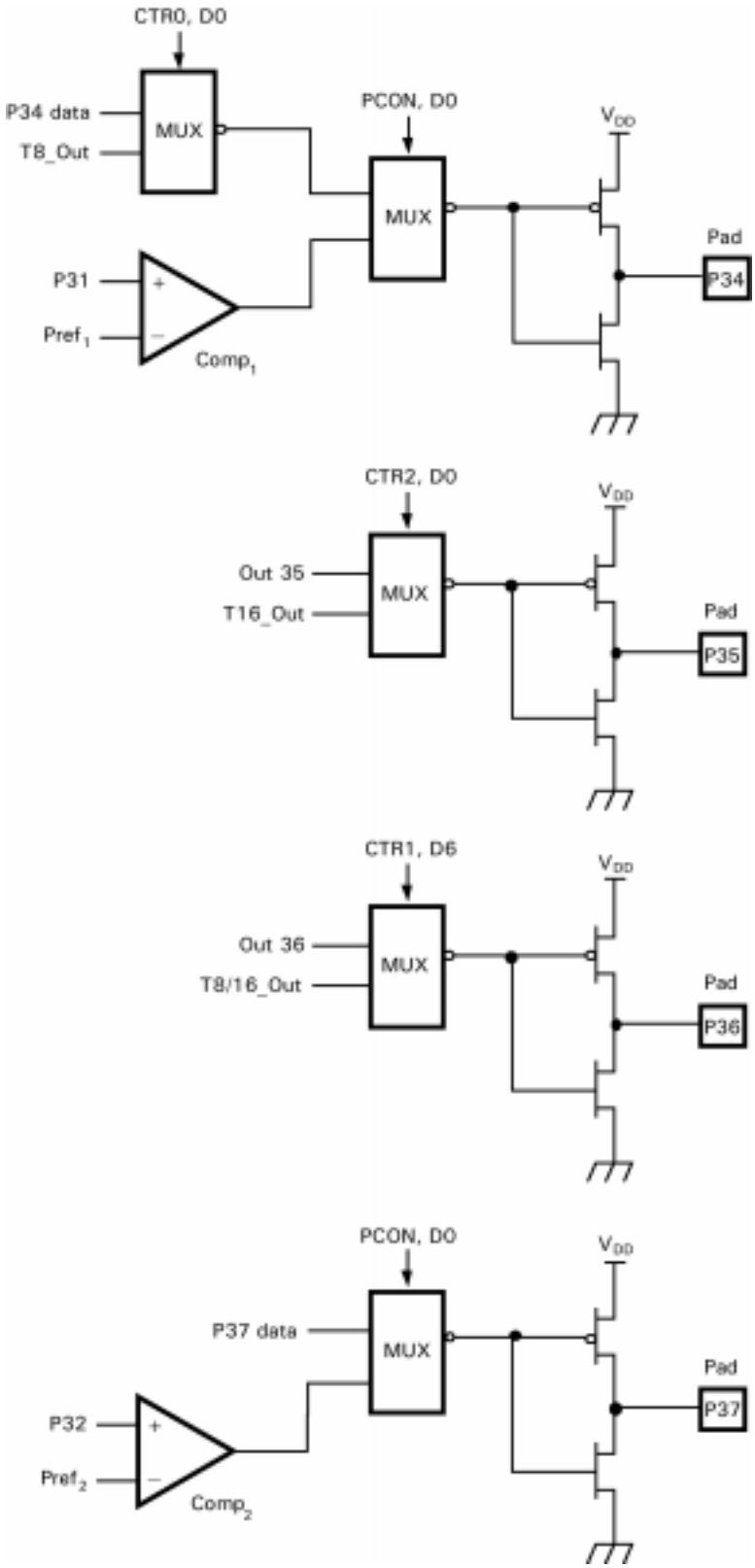

Figure 13. Port 3 Counter Timer Output Configuration

FUNCTIONAL DESCRIPTION

The Z86D73 incorporate special functions to enhance the Z8's functionality in consumer and battery operated applications.

Program Memory. The Z86D73 addresses 32 KB of OTP memory. The first twelve bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors which correspond to the five available interrupts.

RAM. The Z86D73 device features 256 bytes of RAM.

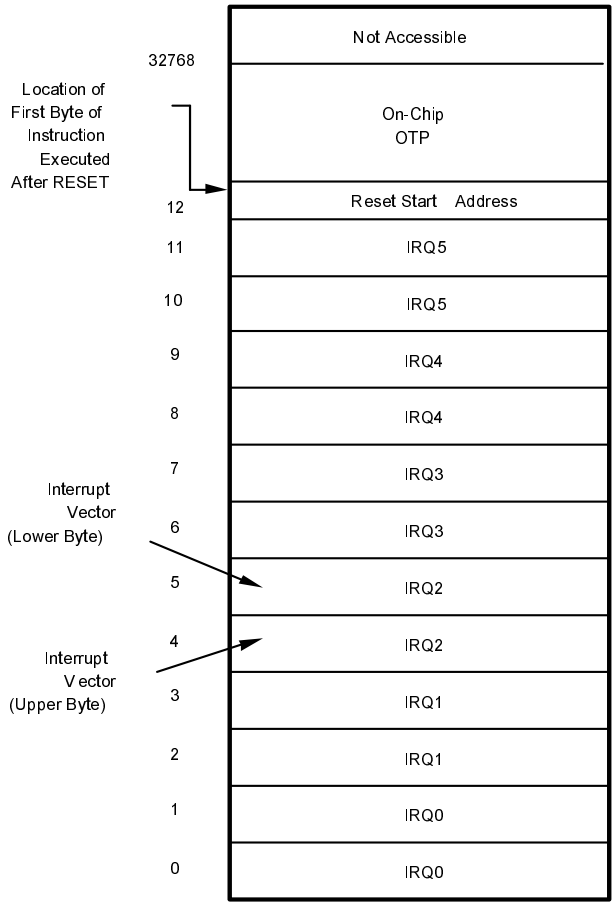

Figure 14. Program Memory Map (32K OTP)

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices into the register address area. The Z8 register address space (R0 through R15) has been implemented as 16 banks with 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

Note: An expanded register bank is also referred to as an expanded register group (see Figure 15).

The upper nibble of the register pointer (Figure 16) selects which working register group, of 16 bytes in the register file, will be accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z86D73 family, banks 0, F, and D are implemented. A 0h in the lower nibble will allow the normal register file (bank 0) to be addressed. Any other value from 1h to Fh will exchange the lower 16 registers to an expanded register bank.

Example: Z86D73: (See Figure 15)

```
R253 RP = 00h
     R0 = Port 0
     R1 = Port 1
     R2 = Port 2
     R3 = Port 3

But if:

R253 RP = 0Dh
     R0 = CTRL0
     R1 = CTRL1
     R2 = CTRL2
     R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily performed using the following:

Example:

```
LD   RP, #0Dh          ; Select ERF D for access
to bank D (working register group 0)
LD   R0,#xx            ; load CTRL0
LD   1, #xx            ; load CTRL1
LD   R1, 2             ; CTRL2→CTRL1

LD   RP, #0Dh          ; Select ERF D for access
to bank D (working register group 0)
LD   RP, #7Dh          ; Select expanded register
bank D and working register group 7 of bank 0 for
access.
LD   71h, 2            ; CTRL2→register 71h
LD   R1, 2             ; CTRL2→register 71h
```

FUNCTIONAL DESCRIPTION (Continued)

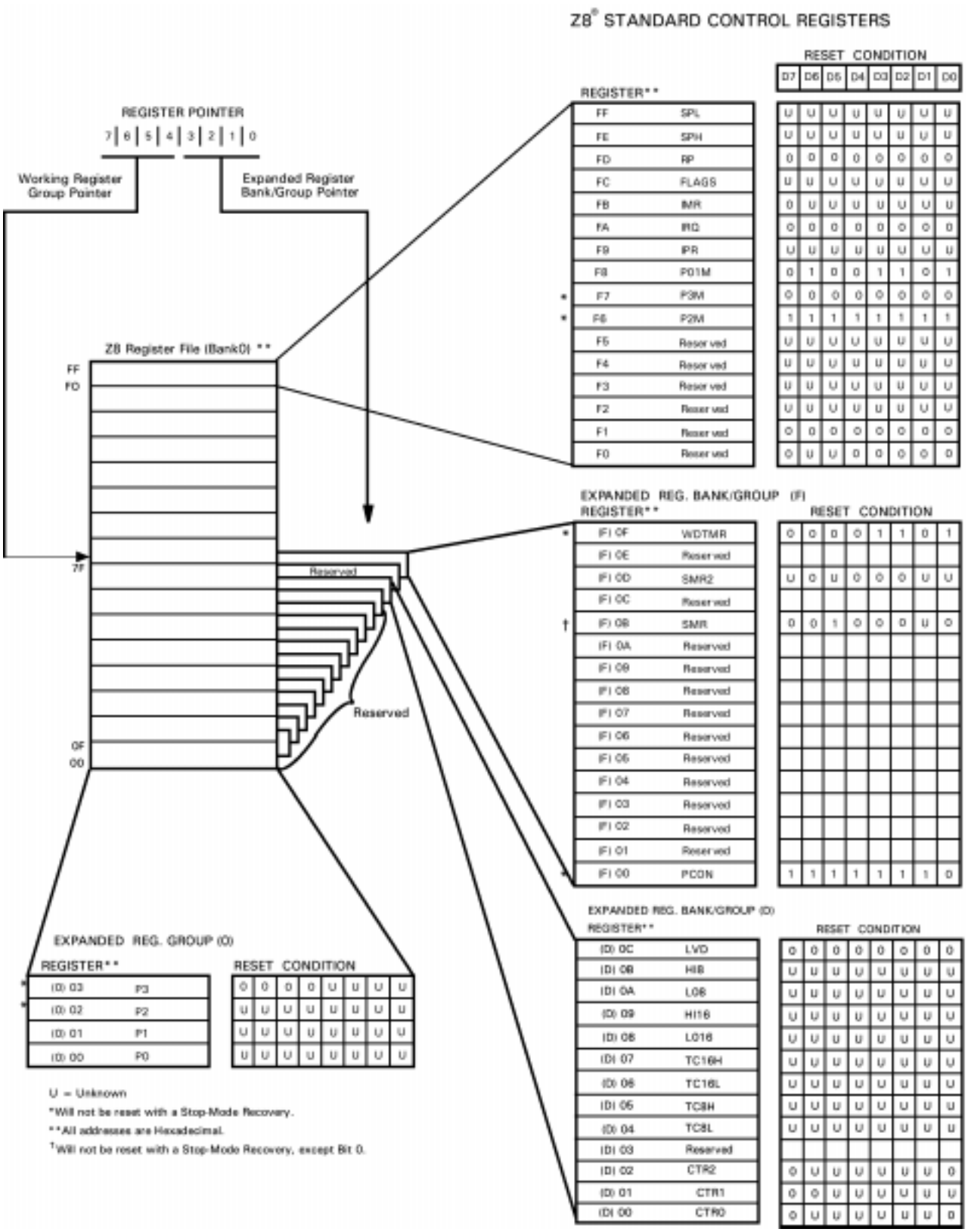

Figure 15. Expanded Register File Architecture

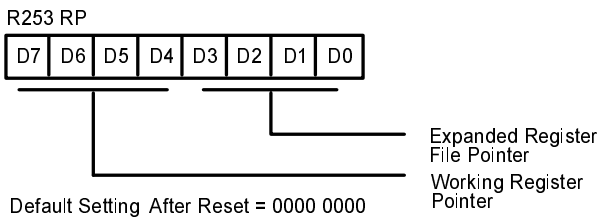

Figure 16. Register Pointer

Register File. The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Working register group E0–EF can only be accessed through working registers and indirect addressing modes.

Stack. The Z86D73 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed.

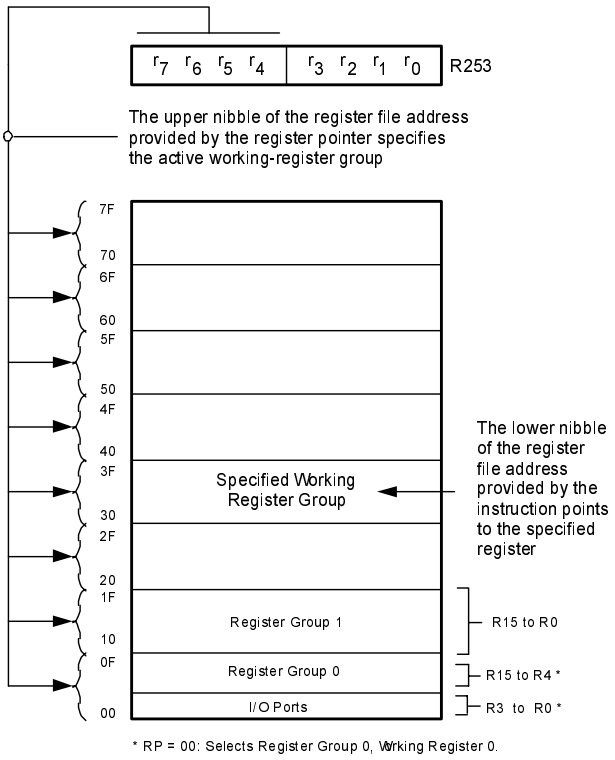

Figure 17. Register Pointer—Detail

FUNCTIONAL DESCRIPTION (Continued)

Counter/Timer Register Description

Table 5. Expanded Register Group D

(D)%0C	Reserved
(D)%0B	HI8
(D)%0A	LO8
(D)%09	HI16
(D)%08	LO16
(D)%07	TC16H
(D)%06	TC16L
(D)%05	TC8H
(D)%04	TC8L
(D)%03	Reserved
(D)%02	CTR2
(D)%01	CTR1
(D)%00	CTR0

Register Description

LVD(D)%0C. Low Voltage Detection Register.

Field	Bit Position			Description
LVD	765432--			Reserved No Effect
	------1-	R	I	LV flag set
	-------0		O*	LV flag reset
		R/W	I	Enable LVD
			O*	Disable LVD

Note: Default after POR.

HI8(D)%0B. This register holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	76543210	R	Captured Data
		W	No Effect

L08(D)%0A. This register holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	76543210	R	Captured Data
		W	No Effect

HI16(D)%09. This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	76543210	R	Captured Data
		W	No Effect

L016(D)%08. This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	76543210	R	Captured Data
		W	No Effect

TC16H(D)%07. Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)%06. Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)%05. Counter/Timer8 High Hold Register.

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)%04. Counter/Timer8 Low Hold Register.

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

Table 6. CTR0 (D)00 Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:
*Indicates the value upon Power-On Reset.

CTR0 Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set (written) to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location.

Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.

The first clock of T8 may not have complete clock width and can occur anytime when enabled.

Note: Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be ORed or ANDed with the designated value and then written back into the registers.

Example: When the status of bit 5 is 1, a timer reset condition will occur.

T8 Clock. This bit defines the frequency of the input signal to T8.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask. Set this bit to allow an interrupt when T8 has a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

FUNCTIONAL DESCRIPTION (Continued)

CTR1(D)%01. .Controls the functions in common with the T8 and T16.

Table 7. CTR1(D)%01 T8 & T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode Demodulation Mode
P36_Out/Demodulator _Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/ Edge _Detect	--54----	R/W		Transmit Mode
			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/ Glitch_Filter	----32--	R/W		Transmit Mode
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

CTR1 Register Description

Mode. If the result is 0, the Counter/Timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input. In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In Transmit Mode, this field defines whether T8 and T16 are in the "Ping-Pong" mode or in independent normal operation mode. Setting this field to "Normal Operation Mode" terminates the "Ping-Pong Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When The counter is not enabled and this bit is set to 1 or 0, T8_OUT will be set to the opposite state of this bit. This ensures that when the clock is enabled a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit Mode, if the bit is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT will be set to the opposite state of this bit. This ensures that when the clock is enabled a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1, (D1 or D0) while the counters are enabled will cause unpredictable output from T8/16_OUT.

FUNCTIONAL DESCRIPTION (Continued)

Table 8. CTR2(D)%02: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out
		W	0	Occurred
			1	No Effect
				Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
				Enable Time-Out Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note:
*Indicates the value upon Power-On Reset.

CTR2 Counter/Timer 16 Control Register Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In Transmit Mode, when set to 0, the counter reloads the initial value when the terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 36.

Time_Out. This bit is set when T16 times out (terminal count reached). In order to reset the bit, a 1 should be written to this location.

T16_Clock. This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Set this bit to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow an interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

Table 9. SMR2(F)%0D: Stop-Mode Recovery Register 2*

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0† 1	Low High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000† 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND or P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
*Port pins configured as outputs are ignored as a SMR recovery source.
†Indicates the value upon Power-On Reset.

Counter/Timer Functional Blocks

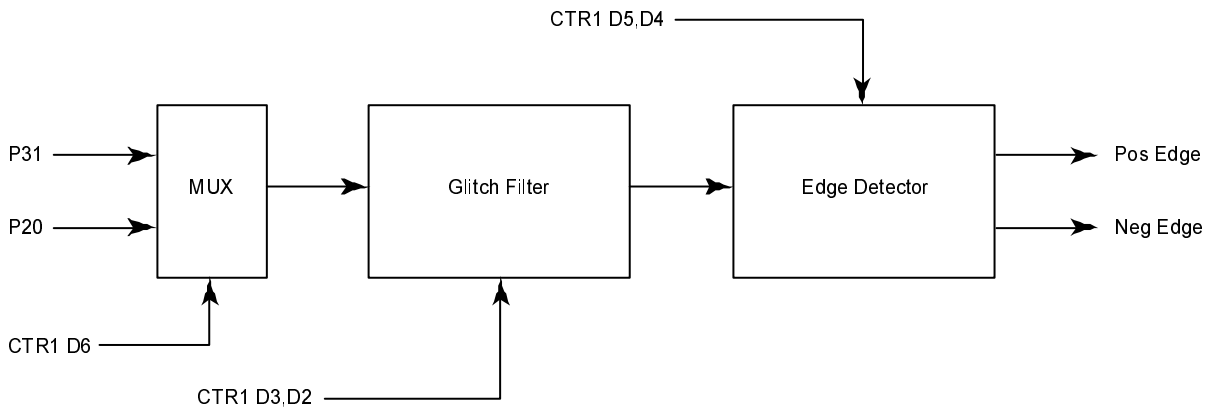

Figure 18. Glitch Filter Circuitry

FUNCTIONAL DESCRIPTION (Continued)

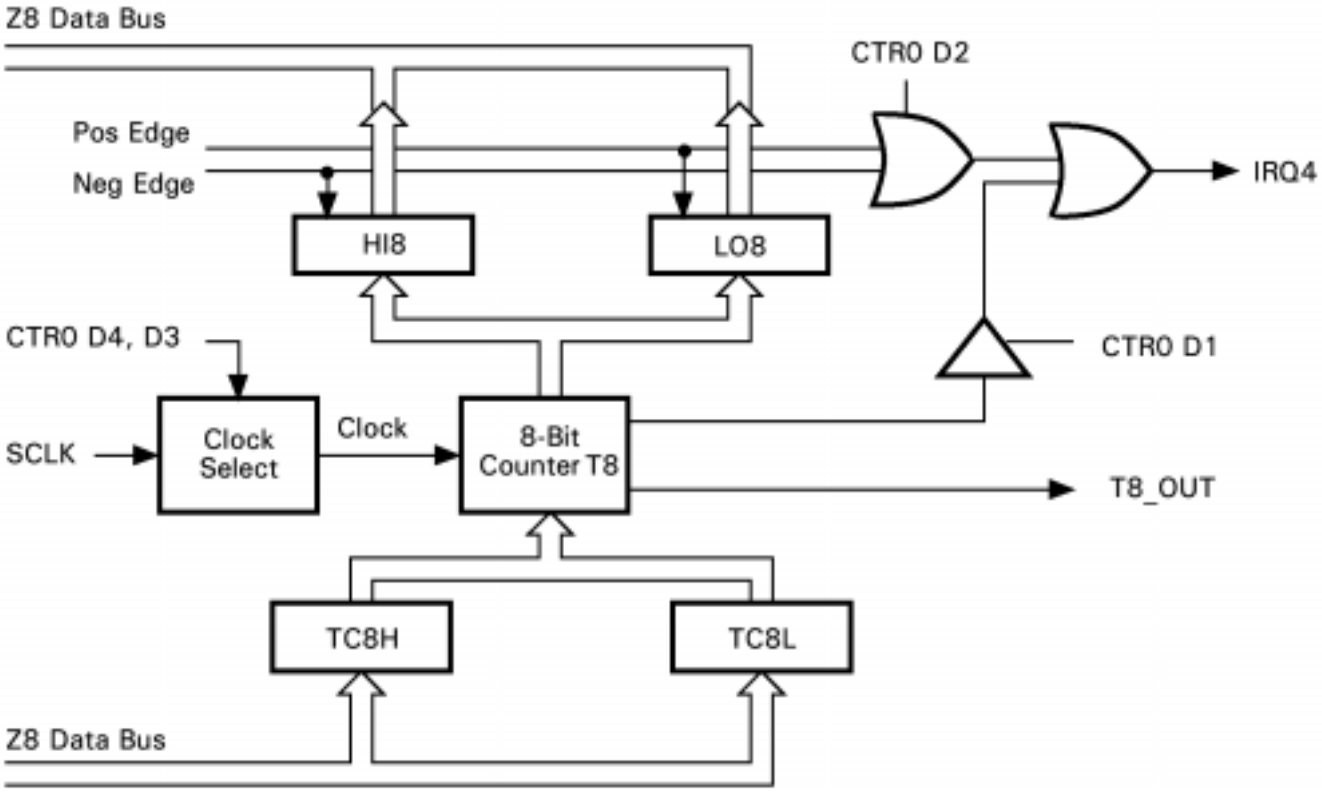

Figure 19. 8-Bit Counter/Timer Circuits

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In Single-Pass Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0). TC8L is then loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. *An initial count of 1 is not allowed (a non-function will occur).* An initial count of 0 will cause TC8 to count from 0 to %FF to %FE.

Note: % is used for hexadecimal values.

Transition from 0 to %FF is not a time-out condition.

Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur.

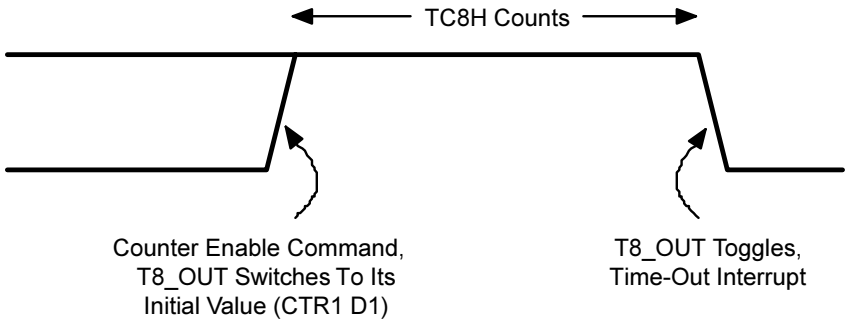

Figure 20. T8_OUT in Single-Pass Mode

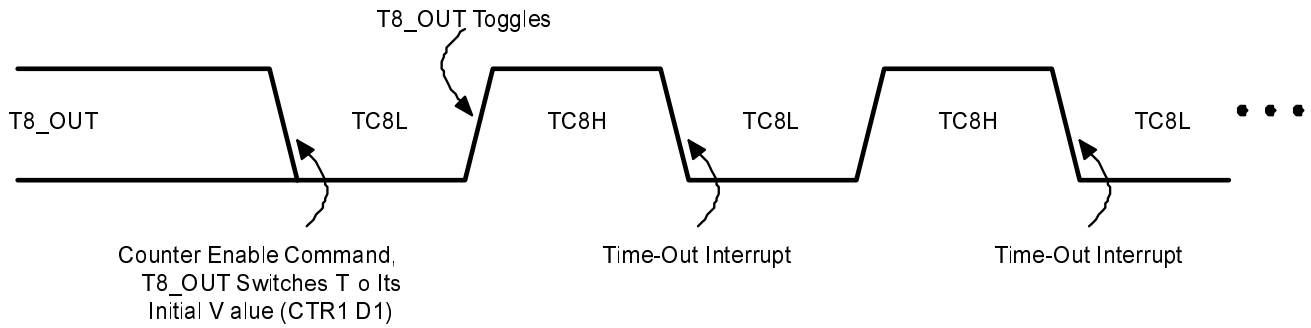

Figure 21. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if a negative edge, HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from %FF (Figure 22).

FUNCTIONAL DESCRIPTION (Continued)

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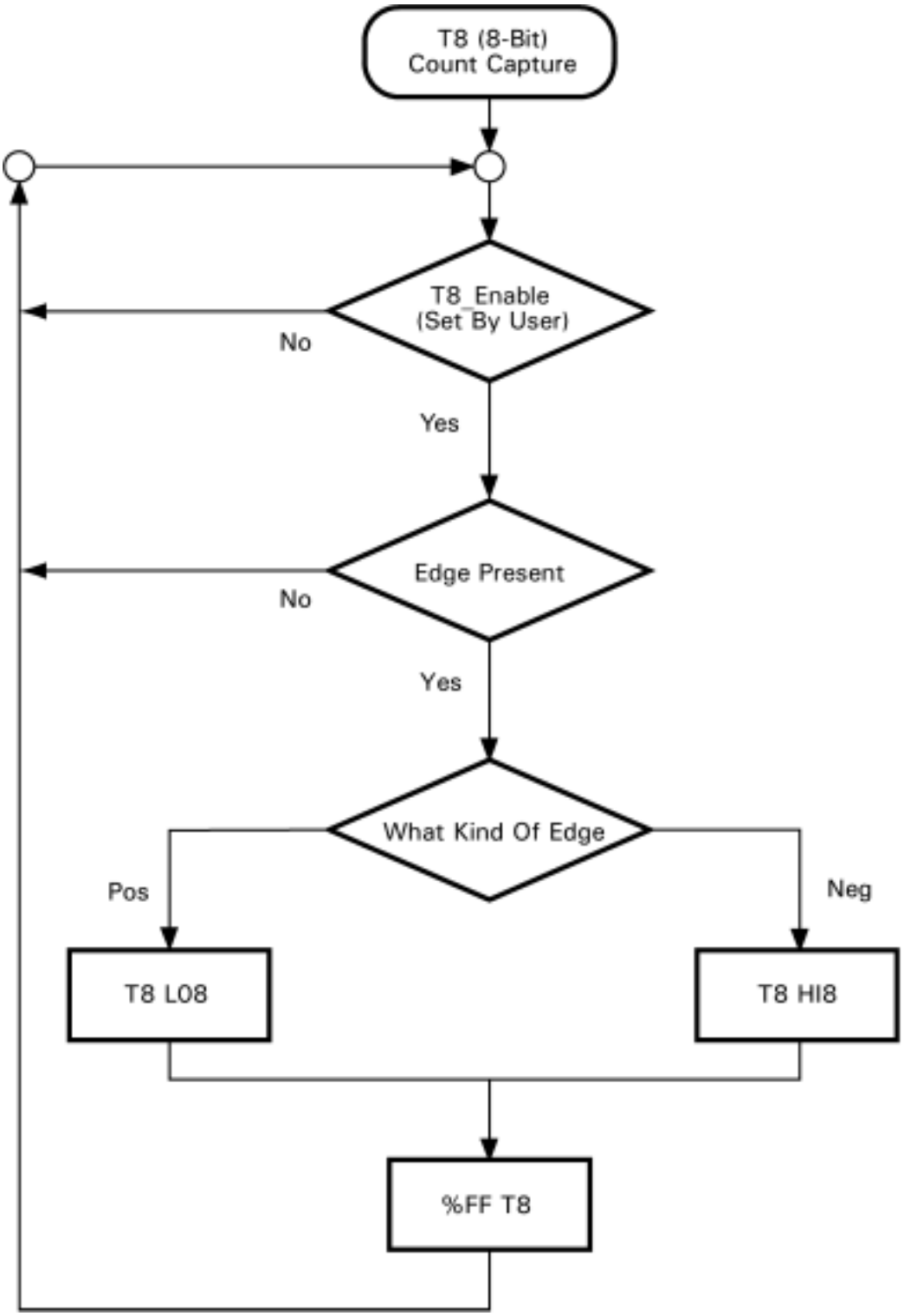


Figure 22. Demodulation Mode Count Capture Flowchart

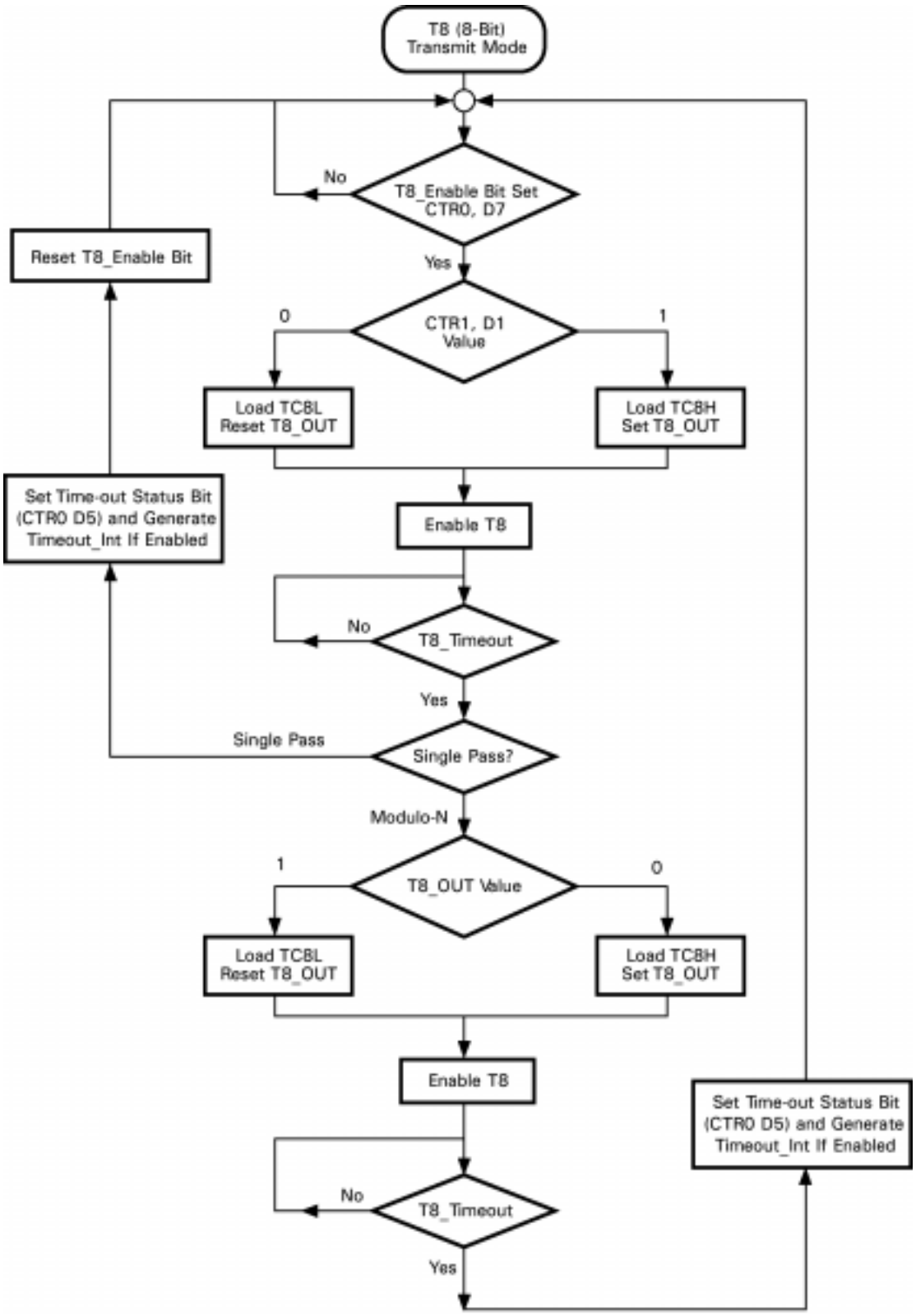


Figure 23. Transmit Mode Flowchart

FUNCTIONAL DESCRIPTION (Continued)

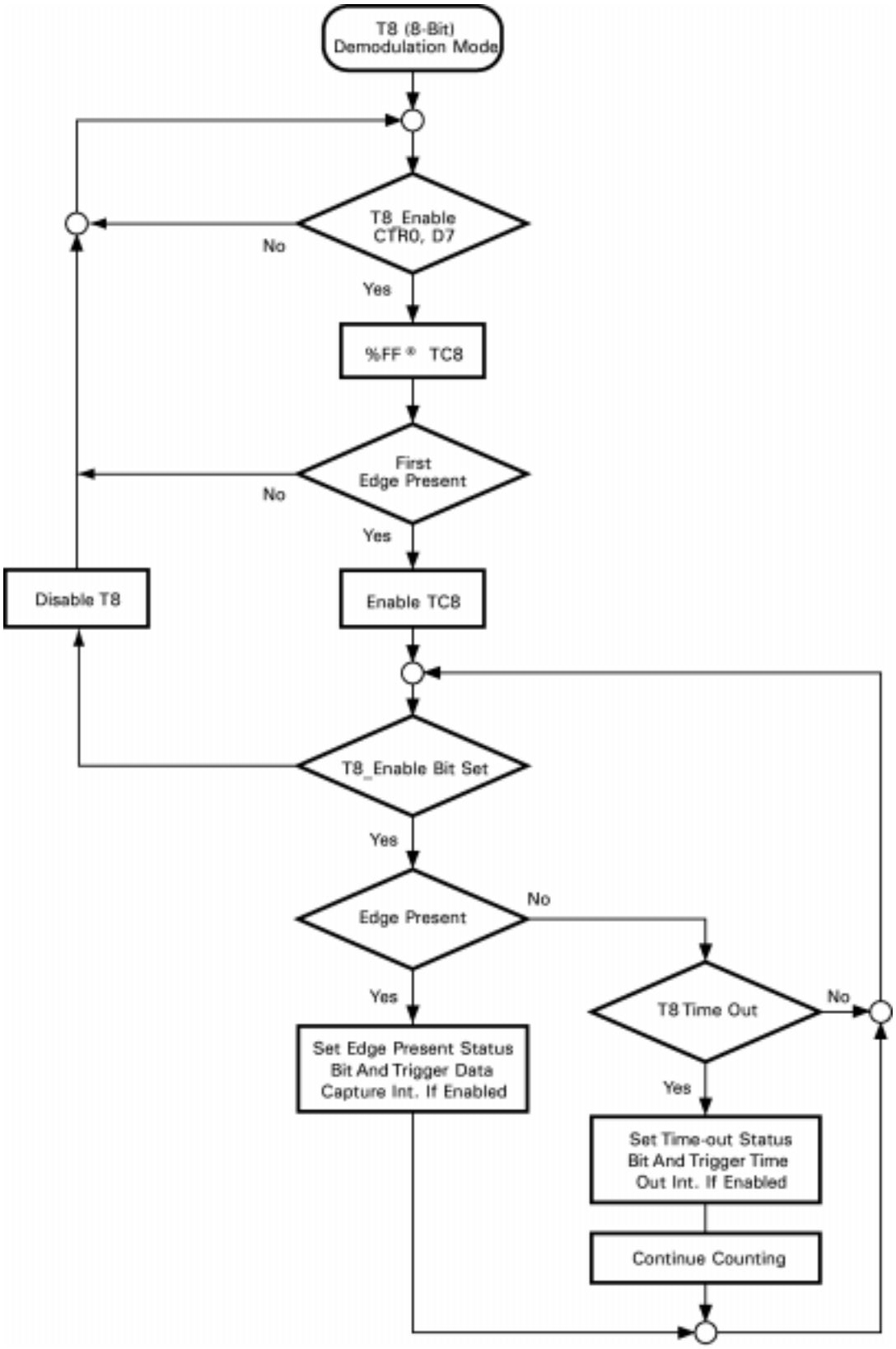


Figure 24. Demodulation Mode Flowchart

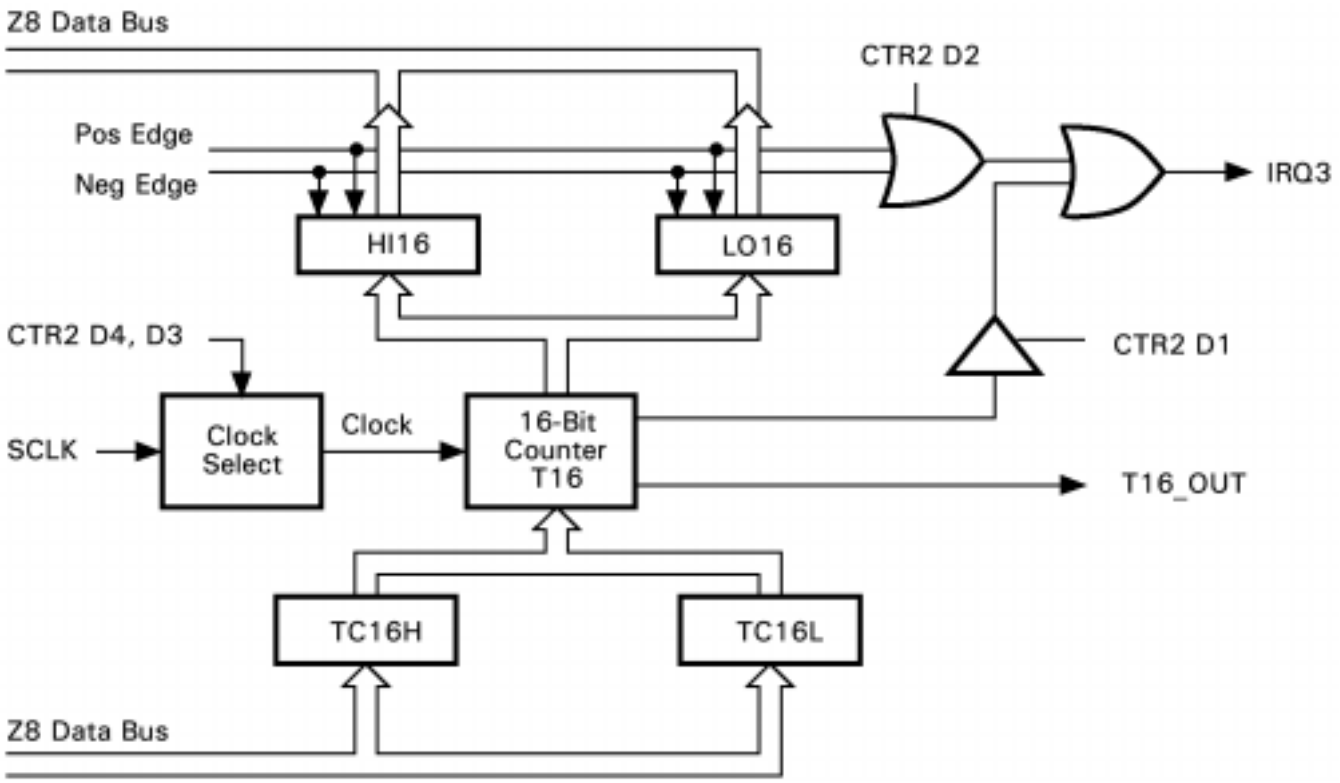


Figure 25. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 (when not enabled) is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1, D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt (CTR2, D1) is generated if enabled, and a status bit (CTR2, D5) is set.

Note: Global interrupts will override this function as described in the Interrupts section, page 38.

If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 will cause T16 to count from 0 to %FFFF to %FFFE. Transition from 0 to %FFFF is not a time-out condition.

FUNCTIONAL DESCRIPTION (Continued)

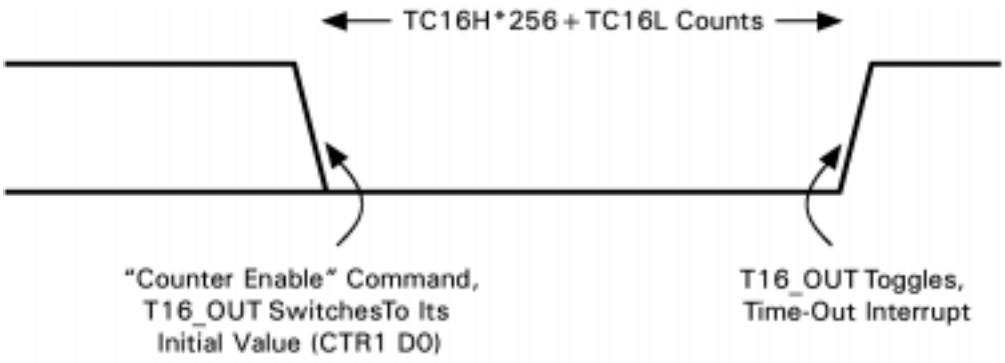


Figure 26. T16_OUT in Single-Pass Mode

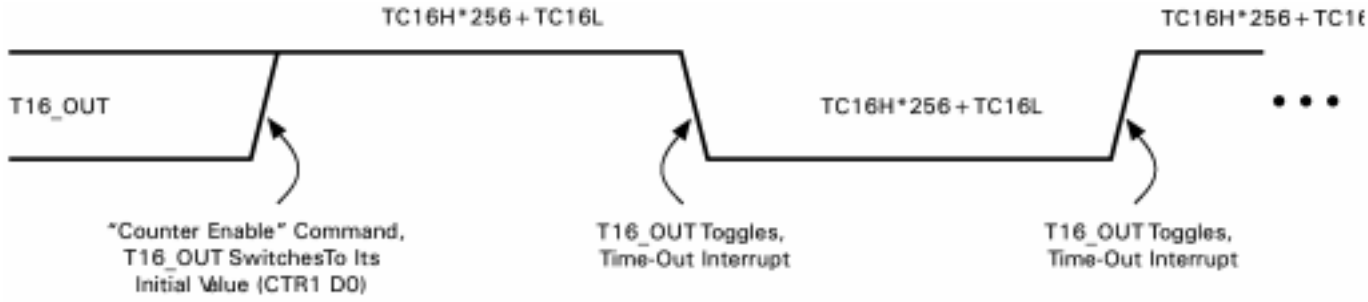


Figure 27. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 is 0. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with %FFFF and starts again.

This T16 mode is generally used to measure space time; the length of time between bursts of carrier signal (marks).

If D6 of CTR2 is 1. T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) continuing to ignore subsequent edges.

This T16 mode is generally used to measure mark times; the length of an active carrier signal bursts.

Should T16 reach 0, it continues counting from %FFFF. Meanwhile, a status bit (CTR2, D5) is set, and an interrupt time-out can be generated if enabled (CTR2, D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 must be programmed in Single-Pass Mode (CTR0, D6; CTR2, D6) and Ping-Pong Mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR,2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is

loaded, and T16 starts to count. After T16 reaches the terminal count it stops. T8 is again enabled, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. Disable the counter/timers, then reset the status flags prior to instituting this operation.

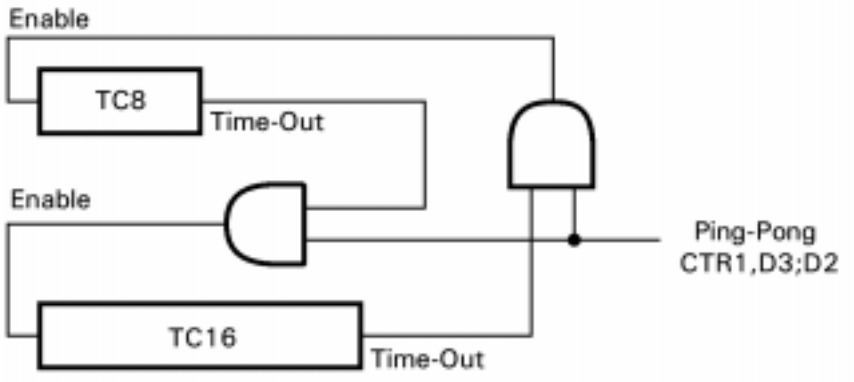


Figure 28. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass Mode (CTR,0 D6), set T16 into Single-Pass Mode (CTR2, D6), and set Ping-Pong Mode (CTR1, D2; D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2, D7).

The initial value of T8 or T16 must not be "1". If the timer is stopped by the user and started again, the user must reload the initial value to avoid an unknown previous value.

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) will be set and cleared alternately by hardware. The time-out bits (CTR0, D5; CTR2, D5) will be set every time the counter/timers reach the terminal count.

FUNCTIONAL DESCRIPTION (Continued)

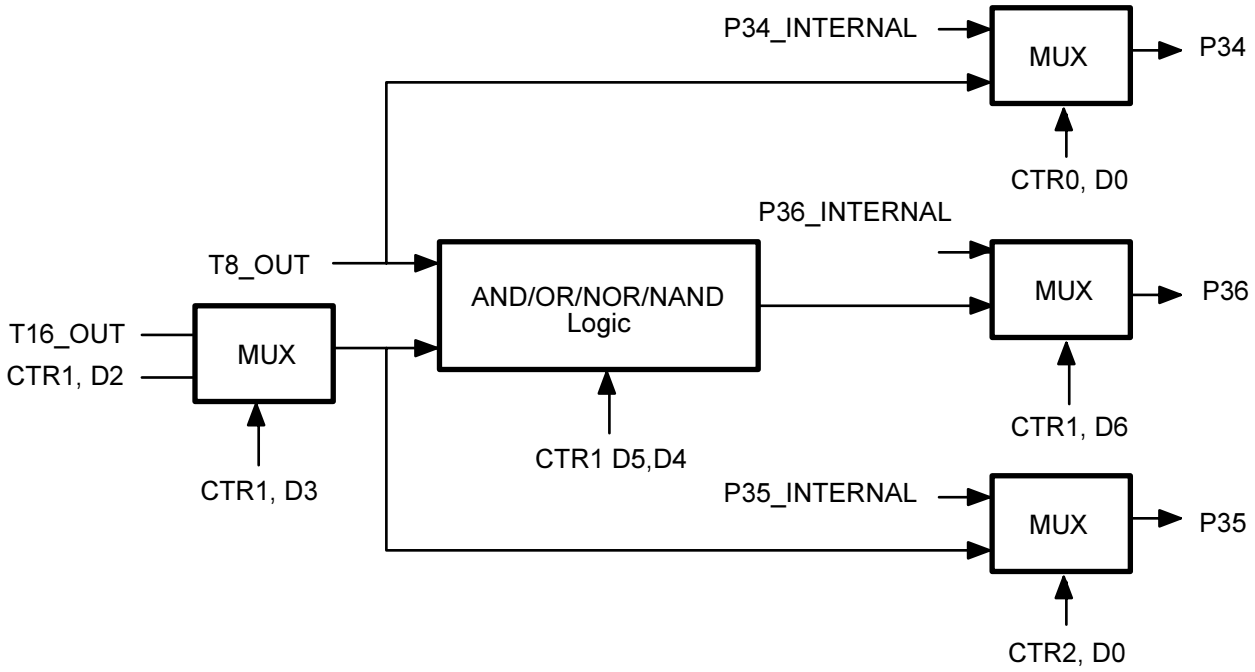


Figure 29. Output Circuit

Interrupts. The Z86D73 feature five different interrupts. The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, and two by the counter/timers (Table 8). The Interrupt Mask Register (globally or individually) enables or disables the five interrupt requests.

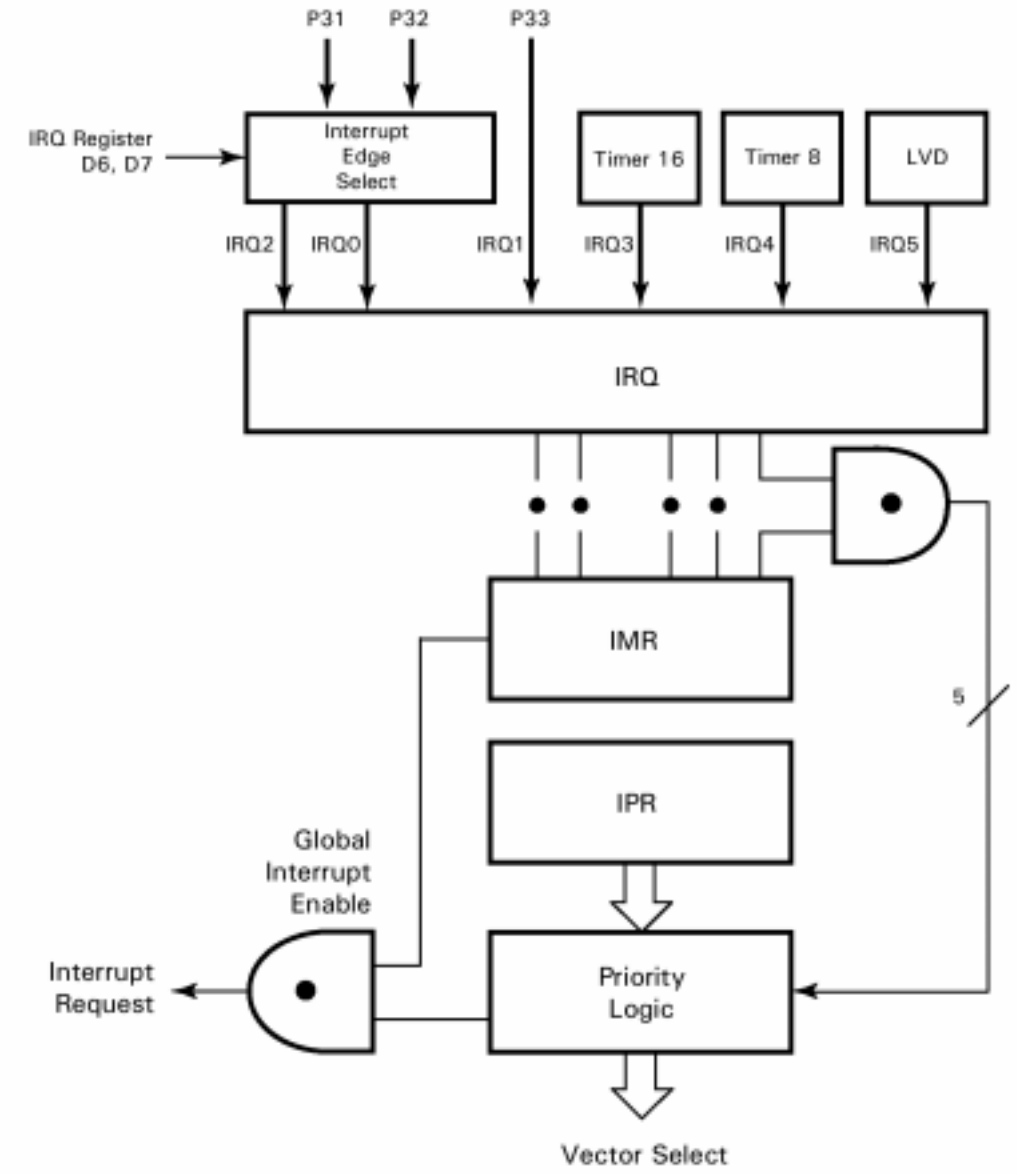


Figure 30. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Table 10. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86D73 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 11.

Table 11. IRQ Register*

IRQ		Interrupt Edge	
D7	D6	IRQ2(P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
*In Stop Mode, the comparators are turned off.

Clock. The Z86D73 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100Ω. The Z86LXX on-chip oscillator may be driven with a low-cost RC network or other suitable external clock source.

For 32 kHz crystal operation, an external feedback resistor (Rf) and a serial resistor (Rd) are required. See Figure 31.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 31).

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status, including Waking up from (V_{BO} Standby).
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC and LC oscillators).

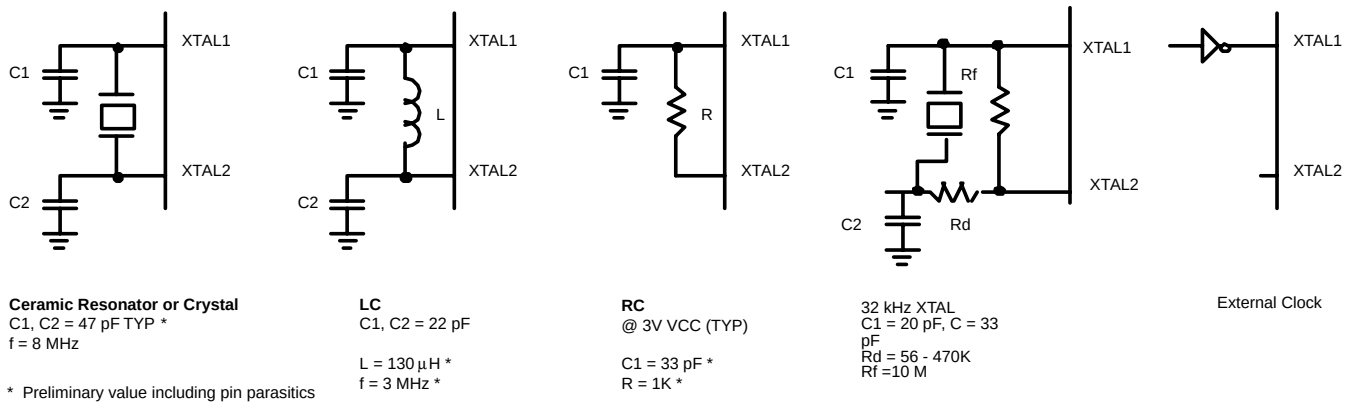


Figure 31. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation, thereby reducing the standby current to 10 µA or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This condition causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. The user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```
Example: FF    NOP     ; clear the pipeline
         6F    STOP    ; enter STOP Mode
         or
         FF    NOP     ; clear the pipeline
         7F    HALT    ; enter HALT Mode
```

FUNCTIONAL DESCRIPTION (Continued)

Port Configuration Register (PCON). The PCON register configures the comparator output on Port 3. The register is located in the expanded register 2 at Bank F, location 00.

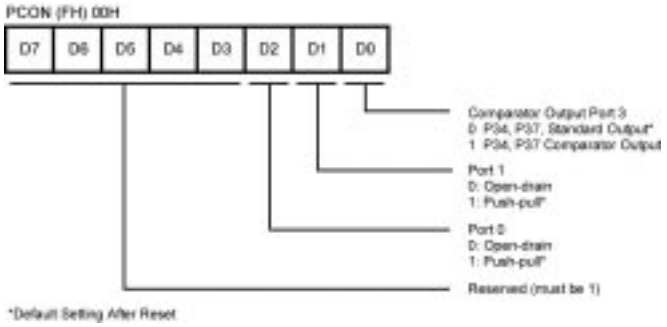


Figure 32. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, while a 0 releases the Port to its standard I/O configuration.

Port0 Output mode (D2). Bit 2 controls the output mode of port 0. A 1 in this location set the output to push-pull, while a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 33). All bits are Write Only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

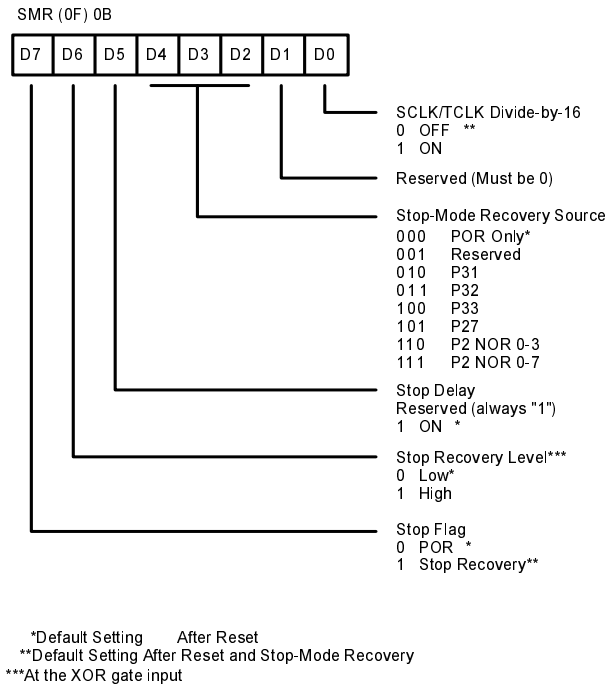


Figure 33. Stop-Mode Recovery Register

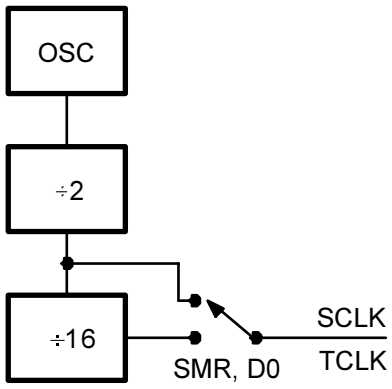


Figure 34. SCLK Circuit

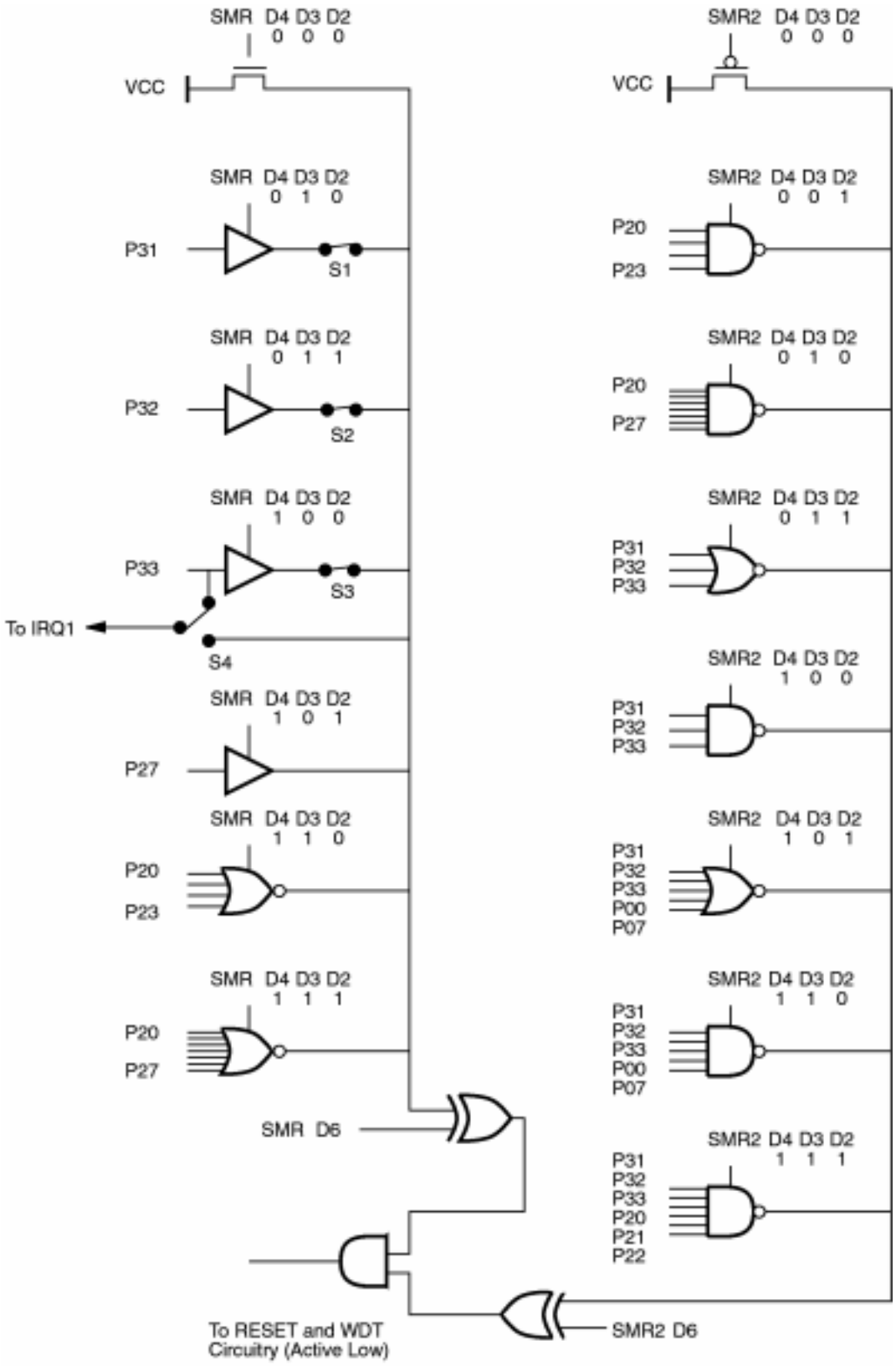


Figure 35. Stop-Mode Recovery Source

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to 0.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the STOP recovery (Figure 35 and Table 12).

Table 12. Stop-Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output will drive the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register for other recover sources.

Stop-Mode Recovery Delay Select (D5). This bit, if low, disables the 5 ms $\overline{\text{RESET}}$ delay after Stop-Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop-Mode Recovery source must be kept active for at least 5TpC.

Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86D73 from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7). This bit is read only. It is set to 1 when the device is recovered from Stop Mode. It is set to 0 when the device reset is other than Stop-Mode Recovery.

Stop-Mode Recovery Register 2 (SMR2). This register determines the mode of Stop-Mode Recovery for SMR2 (Figure 36).

If SMR2 is used in conjunction with SMR, either of the specified events will cause a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source, and P20 is configured as an output, then the remaining SMR pins (P23–P21) form the NAND equation.

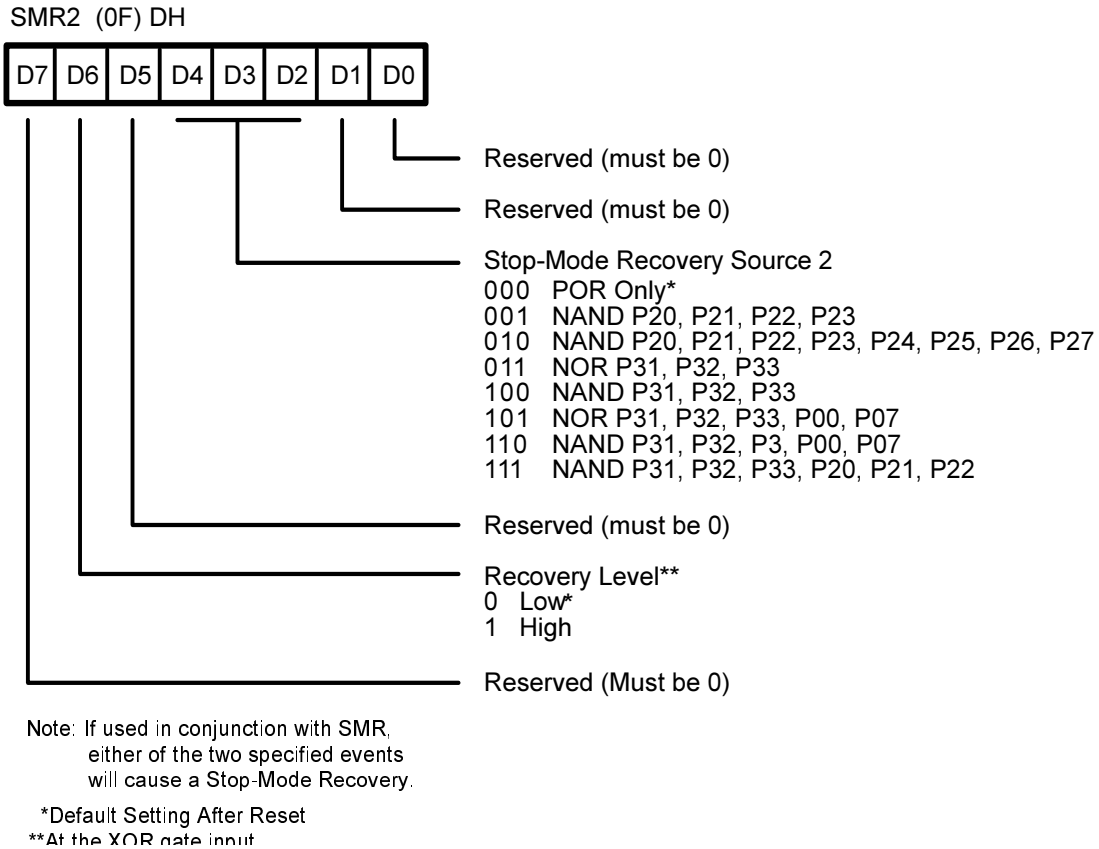


Figure 36. Stop-Mode Recovery Register 2 ((0F) DH: D2–D4, D6 Write Only)

FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the minimum time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 37). This register is accessible only during the first 61 processor cycles (122 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. This register is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

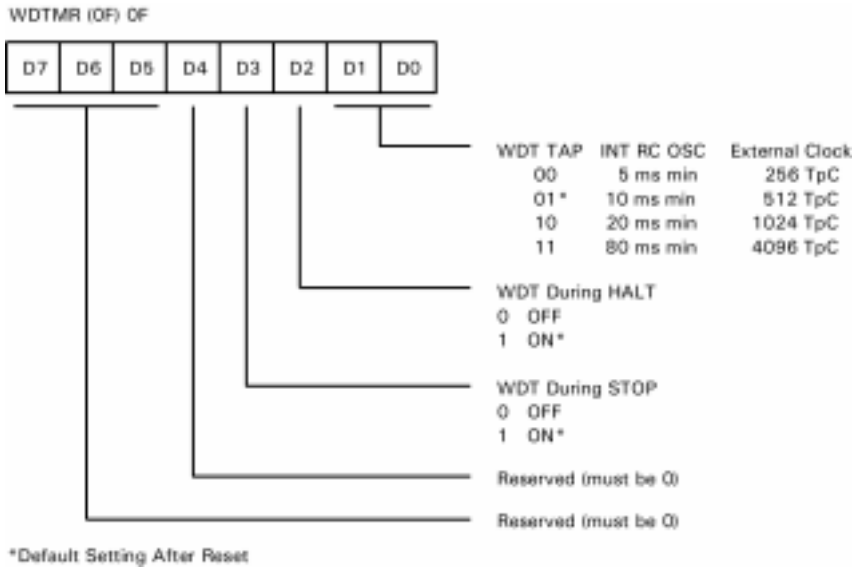


Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1). This bit selects the WDT time period. It is configured as indicated in Table 13.

Table 13. WDT Time Select*

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Note:
*TpC = XTAL clock cycle. The default on reset is 10 ms.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, (XTAL1). The default configuration of this bit is 0, which selects the RC oscillator.

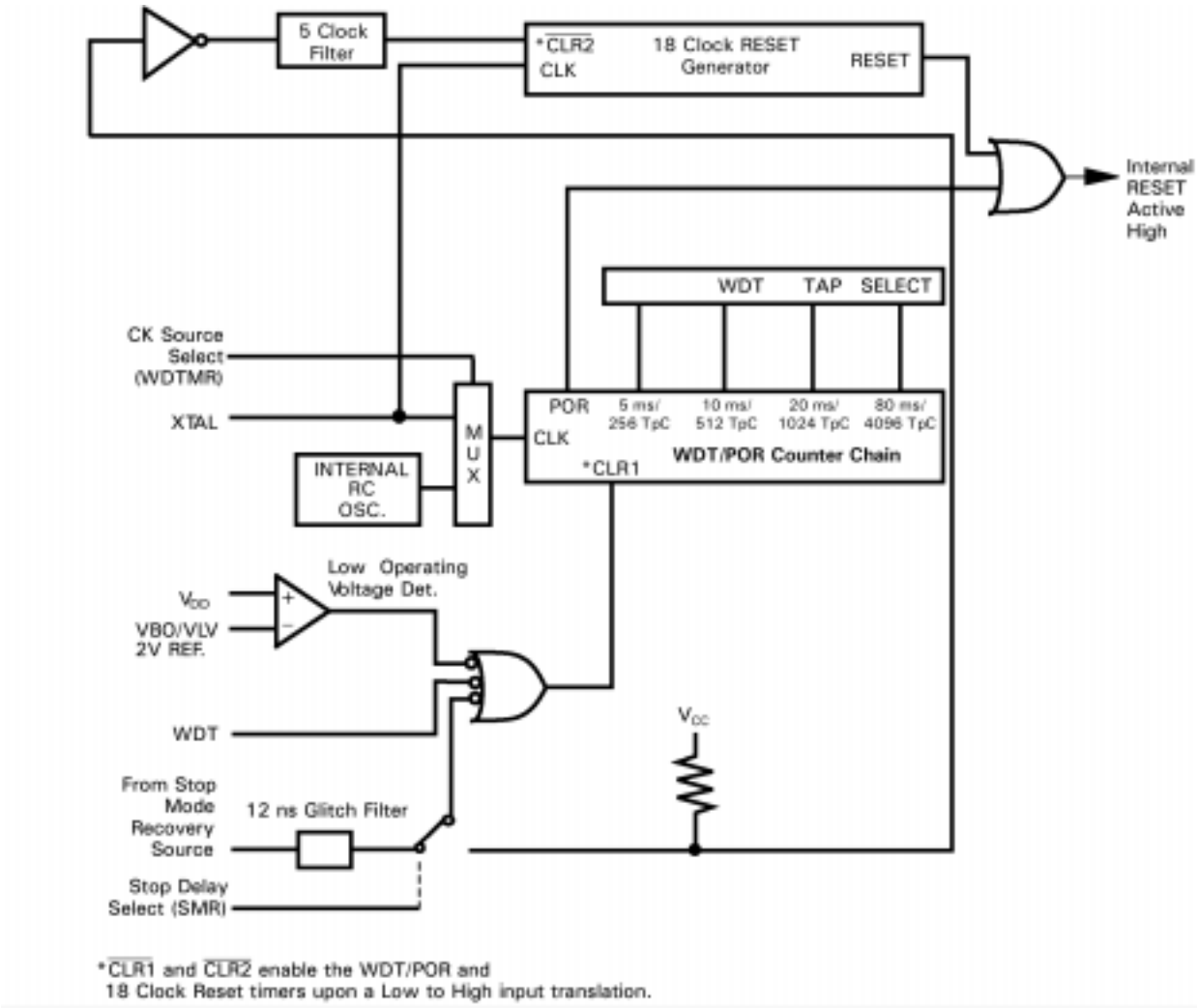


Figure 38. Resets and WDT

Mask Selectable Options. There are seven Mask Selectable Options to choose from based on ROM code requirements. These are:

Table 14. Mask Selectable Options

RC/Other	RC/XTAL
32 kHz XTAL	On/Off
Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
Port 3: Pull-Ups	On/Off
Port 0: 0–3 Normal Mode ($0.5V_{DD}$ Input Threshold) vs. Mouse Mode (0.4 VDD Input Threshold)	

Blown-out Voltage/Standby. An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{BO}. A small drop in V_{CC} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. Typical Low-Voltage power consumpion in this Low Voltage Standby mode (I_{LV}) is about 20 µA. If the V_{CC} is allowed to stay above Vram, the RAM content is preserved. When the power level is returned to above V_{BO}, the device will perform a POR and function normally.

Low-Voltage Detection and Flag. A low-voltage detection circuit can optionally be used when the voltage drops to V_{LVD}. Expanded Register Bank %0D register %0C bit 0 and 1 are used for this option. Bit D0 is used to enable or LVD; bit D1 is the status flag for LVD.

FUNCTIONAL DESCRIPTION (Continued)

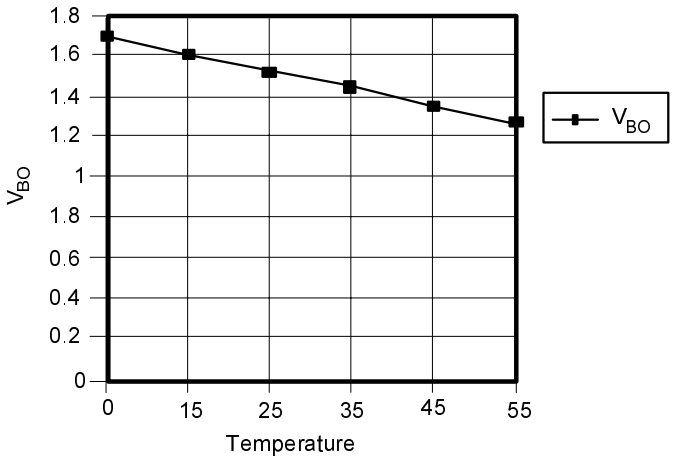


Figure 39. Typical Z86D73 Low Voltage vs. Temperature at 8 MHZ

The minimum operating voltage varies with the temperature and operating frequency, while V_{BO} varies with temperature only.

The Low Voltage trip current (V_{BO}) is less than 2.15V under the following conditions:

Maximum (V_{BO}) Conditions:

T_A = 0°C, +55°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

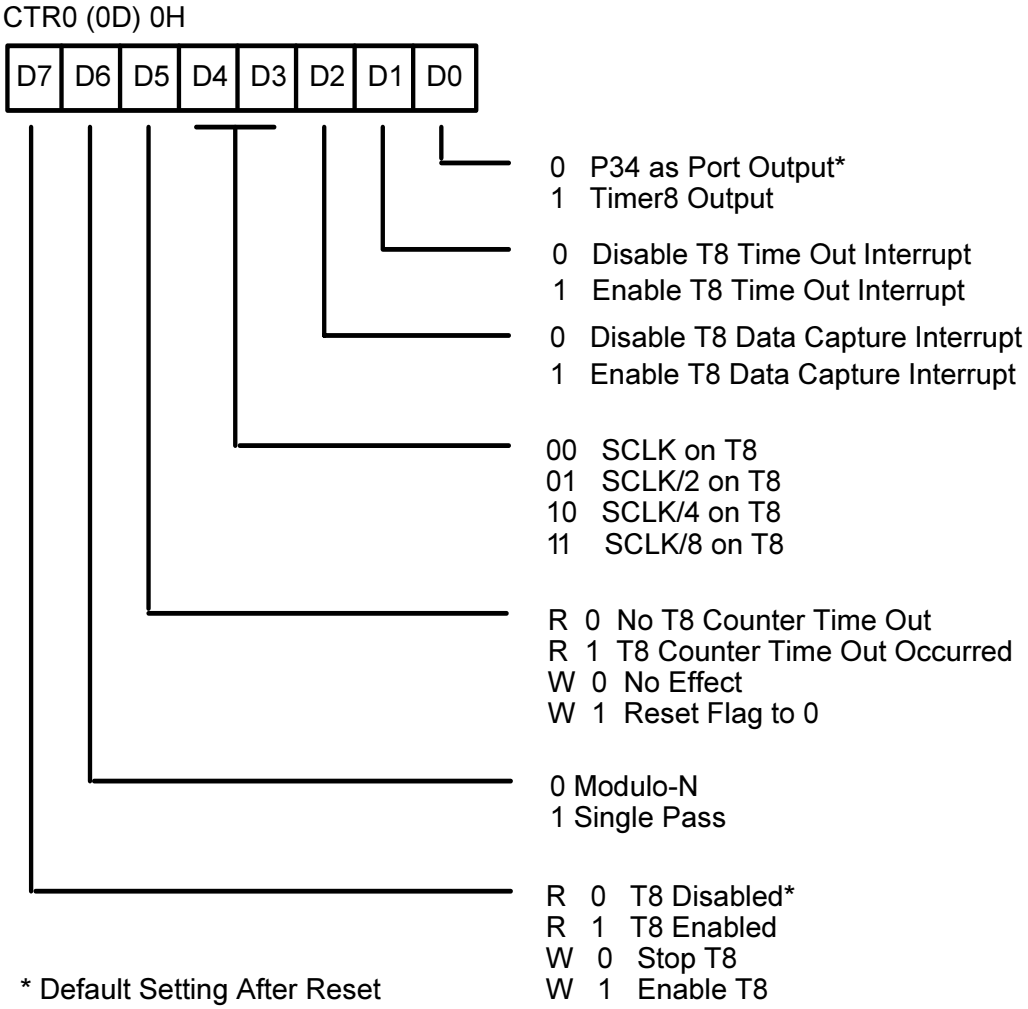


Figure 40. TC8 Control Register
((0D) OH: Read/Write Except Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0D) (Continued)

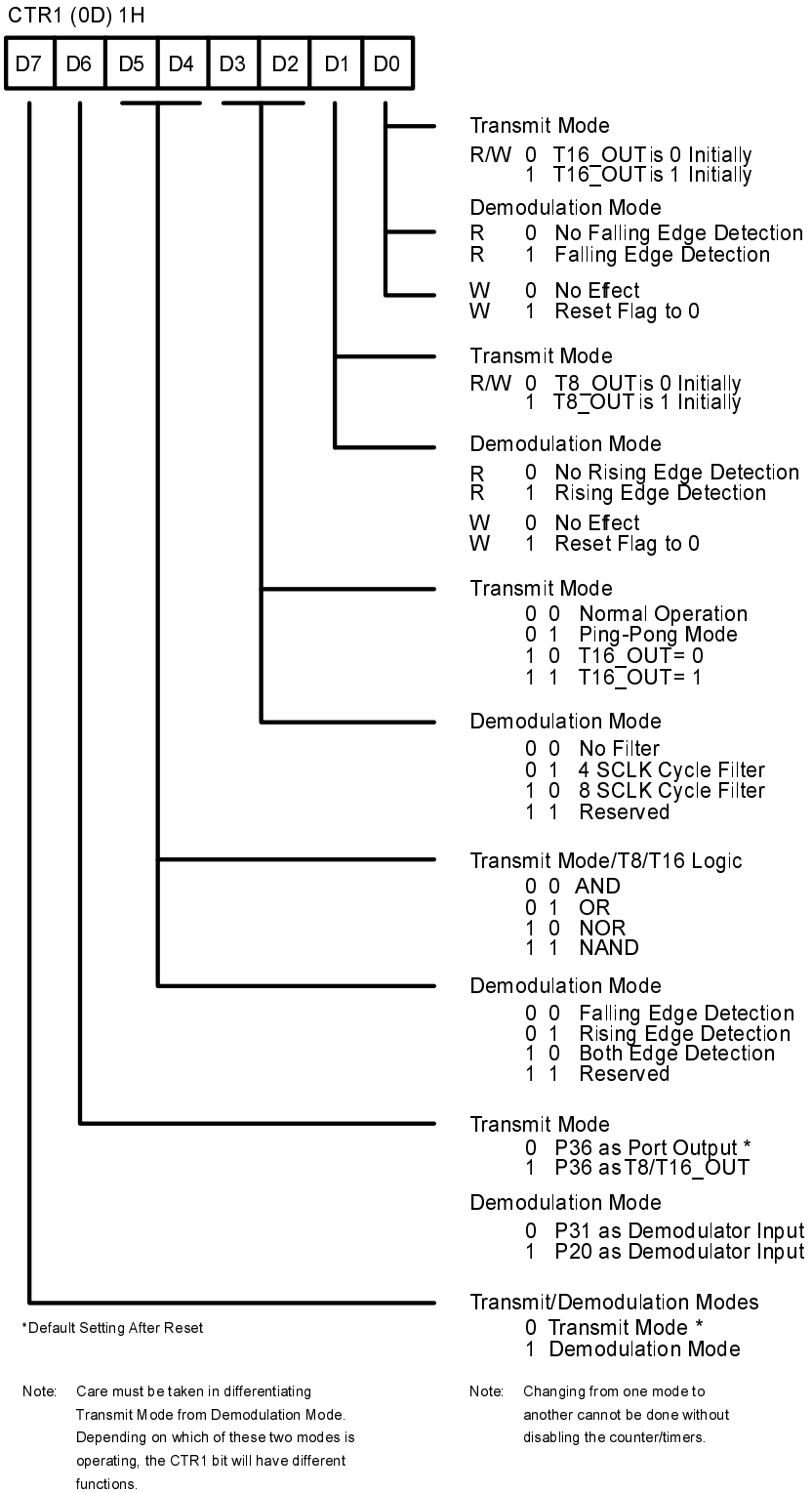


Figure 41. T8 and T16 Common Control Functions ((0D) 1H: Read/Write)

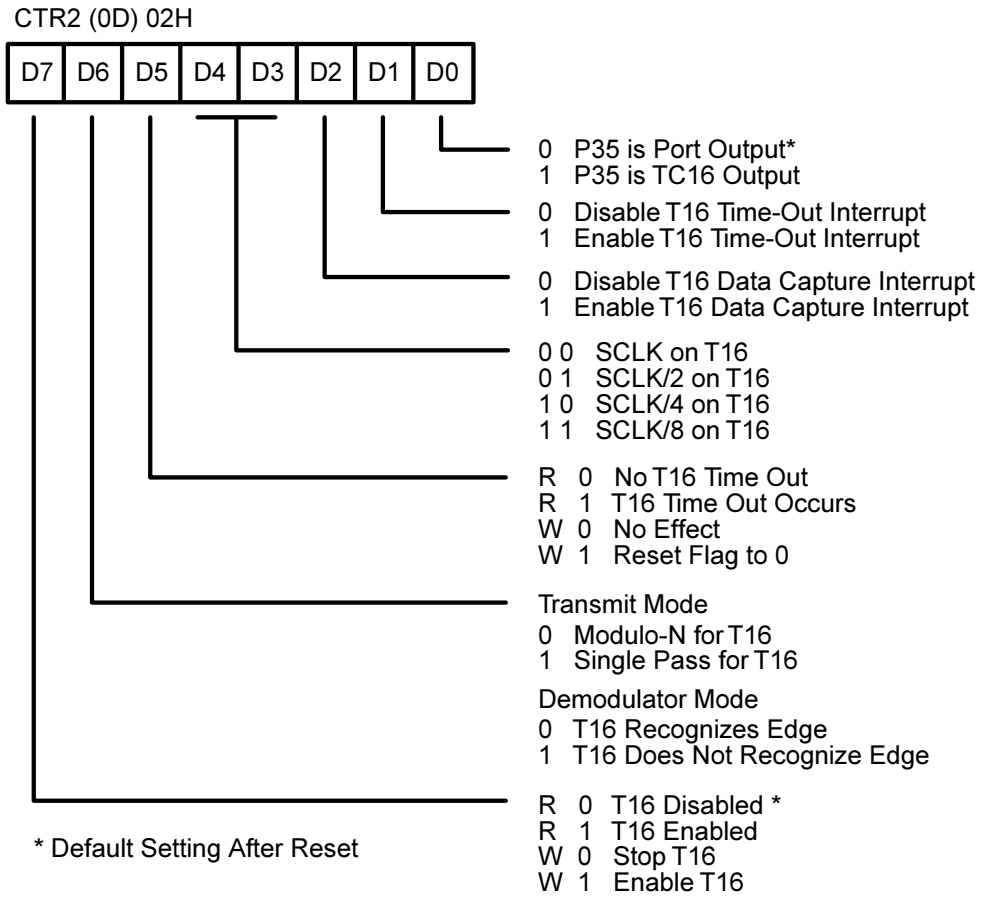


Figure 42. T16 Control Register
((0D) 2H: Read/Write Except Where Noted)

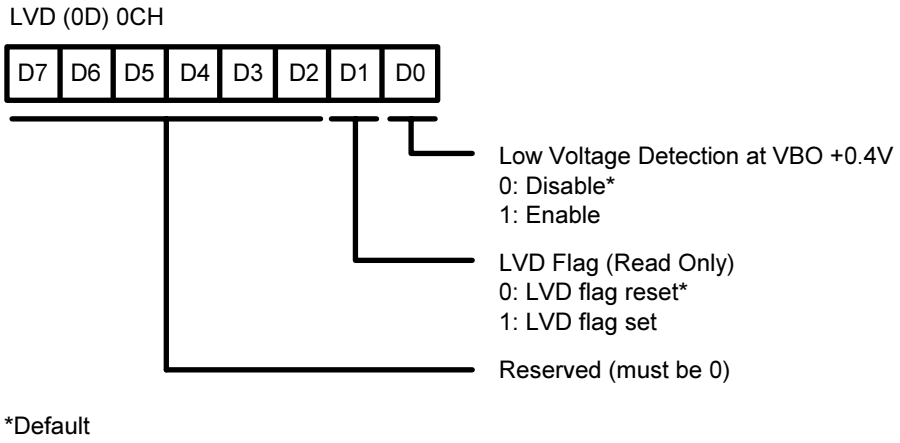


Figure 43. Low-Voltage Detection

EXPANDED REGISTER FILE CONTROL REGISTERS (0F)

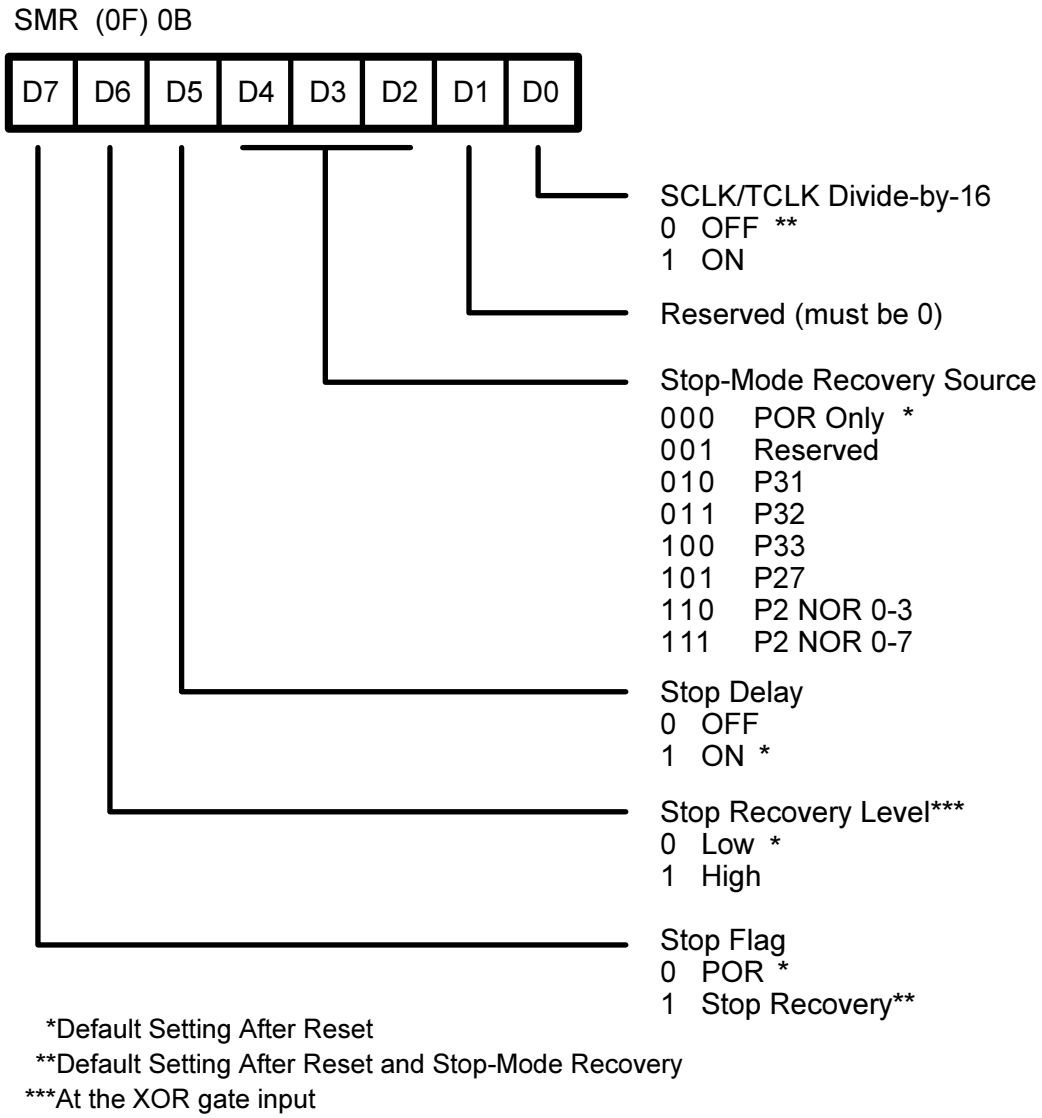


Figure 44. Stop-Mode Recovery Register
((0F) 0BH: D6–D0 = Write Only, D7 = Read Only)

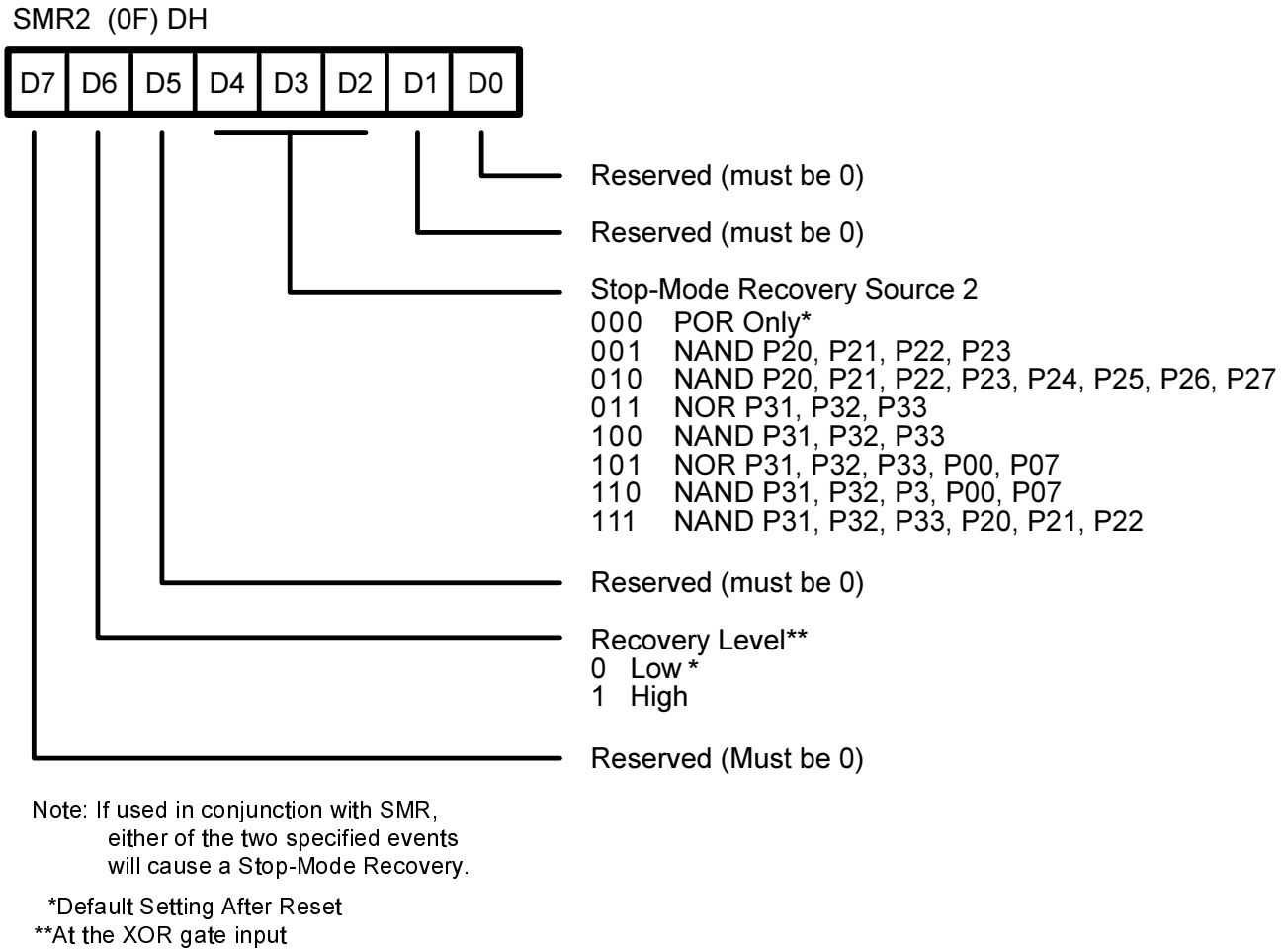


Figure 45. Stop-Mode Recovery Register 2
((0F) 0DH: D2–D4, D6 Write Only)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F) (Continued)

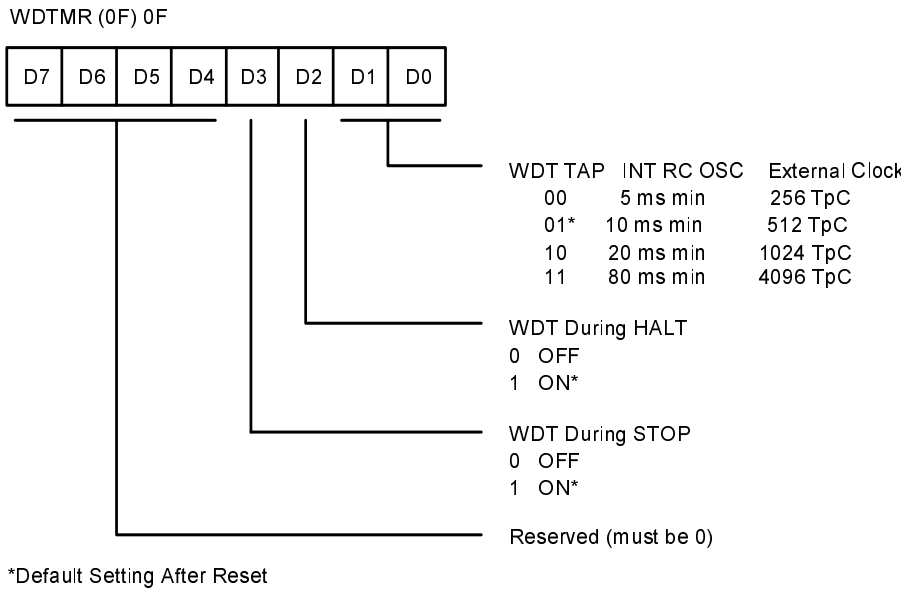


Figure 46. Watch-Dog Timer Register ((0F) 0FH: Write Only)

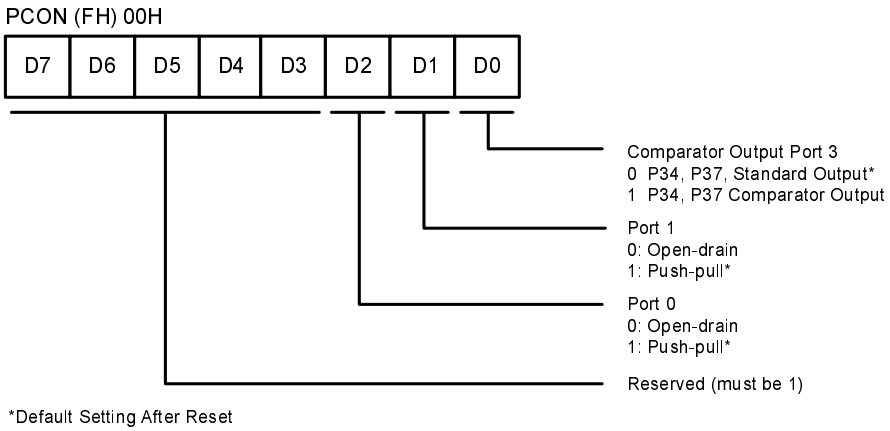


Figure 47. Port Configuration Register (PCON) ((0F) 0H: Write Only)

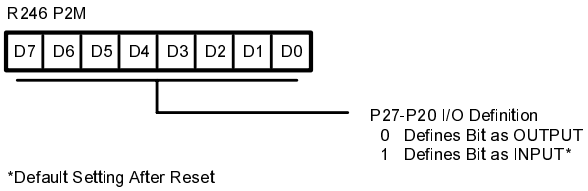


Figure 48. Port 2 Mode Register (F6H: Write Only)

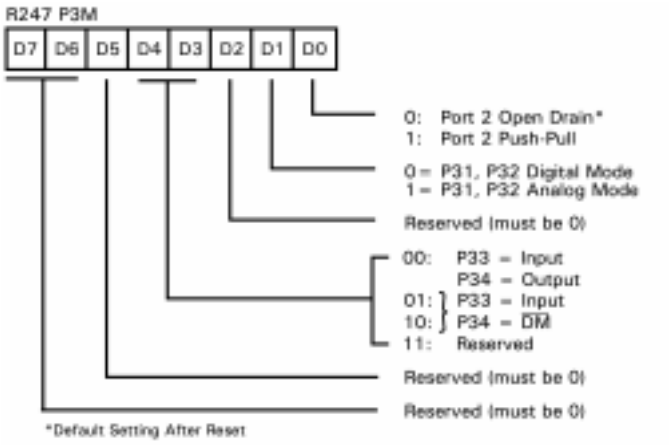


Figure 49. Port 3 Mode Register (F7H: Write Only)

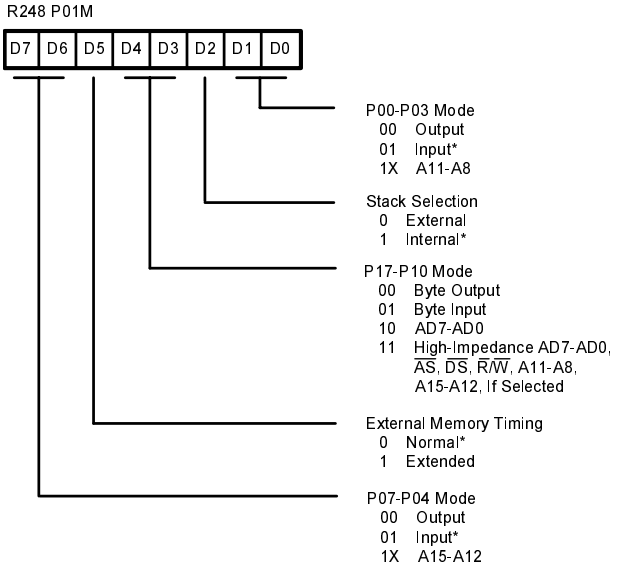


Figure 50. Port0 and 1 Mode Register (F8H: Write Only)

Figure 51. Interrupt Priority Register (F9H: Write Only)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F) (Continued)

Figure 52. Interrupt Request Register (FAH: Read/Write)

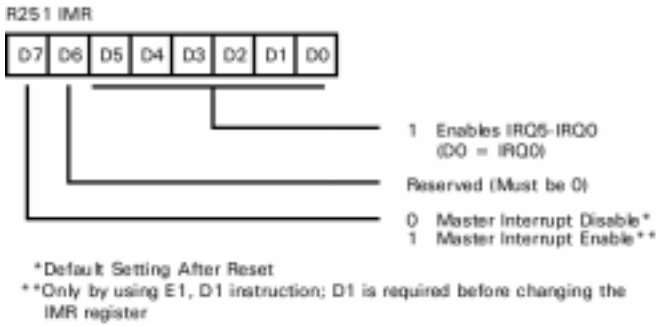


Figure 53. Interrupt Mask Register (FBH: Read/Write)

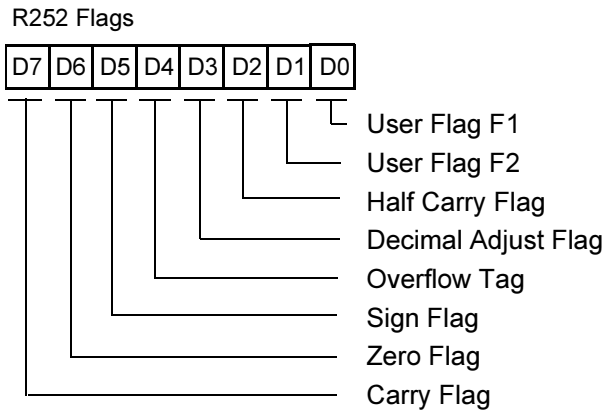


Figure 54. Flag Register (FCH: Read/Write)

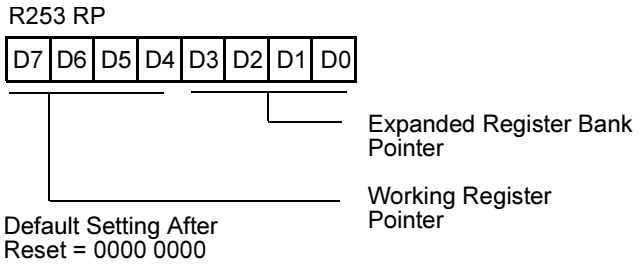


Figure 55. Register Pointer (FDH: Read/Write)

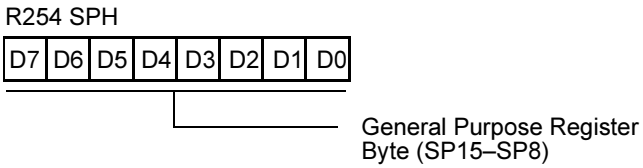


Figure 56. Stack Pointer High (FEH: Read/Write)

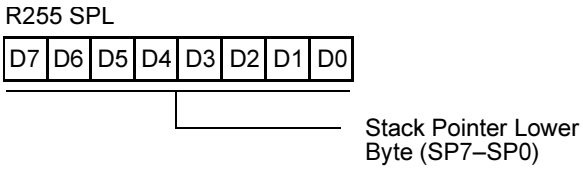
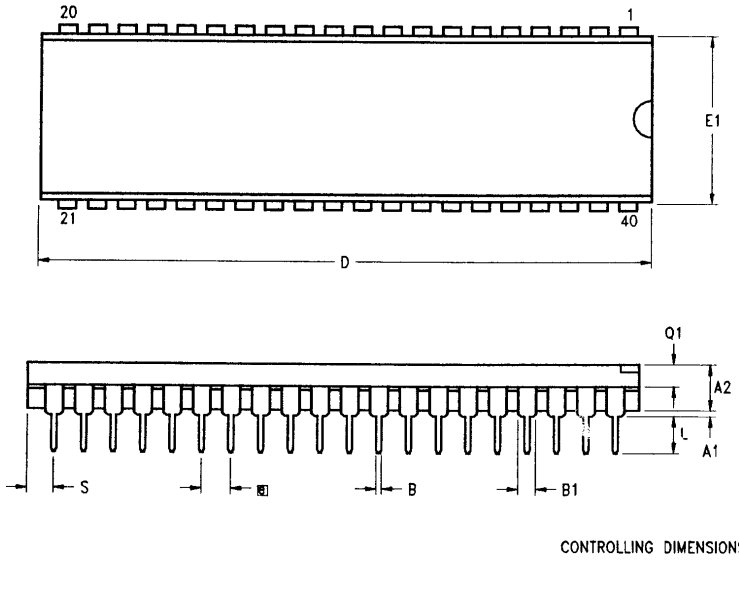


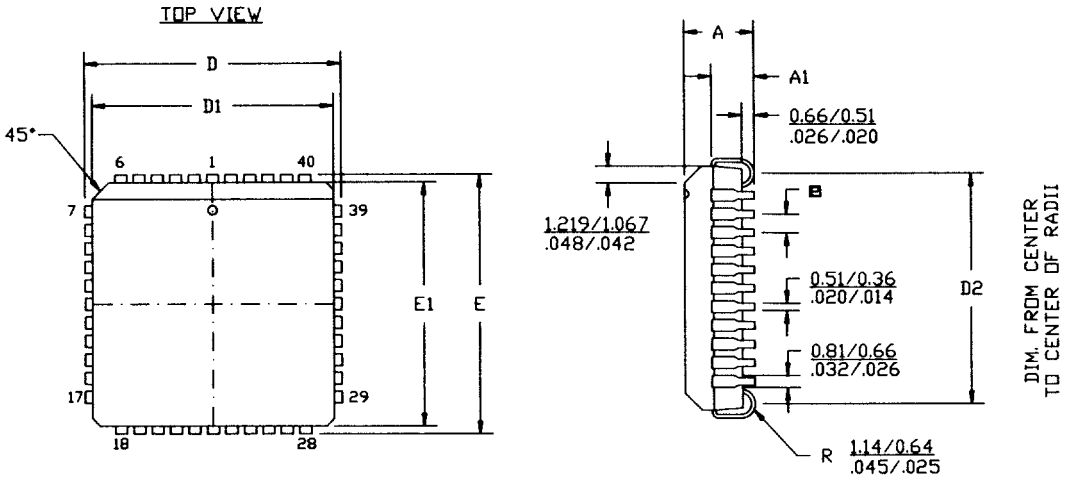
Figure 57. Stack Pointer Low (FFH: Read/Write)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

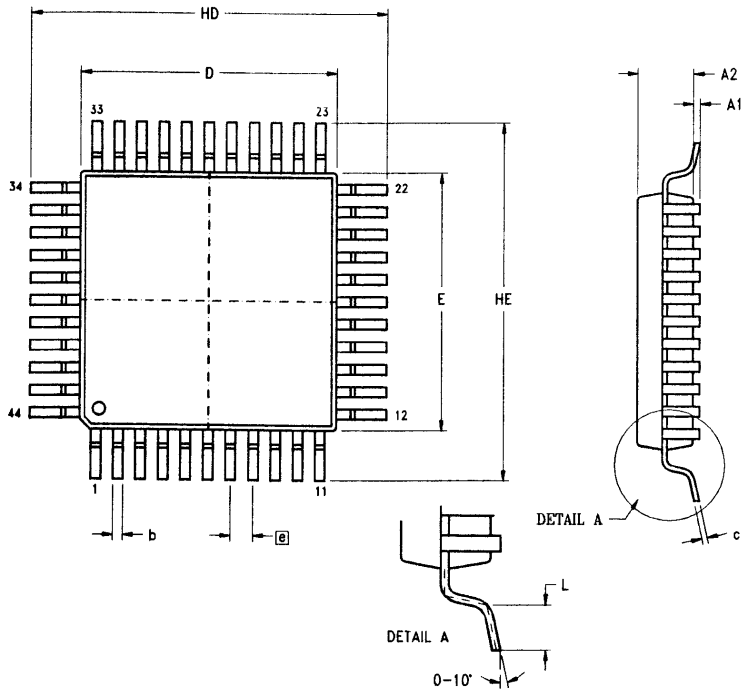
Figure 58. 40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 59. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 / .004"

Figure 60. 44-pin QFP Package Design

ORDERING INFORMATION

Z86D73

8.0-MHz 40-pin DIP	8.0-MHz 44-pin PLCC	8.0-MHz 44-pin QFP
Z86D7308PSC	Z86D7308VSC	Z86D7308FSC

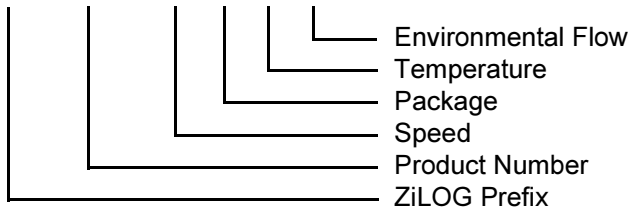
For fast results, contact your ZiLOG sales office for assistance in ordering the part required.

CODES

Package
P = Plastic DIP
F = Plastic Quad Flat Pack
V = Plastic Chip Carrier
S = SOIC (Small Outline Integrated Circuit)
Speed
8 = 8MHz
Environmental
C = Plastic Standard
Temperature
S = 0°C to +70°C

Example:

Z 86D73 08 P S C is a Z86D73, 8 MHz, DIP, 0°C to 70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

Development Projects:

Customer is cautioned that while reasonable efforts will be employed to meet performance objectives and milestone dates, development is subject to unanticipated problems and delays. No production release is authorized or committed until the Customer and ZiLOG have agreed upon a Product Specification for this project.

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