# DATA SHEET

I²C
BUS

# PCA9542A

## 2-channel I²C multiplexer and interrupt logic

PHILIPS
Semiconductors

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# 2-channel I²C multiplexer and interrupt logic          PCA9542A

The pass gates of the multiplexer are constructed such that the $V_{DD}$ pin can be used to limit the maximum high voltage which will be passed by the PCA9542A. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.
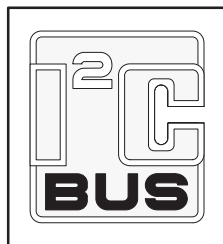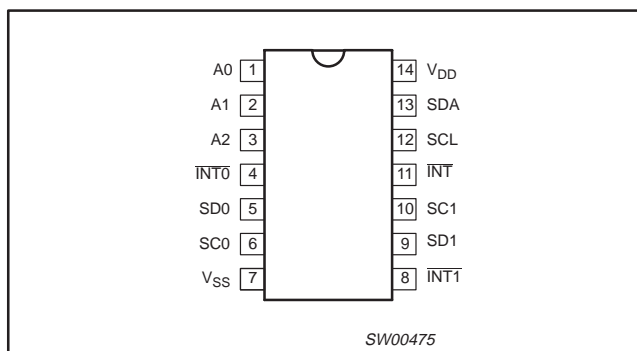
## FEATURES

- 1-of-2 bi-directional translating multiplexer

- I²C interface logic; compatible with SMBus

- 2 Active Low Interrupt Inputs

- Active Low Interrupt Output

- 3 address pins allowing up to 8 devices on the I²C-bus

- Channel selection via I²C-bus

- Power up with all multiplexer channels deselected

- Low $Rds_{ON}$ switches

- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses

- No glitch on power-up

- Supports hot insertion

- Low stand-by current

- Operating power supply voltage range of 2.3 V to 5.5 V

- 5 V tolerant Inputs

- 0 to 400 kHz clock frequency

- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000V per JESD22-C101

- Latchup testing is done to JESDEC Standard JESD78 which exceeds 100 mA

- Packages offered: SO14, TSSOP14

## DESCRIPTION

The PCA9542A is a 1-of-2 bi-directional translating multiplexer, controlled via the I²C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Two interrupt inputs, $\overline{INT0}$ and $\overline{INT1}$, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, $\overline{INT}$, which acts as an AND of the two interrupt inputs, is provided.

A power-on reset function puts the registers in their default state and initializes the I²C state machine with no channels selected.

## PIN CONFIGURATION



**Figure 1.  Pin configuration**

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1 | A0 | Address input 0 |
| 2 | A1 | Address input 1 |
| 3 | A2 | Address input 2 |
| 4 | $\overline{INT0}$ | Active LOW interrupt input 0 |
| 5 | SD0 | Serial data 0 |
| 6 | SC0 | Serial clock 0 |
| 7 | $V_{SS}$ | Supply ground |
| 8 | $\overline{INT1}$ | Active LOW interrupt input 1 |
| 9 | SD1 | Serial data 1 |
| 10 | SC1 | Serial clock 1 |
| 11 | $\overline{INT}$ | Active LOW interrupt output |
| 12 | SCL | Serial clock line |
| 13 | SDA | Serial data line |
| 14 | $V_{DD}$ | Supply voltage |

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | TOPSIDE MARK | DRAWING NUMBER |
|---|---|---|---|---|
| 14-Pin Plastic SO | −40 °C to +85 °C | PCA9542AD | PCA9542AD | SOT108-1 |
| 14-Pin Plastic TSSOP | −40 °C to +85 °C | PCA9542APW | PA9542A | SOT402-1 |

Standard packing quantities and other packaging data is available at www.standardproducts.philips.com/packaging.

# 2-channel I$^2$C multiplexer and interrupt logic
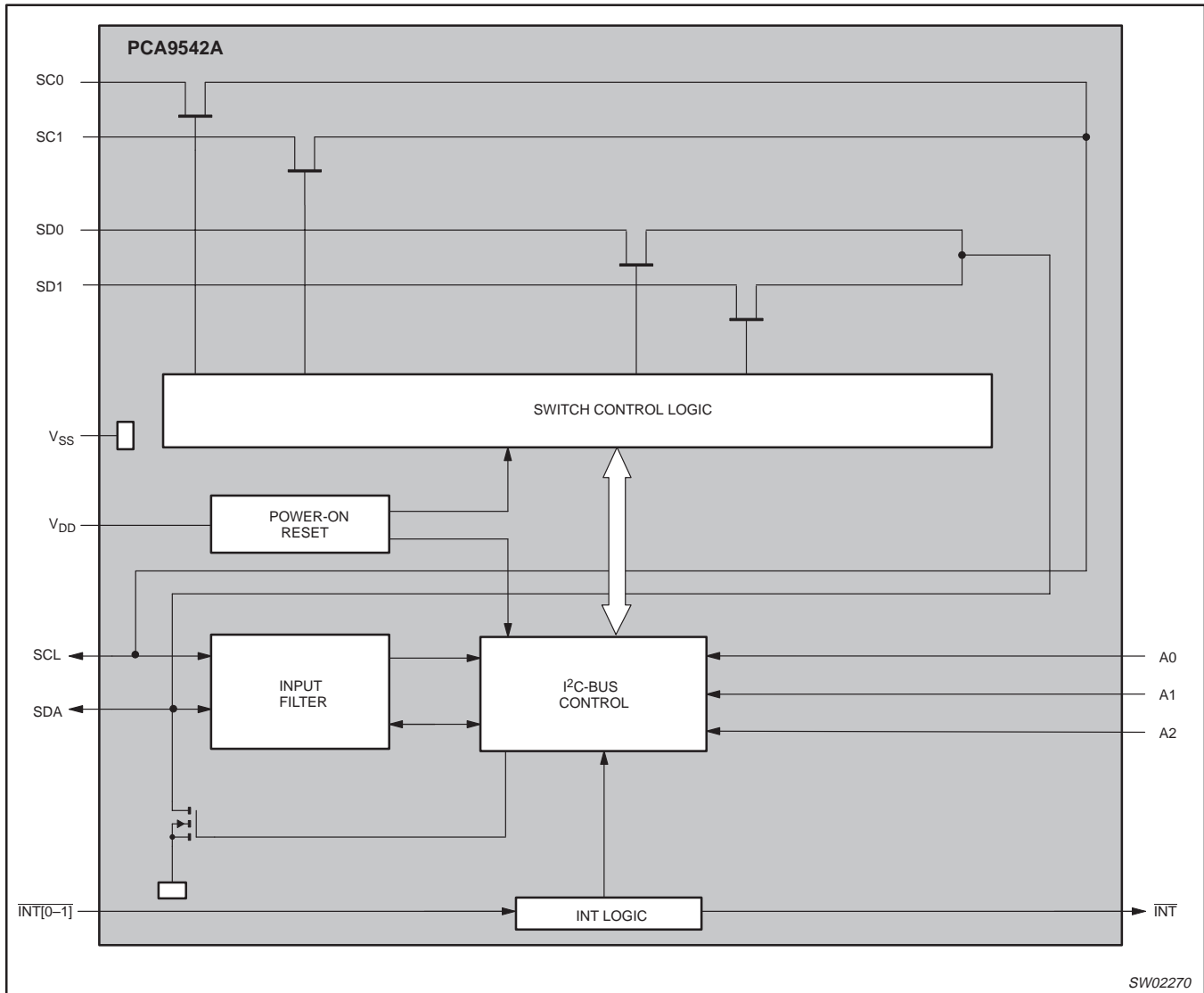
## PCA9542A

### BLOCK DIAGRAM



**Figure 2.  Block diagram**

## 2-channel I$^2$C multiplexer and interrupt logic

## PCA9542A

### DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9542A is shown in Figure 3. To conserve power, no internal pullup resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.
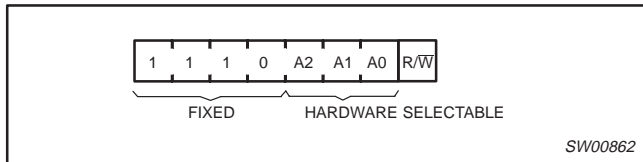
| 1 | 1 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ |

FIXED    HARDWARE SELECTABLE

SW00862

**Figure 3.  Slave address**

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

### CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9542A which will be stored in the Control Register. If multiple bytes are received by the PCA9542A, it will save the last byte received. This register can be written or read via the I$^2$C-bus.
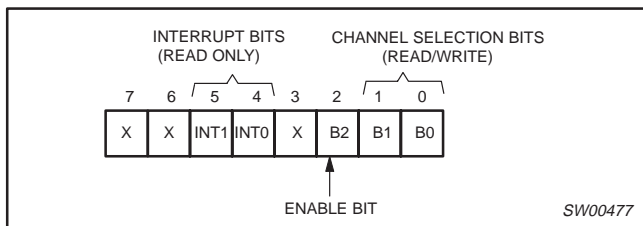
INTERRUPT BITS (READ ONLY)    CHANNEL SELECTION BITS (READ/WRITE)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| X | X | INT1 | INT0 | X | B2 | B1 | B0 |

ENABLE BIT

SW00477

**Figure 4.  Control register**

### CONTROL REGISTER DEFINITION

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9542A has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a stop condition has been placed on the I$^2$C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

**Table 1.  Control Register;  Write — Channel Selection/ Read — Channel Status**

| D7 | D6 | INT1 | INT0 | D3 | B2 | B1 | B0 | COMMAND |
|----|----|------|------|----|----|----|----|---------|
| X | X | X | X | X | 0 | X | X | No channel selected |
| X | X | X | X | X | 1 | 0 | 0 | Channel 0 enabled |
| X | X | X | X | X | 1 | 0 | 1 | Channel 1 enabled |
| X | X | X | X | X | 1 | 1 | X | No channel selected |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No channel selected; power-up default state |

### POWER-ON RESET

When power is applied to $V_{DD}$, an internal Power On Reset holds the PCA9542A in a reset condition until $V_{DD}$ has reached $V_{POR}$. At this point, the reset condition is released and the PCA9542A registers and I$^2$C state machine are initialized to their default states, all zeroes causing all the channels to be deselected. Thereafter, $V_{DD}$ must be lowered below 0.2 V to reset the device.

### INTERRUPT HANDLING

The PCA9542A provides 2 interrupt inputs, one for each channel and one open drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9542A and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte.

Bits 4 – 5 of the control byte correspond to channels 0 – 1 of the PCA9542A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9542A and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9542A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to $V_{DD}$ through a pull-up resistor.

**Table 2.  Control Register; Read — Interrupt**

| D7 | D6 | INT1 | INT0 | D3 | B2 | B1 | B0 | COMMAND |
|----|----|------|------|----|----|----|----|---------|
| 0 | 0 | X | 0 | X | X | X | X | No interrupt on channel 0 |
| 0 | 0 | X | 1 | X | X | X | X | Interrupt on channel 0 |
| 0 | 0 | 0 | X | X | X | X | X | No interrupt on channel 1 |
| 0 | 0 | 1 | X | X | X | X | X | Interrupt on channel 1 |

**NOTE:**  The 2 interrupts can be active at the same time.

## 2-channel I$^2$C multiplexer and interrupt logic

## PCA9542A

**VOLTAGE TRANSLATION**

The pass gate transistors of the PCA9542A are constructed such that the $V_{DD}$ voltage can be used to limit the maximum voltage that will be passed from one I$^2$C-bus to another.



$V_{pass}$ vs. $V_{DD}$
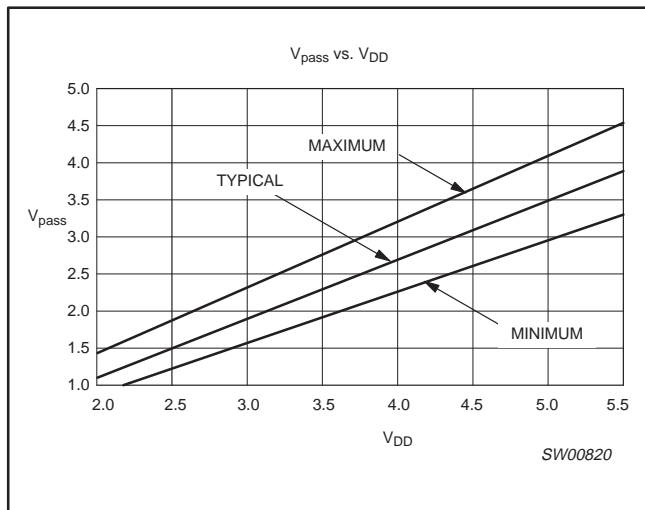
MAXIMUM

TYPICAL

MINIMUM

$V_{DD}$

SW00820

**Figure 5. $V_{pass}$ voltage**

Figure 5 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9542A to act as a voltage translator, the $V_{pass}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{pass}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 5, we see that $V_{pass}$ (max.) will be at 2.7 V when the PCA9542A supply voltage is 3.5 V or lower so the PCA9542A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 12).

More Information can be found in Application Note AN262 *PCA954X family of I$^2$C/SMBus multiplexers and switches.*

# 2-channel I$^2$C multiplexer and interrupt logic

# PCA9542A

## CHARACTERISTICS OF THE I$^2$C-BUS

The I$^2$C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see FIgure 6).
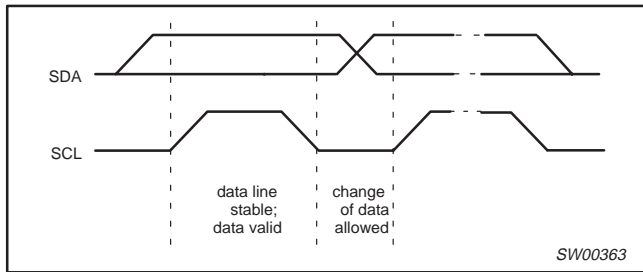
**Figure 6.  Bit transfer**

## Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

## System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).
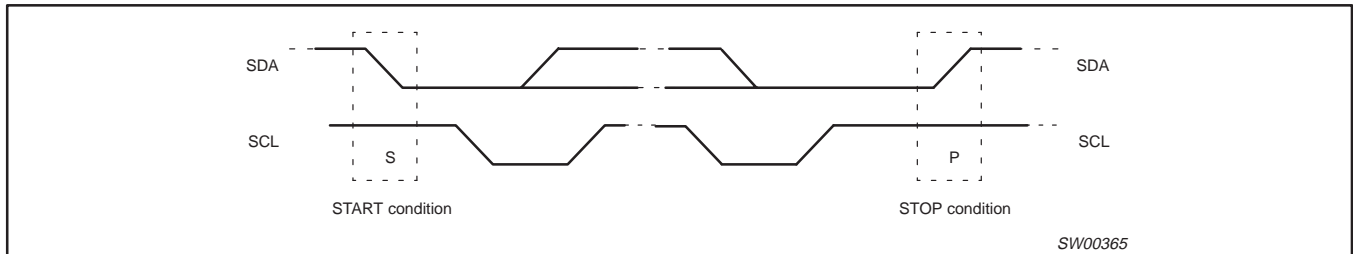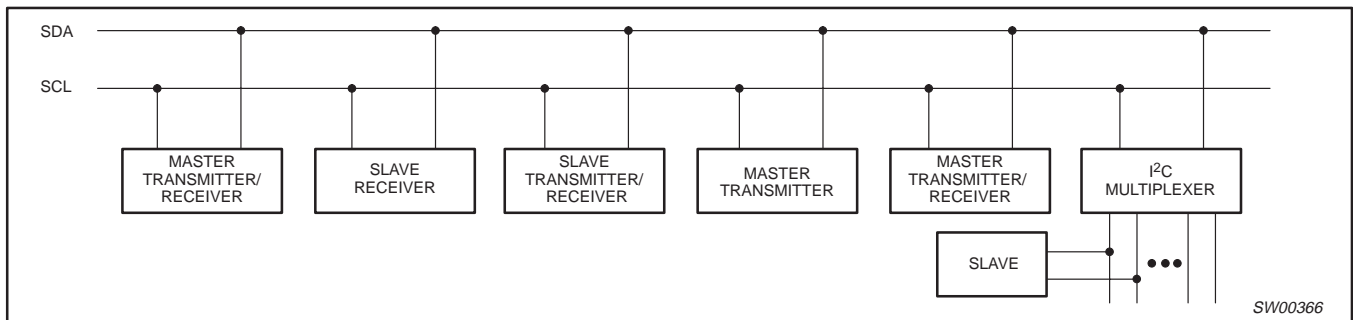
**Figure 7.  Definition of start and stop conditions**

**Figure 8.  System configuration**

2-channel I$^2$C multiplexer and interrupt logic

PCA9542A

## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.
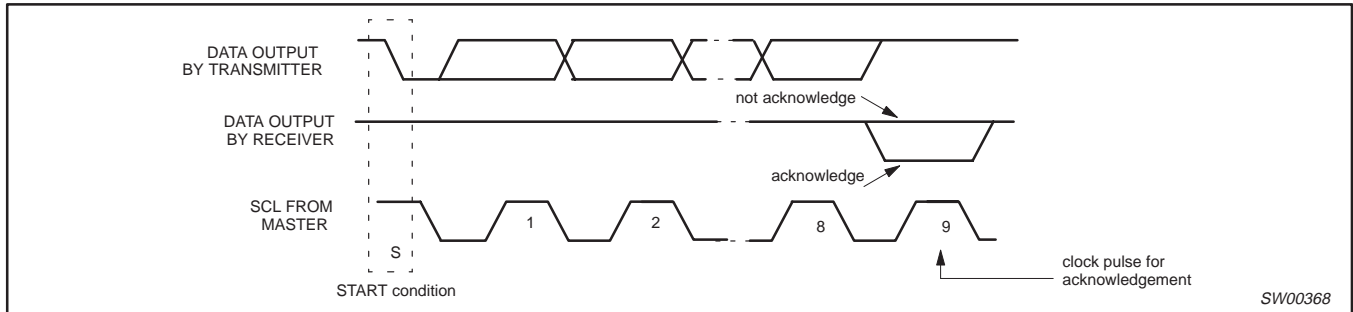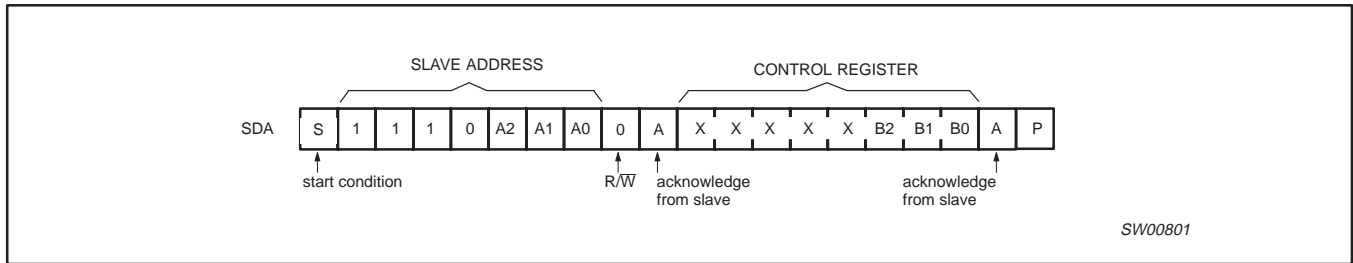


**Figure 9. Acknowledgement on the I$^2$C-bus**
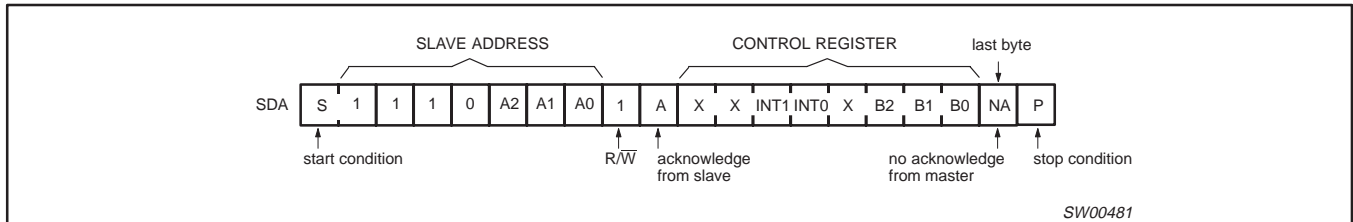


**Figure 10. WRITE control register**



**Figure 11. READ control register**
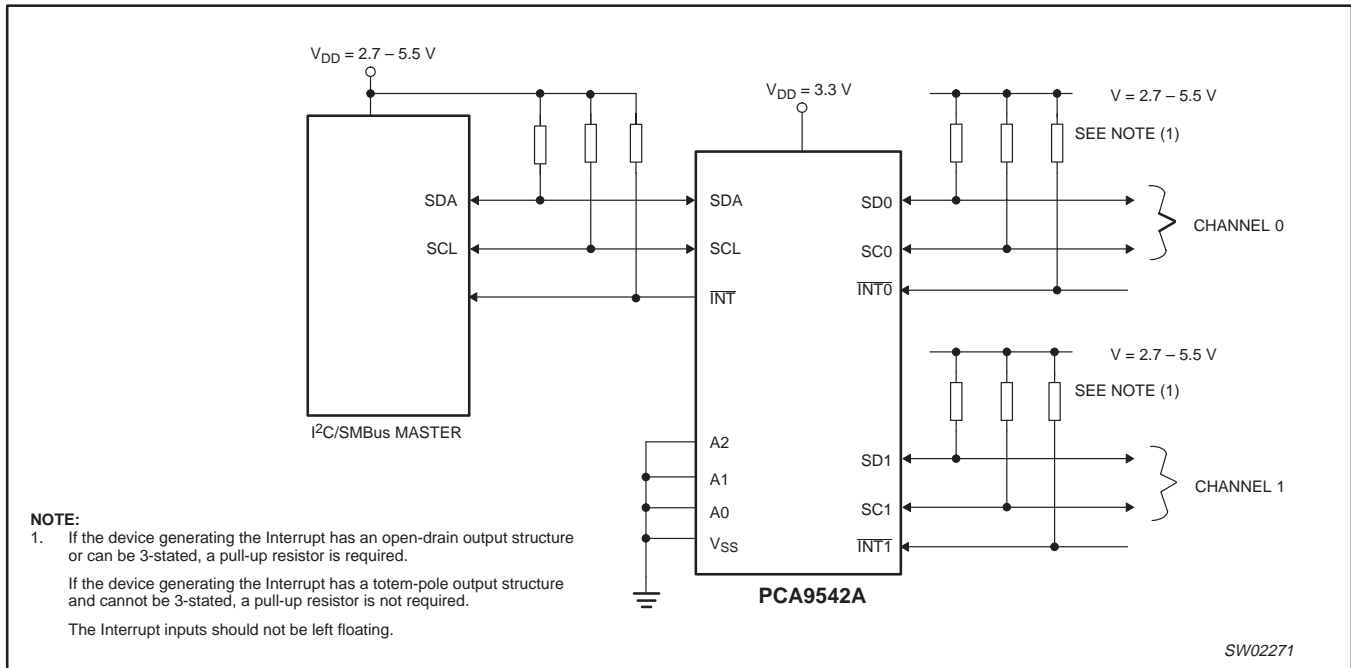
## TYPICAL APPLICATION



**Figure 12. Typical Application**

## ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|--------|-----------|------------|--------|------|
| $V_{DD}$ | DC supply voltage | | −0.5 to +7.0 | V |
| $V_I$ | DC input voltage | | −0.5 to +7.0 | V |
| $I_I$ | DC input current | | ±20 | mA |
| $I_O$ | DC output current | | ±25 | mA |
| $I_{DD}$ | Supply current | | ±100 | mA |
| $I_{SS}$ | Supply current | | ±100 | mA |
| $P_{tot}$ | total power dissipation | | 400 | mW |
| $T_{stg}$ | Storage temperature range | | −60 to +150 | °C |
| $T_{amb}$ | Operating ambient temperature | | −40 to +85 | °C |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

# 2-channel I$^2$C multiplexer and interrupt logic

# PCA9542A

## DC CHARACTERISTICS

$V_{DD}$ = 2.3 V to 3.6 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified. (See page 10 for $V_{DD}$ = 4.5 V to 5.5 V.)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Supply** | | | | | | |
| $V_{DD}$ | Supply voltage | | 2.3 | | 3.6 | V |
| $I_{DD}$ | Supply current | Operating mode; $V_{DD}$ = 3.6 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | − | 10 | 30 | µA |
| $I_{stb}$ | Standby current | Standby mode; $V_{DD}$ = 3.6 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SLC}$ = 0 KHz | − | 0.1 | 1 | µA |
| $V_{POR}$ | Power-on reset voltage (Note 1) | no load; $V_I$ = $V_{DD}$ or $V_{SS}$ | − | 1.6 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.5 | − | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | − | 6 | V |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | 7 | − | mA |
| | | $V_{OL}$ = 0.6 V | 6 | 10 | − | |
| $I_L$ | Leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | − | +1 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | − | 9 | 10 | pF |
| **Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.5 | − | +0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | − | $V_{DD}$ + 0.5 | V |
| $I_{LI}$ | Input leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | − | +1 | µA |
| $C_i$ | Input capacitance | $V_I$ = $V_{SS}$ | − | 1.6 | 3 | pF |
| **Pass Gate** | | | | | | |
| $R_{ON}$ | Switch resistance | $V_{CC}$ = 3.0 to 3.6 V, $V_O$ = 0.4 V, $I_O$ = 15 mA | 5 | 11 | 30 | Ω |
| | | $V_{CC}$ = 2.3 to 2.7 V, $V_O$ = 0.4V, $I_O$ = 10 mA | 7 | 16 | 55 | |
| $V_{Pass}$ | Switch output voltage | $V_{swin}$ = $V_{DD}$ = 3.3 V; $I_{swout}$ = −100 µA | | 1.9 | | V |
| | | $V_{swin}$ = $V_{DD}$ = 3.0 to 3.6 V; $I_{swout}$ = −100 µA | 1.6 | | 2.8 | |
| | | $V_{swin}$ = $V_{DD}$ = 2.5 V; $I_{swout}$ = −100 µA | | 1.5 | | |
| | | $V_{swin}$ = $V_{DD}$ = 2.3 to 2.7 V; $I_{swout}$ = −100 µA | 1.1 | | 2.0 | |
| $I_L$ | Leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | −1 | − | +1 | µA |
| $C_{io}$ | Input/output capacitance | $V_I$ = $V_{SS}$ | − | 3 | 5 | pF |
| **$\overline{INT}$ Output** | | | | | | |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | − | − | mA |
| $I_{OH}$ | HIGH level output current | | — | − | +10 | µA |

**NOTES:**
1. $V_{DD}$ must be lowered to 0.2 V in order to reset part.
2. For operation between published voltage ranges, refer to worst case parameter in both ranges.

2-channel I$^2$C multiplexer and interrupt logic                PCA9542A

## DC CHARACTERISTICS

$V_{DD}$ = 4.5 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified. (See page 9 for $V_{DD}$ = 2.3 V to 3.6 V.)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Supply** | | | | | | |
| $V_{DD}$ | Supply voltage | | 4.5 | | 5.5 | V |
| $I_{DD}$ | Supply current | Operating mode; $V_{DD}$ = 5.5 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | – | 25 | 100 | µA |
| $I_{stb}$ | Standby current | Standby mode; $V_{DD}$ = 5.5 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SLC}$ = 0 KHz | – | 0.3 | 1 | µA |
| $V_{POR}$ | Power-on reset voltage | no load; $V_I = V_{DD}$ or $V_{SS}$ | – | 1.7 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.5 | – | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | – | 6 | V |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | – | – | mA |
| | | $V_{OL}$ = 0.6 V | 6 | – | – | mA |
| $I_{LI}$ | Leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | – | +1 | µA |
| $C_i$ | Input capacitance | $V_I = V_{SS}$ | – | 9 | 10 | pF |
| **Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$** | | | | | | |
| $V_{IL}$ | LOW level input voltage | | −0.5 | – | +0.3 $V_{DD}$ | V |
| $V_{IH}$ | HIGH level input voltage | | 0.7 $V_{DD}$ | – | $V_{DD}$ + 0.5 | V |
| $I_{LI}$ | Input leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | – | +1 | µA |
| $C_i$ | Input capacitance | $V_I = V_{SS}$ | – | 2 | 5 | pF |
| **Pass Gate** | | | | | | |
| $R_{ON}$ | Switch resistance | $V_{CC}$ = 4.5 to 5.5 V, $V_O$ = 0.4 V, $I_O$ = 15 mA | 4 | 9 | 24 | Ω |
| $V_{Pass}$ | Switch output voltage | $V_{swin} = V_{DD}$ = 5.0 V; $I_{swout}$ = −100 µA | – | 3.6 | – | V |
| | | $V_{swin} = V_{DD}$ = 4.5 to 5.5 V; $I_{swout}$ = −100 µA | 2.6 | – | 4.5 | V |
| $I_L$ | Leakage current | $V_I = V_{DD}$ or $V_{SS}$ | −1 | – | +1 | µA |
| $C_{io}$ | Input/output capacitance | $V_I = V_{SS}$ | – | 3 | 5 | pF |
| **$\overline{INT}$ Output** | | | | | | |
| $I_{OL}$ | LOW level output current | $V_{OL}$ = 0.4 V | 3 | – | – | mA |
| $I_{OH}$ | HIGH level output current | | — | – | +10 | µA |

**NOTES:**
1. $V_{DD}$ must be lowered to 0.2 V in order to reset part.
2. For operation between published voltage ranges, refer to worst case parameter in both ranges.

2-channel I$^2$C multiplexer and interrupt logic                    PCA9542A

## AC CHARACTERISTICS

| SYMBOL | PARAMETER | STANDARD-MODE I$^2$C-bus | | FAST-MODE I$^2$C-bus | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay from SDA to SD$_n$ or SCL to SC$_n$ | — | 0.3[1] | — | 0.3[1] | ns |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | µs |
| $t_{HD;STA}$ | Hold time (repeated) START condition After this period, the first clock pulse is generated | 4.0 | — | 0.6 | — | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | — | 1.3 | — | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | — | 0.6 | — | µs |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | µs |
| $t_{SU;STO}$ | Set-up time for STOP condition | 4.0 | — | 0.6 | — | µs |
| $t_{HD;DAT}$ | Data hold time | 0[2] | 3.45 | 0[2] | 0.9 | µs |
| $t_{SU;DAT}$ | Data set-up time | 250 | — | 100 | — | ns |
| $t_R$ | Rise time of both SDA and SCL signals | — | 1000 | $20 + 0.1C_b$[3] | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | — | 300 | $20 + 0.1C_b$[3] | 300 | µs |
| $C_b$ | Capacitive load for each bus line | — | 400 | — | 400 | µs |
| $t_{SP}$ | Pulse width of spikes which must be suppressed by the input filter | — | 50 | — | 50 | ns |
| $t_{VD:DATL}$[4] | Data valid (HL) | — | 1 | — | 1 | µs |
| $t_{VD:DATH}$[4] | Data valid (LH) | — | 0.6 | — | 0.6 | µs |
| $t_{VD:ACK}$ | Data valid Acknowledge | — | 1 | — | 1 | µs |
| $\overline{INT}$ | | | | | | |
| $t_{iv}$ | $\overline{INTn}$ to $\overline{INT}$ active valid time[4] | — | 4 | — | 4 | µs |
| $t_{ir}$ | $\overline{INTn}$ to $\overline{INT}$ inactive delay time[4] | — | 2 | — | 2 | µs |
| $L_{pwr}$ | LOW level pulse width rejection of $\overline{INTn}$ inputs[4] | 10 | — | 1 | — | ns |
| $H_{pwr}$ | HIGH level pulse width rejection of $\overline{INTn}$ inputs[4] | 500 | — | 500 | — | ns |

NOTES:
1. Pass gate propagation delay is calculated from the 20 Ω typical R$_{ON}$ and and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V$_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. $C_b$ = total capacitance of one bus line in pF.
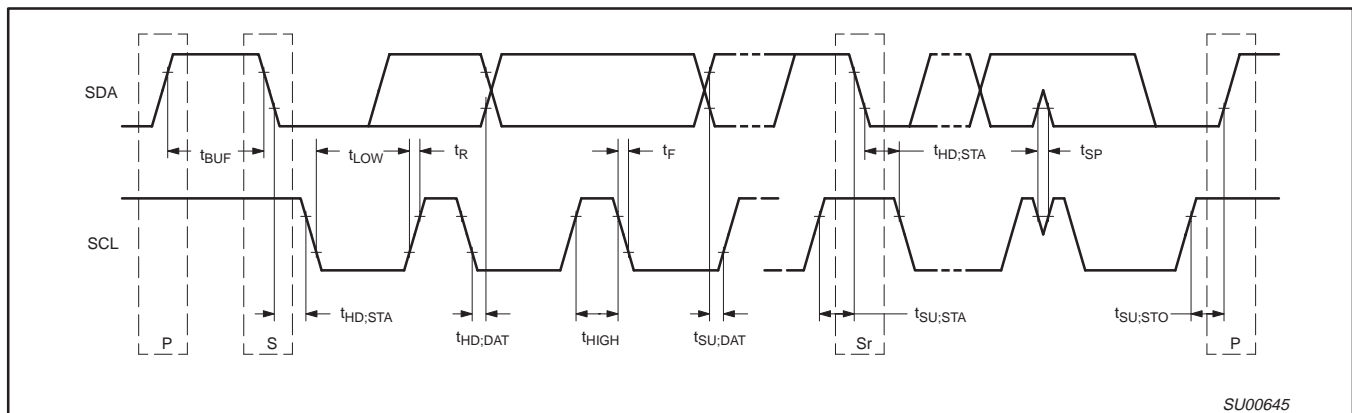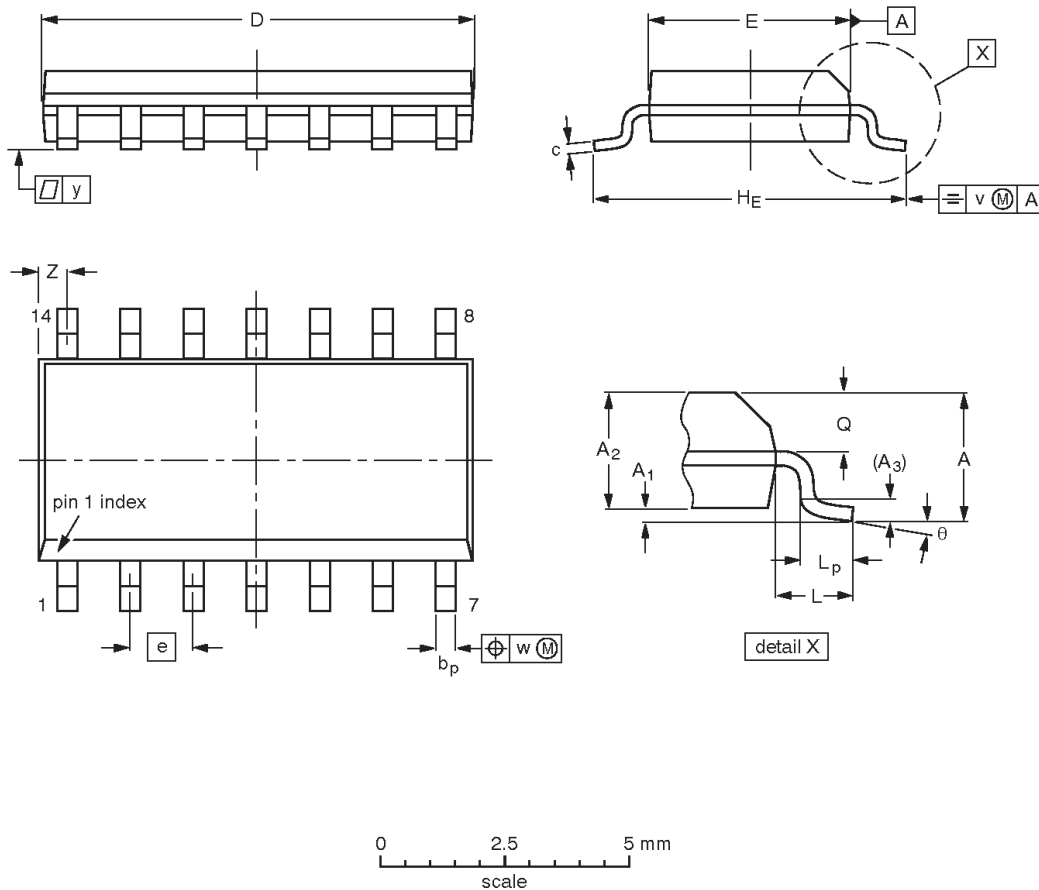4. Measurements taken with a 1 kΩ pull-up resistor and 50 pF load.



**Figure 13. Definition of timing on the I$^2$C-bus**

# 2-channel I²C multiplexer and interrupt logic

## PCA9542A

**SO14:** plastic small outline package; 14 leads; body width 3.9 mm

**SOT108-1**



pin 1 index

detail X

0          2.5          5 mm

scale

**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D[1] | E[1] | e | H_E | L | L_p | Q | v | w | y | Z[1] | θ |
|------|--------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| mm | 1.75 | 0.25 / 0.10 | 1.45 / 1.25 | 0.25 | 0.49 / 0.36 | 0.25 / 0.19 | 8.75 / 8.55 | 4.0 / 3.8 | 1.27 | 6.2 / 5.8 | 1.05 | 1.0 / 0.4 | 0.7 / 0.6 | 0.25 | 0.25 | 0.1 | 0.7 / 0.3 | 8° / 0° |
| inches | 0.069 | 0.010 / 0.004 | 0.057 / 0.049 | 0.01 | 0.019 / 0.014 | 0.0100 / 0.0075 | 0.35 / 0.34 | 0.16 / 0.15 | 0.05 | 0.244 / 0.228 | 0.041 | 0.039 / 0.016 | 0.028 / 0.024 | 0.01 | 0.01 | 0.004 | 0.028 / 0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | 99-12-27 / 03-02-19 |

# 2-channel I²C multiplexer and interrupt logic     PCA9542A

**TSSOP14:    plastic thin shrink small outline package; 14 leads; body width 4.4 mm**     **SOT402-1**



pin 1 index

detail X

```
0        2.5        5 mm
scale
```
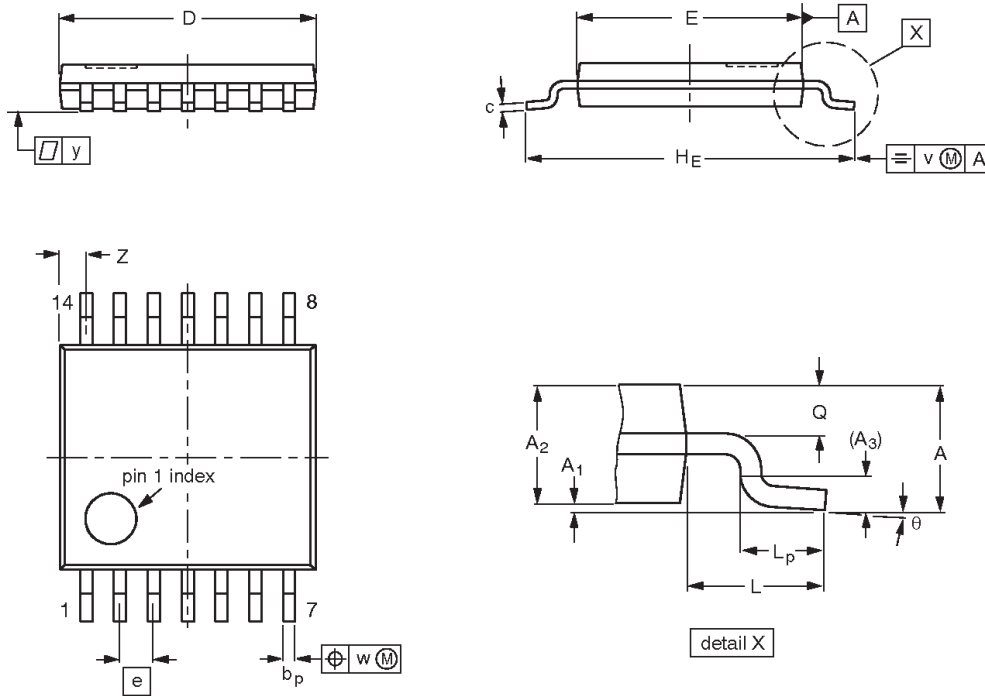
**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D (1) | E (2) | e | Hₑ | L | Lₚ | Q | v | w | y | Z (1) | θ |
|------|--------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.38 | 8° 0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|-------|--|--------------------|-----------|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~ 03-02-18 |

2-channel I$^2$C multiplexer and interrupt logic

PCA9542A

### REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| _2 | 20040929 | **Product data sheet (9397 750 13955).  Supersedes Objective data sheet of 2004 Jul 27 (9397 750 13307).** |
| | | Modifications: |
| | | ● Table 1 "Control Register; Write—Channel Selection / Read—Channel Status" on page 4: add 'No channel selected; power-up default state' row to bottom of table. |
| | | ● DC charateristics ($V_{DD}$ = 2.3 V to 3.6 V) table on page 9: |
| | | – Supply; symbol $I_{DD}$: change Typ. limit from 20 $\mu$A to 10 $\mu$A change Max. limit from 100 $\mu$A to 30 $\mu$A |
| | | – Input SCL; input/output SDA; symbol $I_{OL}$: Test condition $V_{OL}$ = 0.4 V: change Typ. limit from "–" to 7 mA Test condition $V_{OL}$ = 0.6 V: change Typ. limit from "–" to 10 mA |
| | | – $\overline{INT}$ output; symbol $I_{OH}$: change Max. limit from +100 $\mu$A to +10 $\mu$A |
| | | – Add  Note 2. |
| | | ● DC characteristics ($V_{DD}$ = 4.5 V to 5.5 V) table on page 10: |
| | | – change supply voltage range from "$V_{DD}$ = 3.6 V to 5.5 V" to "$V_{DD}$ = 4.5 V to 5.5 V" |
| | | – Supply; symbol $I_{DD}$: change Typ. limit from 65 $\mu$A to 25 $\mu$A |
| | | – Input SCL; input/output SDA: remove parameters for $I_{IL}$ and $I_{IH}$ add parameter $I_L$ |
| | | – Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$; symbol $I_{LI}$: change Max. limit from +50 $\mu$A to +1 $\mu$A |
| | | – Pass Gate; symbol $I_L$: change Min. limit from −10 $\mu$A to −1 $\mu$A change Max. limit from +100 $\mu$A to +1 $\mu$A |
| | | – $\overline{INT}$ output; symbol $I_{OH}$: change Max limit from +100 $\mu$A to +10 $\mu$A |
| | | – Add  Note 2. |
| | | ● AC characteristics table on page 11: table replaced in its entirety. |
| _1 | 20040727 | **Objective data sheet (9397 750 13307).** |

Purchase of Philips I$^2$C components conveys a license under the Philips' I$^2$C patent to use the components in the I$^2$C system provided the system conforms to the I$^2$C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

| Level | Data sheet status [1] | Product status [2] [3] | Definitions |
|-------|----------------------|------------------------|-------------|
| I | Objective data sheet | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[2]  The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3]  For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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