

Linear Systems replaces discontinued Intersil IT122

The LS122 is a monolithic pair of NPN transistors mounted in a single P-DIP package. The monolithic dual chip design reduces parasitics and gives better performance while ensuring extremely tight matching. The LS122 is a direct replacement for discontinued Intersil IT122.

The 8 Pin P-DIP provides ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS122 Features:

- High h_{FE} at low current
- Tight matching
- Tight V_{BE} tracking
- Low Output Capacitance

FEATURES

Direct Replacement for INTERSIL LS122

HIGH h_{FE} @ LOW CURRENT ≥ 80 @ $10\mu A$

OUTPUT CAPACITANCE $\leq 2.0pF$

V_{BE} tracking $\leq 20\mu V/^{\circ}C$

ABSOLUTE MAXIMUM RATINGS¹
@ $25^{\circ}C$ (unless otherwise noted)

Maximum Temperatures

Storage Temperature $-65^{\circ}C$ to $+200^{\circ}C$

Operating Junction Temperature $-55^{\circ}C$ to $+150^{\circ}C$

Maximum Power Dissipation

Continuous Power Dissipation (One side) 250mW

Continuous Power Dissipation (Both sides) 500mW

Linear Derating factor (One side) $2.3mW/^{\circ}C$

Linear Derating factor (Both sides) $4.3mW/^{\circ}C$

Maximum Currents

Collector Current 10mA

MATCHING CHARACTERISTICS @ $25^{\circ}C$ (unless otherwise stated)

| SYMBOL | CHARACTERISTIC | MIN | TYP | MAX | UNITS | CONDITIONS |
|--|---|-----|-----|-----|-------------------|---|
| $ V_{BE1} - V_{BE2} $ | Base Emitter Voltage Differential | -- | -- | 5 | mV | $I_C = 10\mu A, V_{CE} = 5V$ |
| $\Delta (V_{BE1} - V_{BE2}) / \Delta T$ | Base Emitter Voltage Differential Change with Temperature | -- | -- | 20 | $\mu V/^{\circ}C$ | $I_C = 10\mu A, V_{CE} = 5V$ $T_A = -55^{\circ}C$ to $+125^{\circ}C$ |
| $ I_{B1} - I_{B2} $ | Base Current Differential | -- | -- | 25 | nA | $I_C = 10\mu A, V_{CE} = 5V$ |

ELECTRICAL CHARACTERISTICS @ $25^{\circ}C$ (unless otherwise noted)

| SYMBOL | CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---------------|--|------|------|------|-------|--|
| BV_{CBO} | Collector to Base Voltage | 45 | -- | -- | V | $I_C = 10\mu A, I_E = 0$ |
| BV_{CEO} | Collector to Emitter Voltage | 45 | -- | -- | V | $I_C = 10\mu A, I_B = 0$ |
| BV_{EBO} | Emitter-Base Breakdown Voltage | 6.2 | -- | -- | V | $I_E = 10\mu A, I_C = 0^2$ |
| BV_{CCO} | Collector to Collector Voltage | 60 | -- | -- | V | $I_C = 10\mu A, I_E = 0$ |
| h_{FE} | DC Current Gain | 80 | -- | -- | | $I_C = 10\mu A, V_{CE} = 5V$ |
| | | 100 | -- | -- | | $I_C = 1.0mA, V_{CE} = 5V$ |
| $V_{CE(SAT)}$ | Collector Saturation Voltage | -- | -- | 0.5 | V | $I_C = 0.5mA, I_B = 0.05mA$ |
| I_{EBO} | Emitter Cutoff Current | -- | -- | 1 | nA | $I_C = 0, V_{EB} = 3V$ |
| I_{CBO} | Collector Cutoff Current | -- | -- | 1 | nA | $I_E = 0, V_{CB} = 45V$ |
| C_{OBO} | Output Capacitance | -- | -- | 2 | pF | $I_E = 0, V_{CB} = 5V$ |
| C_{C1C2} | Collector to Collector Capacitance | -- | -- | 2 | pF | $V_{CC} = 0V$ |
| I_{C1C2} | Collector to Collector Leakage Current | -- | -- | 10 | nA | $V_{CC} = \pm 60V$ |
| f_T | Current Gain Bandwidth Product | 180 | -- | -- | MHz | $I_C = 1mA, V_{CE} = 5V$ |
| NF | Narrow Band Noise Figure | -- | -- | 3 | dB | $I_C = 100\mu A, V_{CE} = 5V, BW = 200Hz, R_G = 10K\Omega, f = 1KHz$ |

Notes:

1. Absolute Maximum ratings are limiting values above which serviceability may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed $10\mu A$.

Available Packages:

LS122 in P-DIP
LS122 available as bare die



Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

P-DIP (Top View)

