Temperature Sensor with Look-Up Table Memory and DAC

The X96011 is a highly integrated bias controller which incorporates a digitally controlled Programmable Current Generator and temperature compensation using one look-up table. All functions of the device are controlled via a 2-wire digital serial interface.

The temperature compensated Programmable Current Generator varies the output current with temperature according to the contents of the associated nonvolatile look-up table. The look-up table may be programmed with arbitrary data by the user, via the 2-wire serial port, and an internal temperature sensor is used to control the output current response.

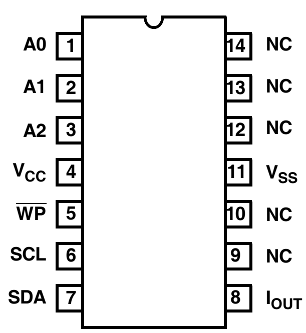
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X96011V14I	X9601 1V I	-40 to +100	14 Ld TSSOP	M14.173
X96011V14IZ (Note)	X9601 1VIZ	-40 to +100	14 Ld TSSOP (Pb-free)	M14.173

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

X96011
(14 LD TSSOP)
TOP VIEW



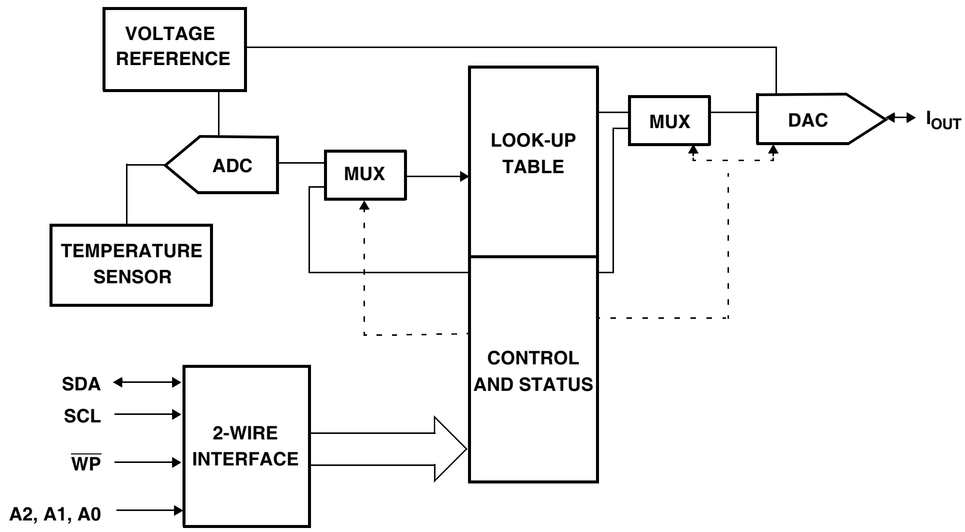
Features

- Single Programmable Current Generator
  - ±1.6mA Max.
  - 8-bit (256 Step) Resolution
  - Internally Programmable Full Scale Current Outputs Internal Voltage Reference
- Integrated 8-bit A/D Converter
- Temperature Compensation
  - Internal Sensor
  - -40°C to +100°C Range
  - 2.2°C/step resolution
  - EEPROM Look-up Table
- Hot Pluggable
- Write Protection Circuitry
  - Intersil BlockLock™
  - Logic Controlled Protection
- 2-wire Bus with 3 Slave Address Bits
- 3V to 5.5V, Single Supply Operation
- Package
  - 14 LD TSSOP
- Pb-Free available (RoHS Compliant)

Applications

- PIN Diode Bias Control
- RF PA Bias Control
- Temperature Compensated Process Control
- Laser Diode Bias Control
- Fan Control
- Motor Control
- Sensor Signal Conditioning
- Data Aquisition Applications
- Gain vs Temperature Control
- High Power Audio
- Open Loop Temperature Compensation
- Close Loop Current, Voltage, Pressure, Temperature, Speed, Position Programmable Voltage Sources, Electronic Loads, Output Amplifiers or Function Generator

Block Diagram



Pin Description

PIN NUMBER	PIN NAME	DESCRIPTION
1	A0	**Device Address Select Pin 0.** This pin determines the LSB of the device address required to communicate using the 2-wire interface. The A0 pin has an on-chip pull-down resistor.
2	A1	**Device Address Select Pin 1.** This pin determines the intermediate bit of the device address required to communicate using the 2-wire interface. The A1 pin has an on-chip pull-down resistor.
3	A2	**Device Address Select Pin 2.** This pin determines the MSB of the device address required to communicate using the 2-wire interface. The A2 pin has an on-chip pull-down resistor.
4	V_{CC}	Supply Voltage.
5	$\overline{WP}$	**Write Protect Control Pin.** This pin is a CMOS compatible input. When LOW, Write Protection is enabled preventing any "Write" operation. When HIGH, various areas of the memory can be protected using the Block Lock bits BL1 and BL0. The $\overline{WP}$ pin has an on-chip pull-down resistor, which enables the Write Protection when this pin is left floating.
6	SCL	**Serial Clock.** This is a TTL compatible input pin. This input is the 2-wire interface clock controlling data input and output at the SDA pin.
7	SDA	**Serial Data.** This pin is the 2-wire interface data into or out of the device. It is TTL compatible when used as an input, and it is Open Drain when used as an output. This pin requires an external pull up resistor.
8	I_{OUT}	**Current Generator Output.** This pin sinks or sources current. The magnitude and direction of the current is fully programmable and adaptive. The resolution is 8 bits.
9, 10, 12,13,14	NC	No Connect.
11	V_{SS}	Ground.

Absolute Maximum Ratings

All voltages are referred to V_{SS}.
Temperature under Bias . . . . -65°C to +100°C
Storage temperature . . . . -65°C to +150°C
Voltage on every pin except V_{CC} . . . . -1.0V to +7V
Voltage on V_{CC} Pin . . . . 0mA to 5.5V
DC Output Current at pin SDA . . . . 0mA to 5mA
DC Output Current at pins Iout . . . . -3 to 3mA
Lead temperature (soldering, 10s) . . . . +300°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
14 Lead TSSOP 96
Pb-free reflow profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range . . . . -40°C to +100°C
Temperature While Writing to Memory . . . . .0°C to +70°C
Voltage on V_{CC} Pin . . . . .3V to 5.5V
Voltage on any other Pin. . . . . V_{CC} ± 0.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

All typical values are for +25°C ambient temperature and 5V at pin V_{CC}. Maximum and minimum specifications are over the recommended operating conditions. All voltages are referred to the voltage at pin V_{SS}. Bit 7 in control register 0 is "1", while other bits in control registers are "0". 400kHz TTL input at SCL. SDA pulled to V_{CC} through an external 2kΩ resistor. 2-wire interface in "standby" (Notes 2 and 3). $\overline{WP}$, A0, A1, and A2 floating.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Iccstby	Standby Current Into V_{CC} Pin	I_{OUT} floating, sink mode			2	mA
Iccfull	Full Operation Current Into V_{CC} Pin	2-wire interface reading from memory, Iout connected to V_{SS}, DAC input bytes: FFh			6	mA
Iccwrite	Nonvolatile Write Current Into V_{CC} Pin	Average from START condition until $t_{\overline{WP}}$ after the STOP condition $\overline{WP}$: Vcc, Iout floating, sink mode VRef unloaded.		4		mA
I_{PLDN}	On-chip Pull Down Current At $\overline{Wp}$, A0, A1,and A2	V($\overline{WP}$), V(A0), V(A1), and V(A2) from 0V to Vcc	0	1	20	µA
V_{ILTTL}	Scl And Sda, Input Low Voltage				0.8	V
V_{IHTTL}	Scl And Sda, Input High Voltage		2.0			V
I_{INTTL}	Scl And Sda Input Current	Pin voltage between 0 and V_{CC}, and SDA as an input.	-1		10	µA
V_{OLSDA}	Sda Output Low Voltage	I(SDA) = 2 mA	0		0.4	V
I_{OHSDA}	Sda Output High Current	V(SDA) = V_{CC}	0		100	µA
V_{ILCMOS}	$\overline{Wp}$, A0, A1, And A2 Input Low Voltage		0		0.2 x V_{CC}	V
V_{IHCMOS}	$\overline{Wp}$, A0, A1, And A2 Input High Voltage		0.8 x V_{CC}		V_{CC}	V
TSenseRange	Temperature Sensor Range	(Note 7)	-40		100	°C
TSenseAccuracy	Temperature Sensor Accuracy			±2		°C
V_{POR}	Power-on Reset Threshold Voltage		1.5		2.8	V
VccRamp	V_{CC} Ramp Rate		0.2		50	mV/µs
V_{ADCOK}	Adc Enable Minimum Voltage	(Figure 8)	2.6		2.8	V

NOTES:

2. The device goes into Standby: 200 ns after any STOP, except those that initiate a nonvolatile write cycle. It goes into Standby t_{WC} after a STOP that initiates a nonvolatile write cycle. It also goes into Standby 9 clock cycles after any START that is not followed by the correct Slave Address Byte.
3. t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
4. This parameter is periodically sampled and not 100% tested.

D/A Converter Characteristics (See pg. 5 for standard conditions)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IFS	Iout Full Scale Current	DAC input Byte = FFh, Source or sink mode, $V(I_{OUT})$ is V_{CC} -1.2V in source mode and 1.2V in sink mode. (Notes 5, 6)	1.56	1.58	1.6	mA
$Offset_{DAC}$	Iout D/a Converter Offset Error		1		1	LSB
$FSError_{DAC}$	Iout D/a Converter Full Scale Error		-2		2	LSB
DNL_{DAC}	Iout D/a Converter Differential Nonlinearity		-0.5		0.5	LSB
INL_{DAC}	Iout D/a Converter Integral Nonlinearity With Respect To A Straight Line Through 0 And The Full Scale Value		-1		1	LSB
VISink	I1 Sink Voltage Compliance	In this range the current at I1 vary < 1%	1.2		V_{CC}	V
VISource	I1 Source Voltage Compliance	In this range the current at I1 vary < 1%	0		V_{CC} - 1.2	V
I_{OVER}	I1 Overshoot On D/a Converter Data Byte Transition	DAC input byte changing from 00h to FFh and vice versa, V(I1) is V_{CC} - 1.2V in source mode and 1.2V in sink mode. (Note 7)			0	µA
I_{UNDER}	I1 Undershoot On D/a Converter Data Byte Transition				0	µA
t_{rDAC}	I1 Rise Time On D/a Converter Data Byte Transition; 10% To 90%		5		30	µs
TCO_{I1I2}	Temperature Coefficient Of Output Current Iout	See Figure 5		±200		ppm/°C

NOTES:

5. LSB is defined as $\left[\frac{2}{3} \times \frac{V(VRef)}{255}\right]$ divided by the resistance between R_1 or R_2 to Vss.
6. $Offset_{DAC}$: The Offset of a DAC is defined as the deviation between the measured and ideal output, when the DAC input is 01h. It is expressed in LSB.
   $FSError_{DAC}$: The Full Scale Error of a DAC is defined as the deviation between the measured and ideal output, when the input is FFh. It is expressed in LSB. The $Offset_{DAC}$ is subtracted from the measured value before calculating $FSError_{DAC}$.
   DNL_{DAC}: The Differential Non-Linearity of a DAC is defined as the deviation between the measured and ideal incremental change in the output of the DAC, when the input changes by one code step. It is expressed in LSB. The measured values are adjusted for Offset and Full Scale Error before calculating DNL_{DAC}.
   INL_{DAC}: The Integral Non-Linearity of a DAC is defined as the deviation between the measured and ideal transfer curves, after adjusting the measured transfer curve for Offset and Full Scale Error. It is expressed in LSB.
7. These parameters are periodically sampled and not 100% tested.

2-Wire Interface AC Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCL}	Scl Clock Frequency	See Table 2-Wire Interface Test Conditions on page 5 (Figure 1, 2 and 3)	1 (Note 10)		400	kHz
t_{IN} (Note 11)	Pulse Width Suppression Time At Inputs				50	ns
t_{AA} (Note 11)	Scl Low To Sda Data Out Valid				900	ns
t_{BUF} (Note 11)	Time The Bus Free Before Start Of New Transmission		1300			ns
t_{LOW}	Clock Low Time		1.3		1200 (Note 10)	µs
t_{HIGH}	Clock High Time		0.6		1200 (Note 10)	µs
$t_{SU:STA}$	Start Condition Setup Time		600			ns
$t_{HD:STA}$	Start Condition Hold Time		600			ns

2-Wire Interface AC Characteristics (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{SU:DAT}$	Data In Setup Time	See Table 2-Wire Interface Test Conditions on page 5 (Figure 1, 2 and 3)	100			ns
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:STO}$	Stop Condition Setup Time		600			ns
t_{DH}	Data Output Hold Time		50			ns
t_R (Note 11)	Sda And Scl Rise Time		20 + 0.1Cb (Note 8)		300	ns
t_F (Note 11)	Sda And Scl Fall Time		20 + 0.1Cb (Note 8)		300	ns
$t_{SU:WP}$ (Note 11)	$\overline{\text{Wp}}$ Setup Time		600			ns
$t_{HD:WP}$ (Note 11)	$\overline{\text{Wp}}$ Hold Time		600			ns
Cb (Note 11)	Capacitive Load For Each Bus Line				400	pF

2-Wire Interface Test Conditions

Input Pulse Levels	10% to 90% of V_{CC}
Input Rise and Fall Times, between 10% and 90%	10ns
Input and Output Timing Threshold Level	1.4V
External Load at pin SDA	2.3kΩ to V_{CC} and 100pF to V_{SS}

Nonvolatile WRITE Cycle Timing

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{WC} (Note 9)	Nonvolatile Write Cycle Time	See Figure 3		5	10	ms

NOTES:

8. Cb = total capacitance of one bus line (SDA or SCL) in pF.
9. t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
10. The minimum frequency requirement applies between a START and a STOP condition.
11. These parameters are periodically sampled and not 100% tested.

Timing Diagrams

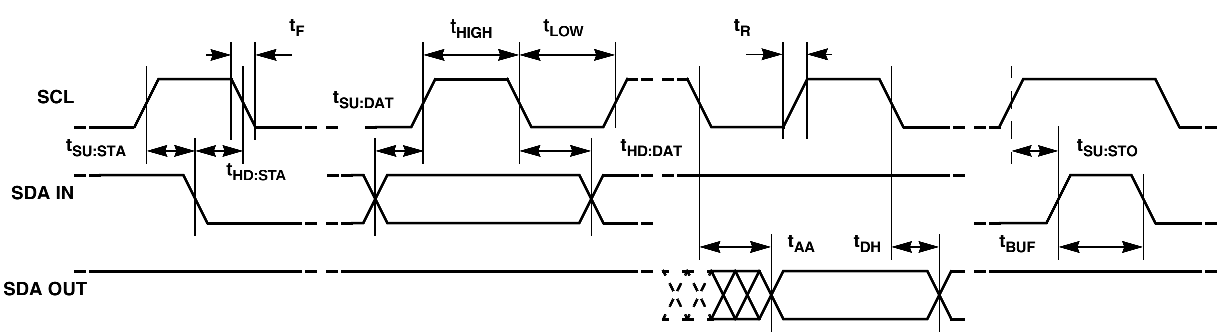


FIGURE 1. BUS TIMING

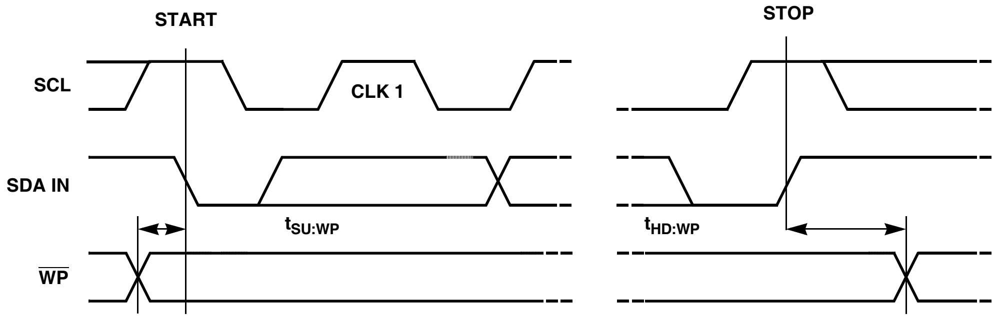


FIGURE 2. WP PIN TIMING

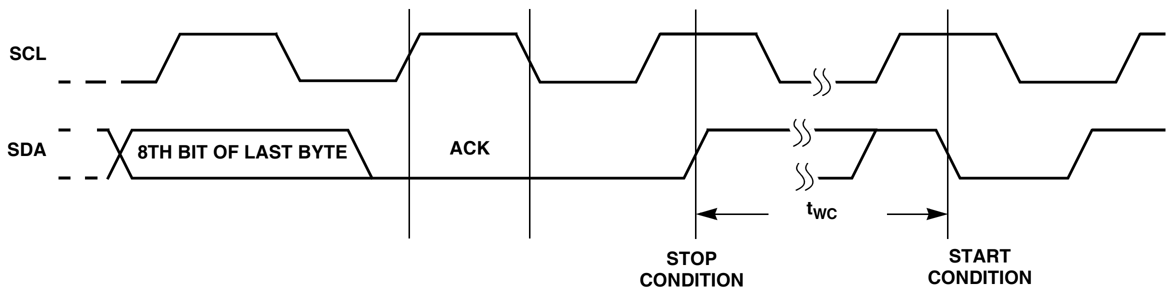


FIGURE 3. NON-VOLATILE WRITE CYCLE TIMING

Intersil Sensor Conditioner Product Family

DEVICE	TITLE	FEATURES/FUNCTIONS							
		INTERNAL TEMPERATURE SENSOR	EXTERNAL SENSOR INPUT	INTERNAL VOLTAGE REFERENCE	VREF INPUT/ OUPUT	GENERAL PURPOSE EEPROM	LOOK-UP TABLE ORGANIZATION	# OF DACS	FSO CURRENT DAC SETTING RESISTORS
X96010	Sensor Conditioner with Dual Look-Up Table Memory and DACs	No	Yes	Yes	Yes	No	Dual Bank	Dual	Ext
X96011	Temperature Sensor with Look-Up Table Memory and DAC	Yes	No	Yes	No	No	Single Bank	Single	Int
X96012	Universal Sensor Conditioner with Dual Look-Up Table Memory and DACs	Yes	Yes	Yes	Yes	Yes	Dual Bank	Dual	Ext / Int

NOTE: FSO = Full Scale Output, Ext = External, Int = Internal

Device Description

The combination of the X96011 functionality and Intersil's QFN package lowers system cost, increases reliability, and reduces board space requirements.

The on-chip Programmable Current Generator may be independently programmed to either sink or source current. The maximum current generated is determined by using an externally connected programming resistor, or by selecting one of three predefined values. Both current generators have a maximum output of ±1.6 mA, and may be controlled to an absolute resolution of 0.39% (256 steps/8 bit).

The current generator is driven using either an on-board temperature sensor or control registers. The internal temperature sensor operates over a very broad temperature range (-40°C to +100°C). The sensor output drives an 8-bit A/D converter. The six MSBs of the ADC output selects one of 64 bytes from the nonvolatile look-up table (LUT).

The contents of the selected LUT row (8-bit wide) drives the input of an 8-bit D/A converter, which generates the output current. All control and setup parameters of the X96011, including the look-up table, are programmable via the 2-wire serial port.

Principles of Operation

Control and Status Registers

The Control and Status Registers provide the user with a mechanism for changing and reading the value of various parameters of the X96011. The X96011 contains five Controls, one Status, and several Reserved registers, each being one Byte wide (See Figure 4). The Control registers 0 through 6 are located at memory addresses 80h through 86h respectively. The Status register is at memory address 87h, and the Reserved registers at memory address 82h, 84h, and 88h through 8Fh.

All bits in Control register 6 always power-up to the logic state "0". All bits in Control registers 0 through 5 power-up to the logic state value kept in their corresponding nonvolatile memory cells. The nonvolatile bits of a register retain their stored values even when the X96011 is powered down, then powered back up. The nonvolatile bits in Control 0 through Control 5 registers are all preprogrammed to the logic state "0" at the factory, except the cases that indicate "1" in Figure 1.

Bits indicated as "Reserved" are ignored when read, and must be written as "0", if any Write operation is performed to their registers.

A detailed description of the function of each of the Control and Status register bits follows.

Control Register 0

This register is accessed by performing a Read or Write operation to address 80h of memory.

ADCFILTOFF: ADC FILTERING CONTROL (NON-VOLATILE)

When this bit is "1", the status register at 87h is updated after every conversion of the ADC. When this bit is "0" (default), the status register is updated after four consecutive conversions with the same result, on the 6 MSBs.

NV13: CONTROL REGISTERS 1 AND 3 VOLATILITY MODE SELECTION BIT (NON-VOLATILE)

When the NV13 bit is set to "0" (default), bytes written to Control registers 1 and 3 are stored in volatile cells, and their content is lost when the X96011 is powered down. When the NV13 bit is set to "1", bytes written to Control registers 1 and 3 are stored in both volatile and nonvolatile cells, and their value doesn't change when the X96011 is powered down and powered back up. See "Writing to Control Registers" on page 16.

IDS: CURRENT GENERATOR DIRECTION SELECT BIT (NON-VOLATILE)

The IDS bit sets the polarity of the Current Generator. When this bit is set to "0" (default), the Current Generator of the X96011 is configured as a Current Source. The Current Generator is configured as a Current Sink when the IDS bit is set to "1". See Figure 5.

BYTE ADDRESS	7 (MSB)	6	5	4	3	2	1	0 (LSB)	REGISTER NAME
80h NON-VOLATILE	1	IDS	NV13	ADCfiltOff	0	0	0	0	CONTROL 0
		Iout Direction 0: Source 1: Sink	CONTROL 1, 3 VOLATILITY 0: VOLATILE 1: NON-VOLATILE	ADC filtering 0: On 1: Off					
DIRECT ACCESS TO THE LUT									
81h VOLATILE OR NON-VOLATILE	RESERVED	RESERVED	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0	CONTROL 1
DIRECT ACCESS TO THE DAC									
83h VOLATILE OR NON-VOLATILE	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	CONTROL 3
85h NON-VOLATILE	0	0	DDAS	LDAS	0	0	IFSO1	IFSO 0	CONTROL 5
			Direct Access to dac 0: Disabled 1: Enabled	Direct Access to lut 0: Disabled 1: Enabled			R Selection 00: Reserved 01: Low Internal 10: Middle Internal 11: High Internal (Default)		
86h VOLATILE	WEL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CONTROL 6
	Write Enable Latch 0: Write Disabled 1: Write Enabled								
ADC OUTPUT									
87H VOLATILE	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	STATUS

REGISTERS IN BYTE ADDRESSES 82H, 84H, AND 88H THROUGH 8FH ARE RESERVED.

REGISTERS BITS SHOWN AS 0 OR 1 SHOULD ALWAYS USE THESE VALUES FOR PROPER OPERATION.

FIGURE 4. CONTROL AND STATUS REGISTER FORMULA

Control Register 1

This register is accessed by performing a Read or Write operation to address 81h of memory. This byte's volatility is determined by bit NV13 in Control register 0.

LDA5 - LDA0: LUT DIRECT ACCESS BITS

When bit LDAS (bit 4 in Control register 5) is set to "1", the LUT is addressed by these six bits, and it is not addressed by the output of the on-chip A/D converter. When bit LDAS is set to "0", these six bits are ignored by the X96011. See Figure 7.

A value between 00h (00_{10}) and 3Fh (63_{10}) may be written to these register bits, to select the corresponding row in the LUT. The written value is added to the base address of the LUT (90h).

Control Register 3

This register is accessed by performing a Read or Write operation to address 83h of memory. This byte's volatility is determined by bit NV13 in Control register 0.

DDA7 - DDA0: D/A DIRECT ACCESS BITS

When bit DDAS (bit 5 in Control register 5) is set to "1", the input to the D/A converter is the content of bits DDA7-DDA0, and it is not a row of LUT. When bit DDAS is set to "0" (default) these eight bits are ignored by the X96011. See Figure 6.

Control Register 5

This register is accessed by performing a Read or Write operation to address 85h of memory.

IFSO1 - IFSO0: CURRENT GENERATOR FULL SCALE OUTPUT SET BITS (NON-VOLATILE)

These two bits are used to set the full scale output current at the Current Generator pin, Iout, according to the following table. The direction of this current is set by bit IDS in Control register 0. See Figure 5.

I1FSO1	I1FSO0	I1 Full Scale Output Current
0	0	Reserved (Don't Use)
0	1	±0.4mA
1	0	±0.85 mA
1	1	±1.3 mA (Default)

LDAS: LUT DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit LDAS is set to "0" (default), the LUT is addressed by the output of the on-chip A/D converter. When bit LDAS is set to "1", LUT is addressed by bits LDA5 - LDA0.

DDAS: D/A DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit DDAS is set to "0" (default), the input to the D/A converter is a row of the LUT. When bit DDAS is set to "1", that input is the content of the Control register 3.

Control Register 6

This register is accessed by performing a Read or Write operation to address 86h of memory.

WEL: WRITE ENABLE LATCH (VOLATILE)

The WEL bit controls the Write Enable status of the entire X96011 device. This bit must be set to "1" before any other Write operation (volatile or nonvolatile). Otherwise, any proceeding Write operation to memory is aborted and no ACK is issued after a Data Byte.

- The WEL bit is a volatile latch that powers up in the "0" state (disabled). The WEL bit is enabled by writing 10000000_2 to Control register 6. Once enabled, the WEL bit remains set to "1" until the X96011 is powered down, and then up again, or until it is reset to "0" by writing 00000000_2 to Control register 6.

A Write operation that modifies the value of the WEL bit will not cause a change in other bits of Control register 6.

Status Register - ADC Output

This register is accessed by performing a Read operation to address 87h of memory.

AD7 - AD0: A/D CONVERTER OUTPUT BITS (READ ONLY)

This byte is the binary output of the on-chip digital thermometer. The output is 00000000_2 for -40°C and 11111111_2 for +100°C. The six MSBs select a row of the LUT.

Look-Up Table

The X96011 memory array contains a 64-byte look-up table. The look-up table is associated to pin Iout's output current generator through the D/A converter. The output of the look-up table is the byte contained in the selected row. By default this byte is the input to the D/A converter driving pin I_{OUT}.

The byte address of the selected row is obtained by adding the look-up table base address 90h, and the appropriate row selection bits. See Figure 6.

By default the look-up table selection bits are the 6 MSBs of the digital thermometer output. Alternatively, the A/D converter can be bypassed and the six row selection bits are the six LSBs of Control Register 1 for the LUT. The selection between these options is illustrated in Figure 6.

Current Generator Block

The Current Generator pin Iout is the output of the current mode D/A converter.

D/A Converter Operation

The Block Diagram for the D/A converter is shown in Figure 5.

The input byte of the D/A converter selects a voltage on the non-inverting input of an operational amplifier. The output of the amplifier drives the gate of a FET. This node is also fed back to the inverting input of the amplifier. The drain of the FET is connected to the output current pin (I_{OUT}) via a "polarity select" circuit block.

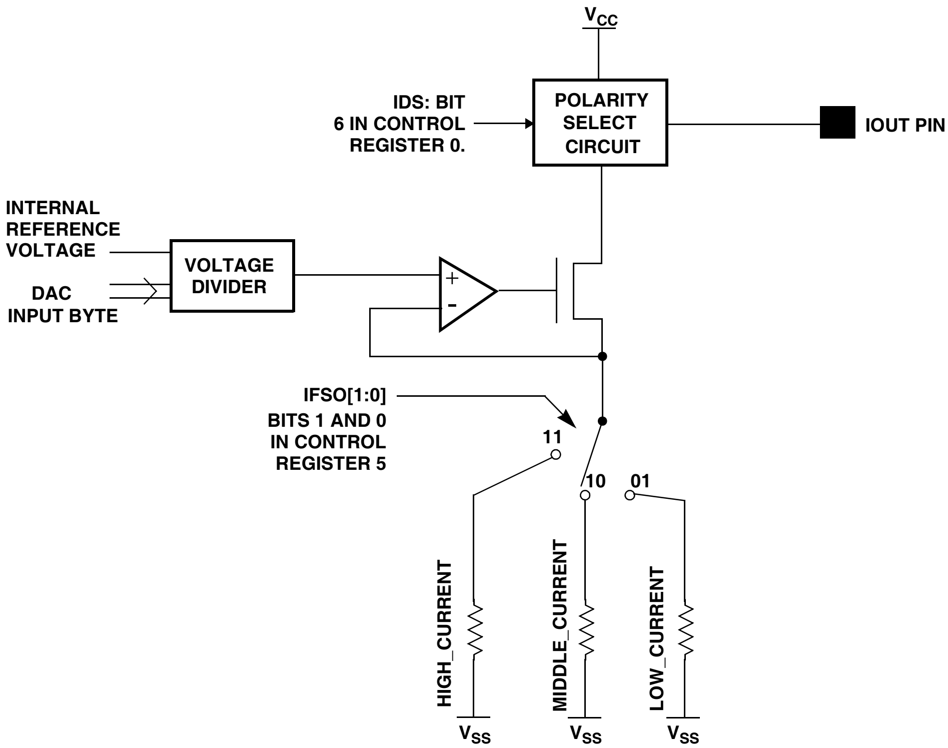


FIGURE 5. D/A CONVERTER BLOCK DIAGRAM

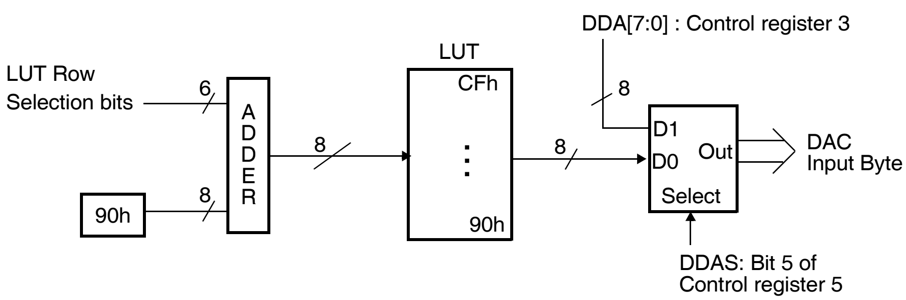


FIGURE 6. LOOK-UP TABLE (LUT) OPERATION

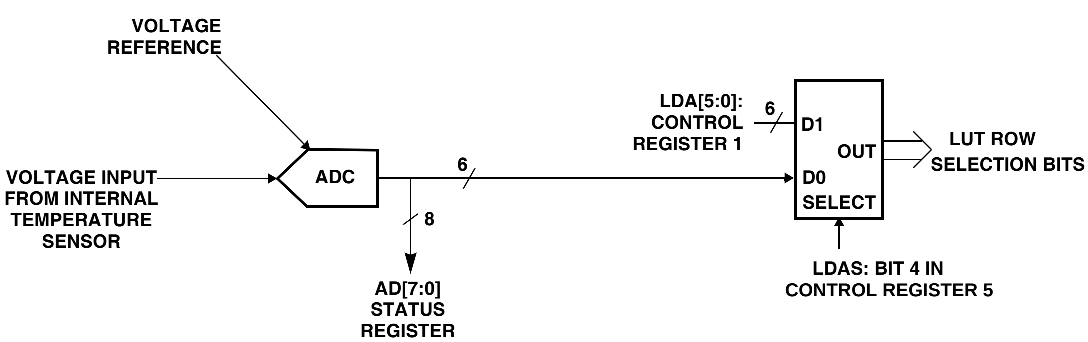


FIGURE 7. LOOK-UP TABLE ADDRESSING

By examining the block diagram in Figure 5, we see that the maximum current through pin I_{OUT} is set by fixing values for V(VRef) and R. The output current can then be varied by changing the data byte at the D/A converter input.

In general, the magnitude of the current at the D/A converter output pin may be calculated by Equation 1:

$$I = (V(VRef) / (384 * R)) * N \quad \text{(EQ. 1)}$$

where N is the decimal representation of the input byte to the corresponding D/A converter.

The value for the resistor determines the full scale output current that the D/A converter may sink or source. Bits IFSO1 and IFSO0 select the full scale output current setting for Iout as described in "IFSO1 - IFSO0: Current Generator Full Scale Output Set Bits (Non-volatile)" on page 9.

Bit IDS and in control register 0 select the direction of the currents through pins Iout (See "IDS: Current Generator Direction Select Bit (Non-volatile)" on page 7, and)"The IDS bit sets the polarity of the Current Generator. When this bit is set to "0" (default), the Current Generator of the X96011 is configured as a Current Source. The Current Generator is configured as a Current Sink when the IDS bit is set to "1". See Figure 5."

D/A Converter Output Current Response

When the D/A converter input data byte changes by an arbitrary number of bits, the output current changes from an intial current level (I_x) to some final level ($I_x + \Delta I_x$). The transition is monotonic and glitchless.

D/A Converter Control

The data byte inputs of the D/A converters can be controlled in three ways:

1) With the A/D converter and through the look-up tables (default)

2) Bypassing the A/D converter and directly accessing the look-up tables

3) Bypassing both the A/D converter and look-up tables, and directly setting the D/A converter input byte

The options are summarized in Table 1.

TABLE 1. D/A CONVERTER ACCESS SUMMARY

LDAS	DDAS	CONTROL SOURCE
0	0	A/D converter through LUT (Default)
1	0	Bits LDA5 - LDA0 through LUT
X	1	Bits DDA7 - DDA0
"X" = Don't Care Condition (May be either "1" or "0")		

Bit DDAS is used to bypass the A/D converter and look-up table, allowing direct access to the input of the D/A converter with the byte in control register 3. See Figure 6, and the descriptions of the control bits.

Bit IDS in Control Register 0 select the direction of the current through pin Iout. See Figure 5, and the descriptions of the control bits.

Power-on Reset

When power is applied to the V_{CC} pin of the X96011, the device undergoes a strict sequence of events before the current outputs of the D/A converters are enabled.

When the voltage at V_{CC} becomes larger than the power-on reset threshold voltage (V_{POR}), the device recalls all control bits from non-volatile memory into volatile registers. Next, the analog circuits are powered up. When the voltage at V_{CC} becomes larger than a second voltage threshold (V_{ADCOK}), the ADC is enabled. In the default case, after the ADC performs four consecutive conversions with the same exact result, the ADC output is used to select a byte from the look-up table. The byte becomes the input of the DAC. During all the previous sequence the input of the DAC is 00h. If bit ADCfiltOff is "1", only one ADC conversion is necessary. Bit DDAS and LDAS, also modify the way the DAC is accessed the first time after power-up, as described in "Control Register 5" on page 9.

The X96011 is a hot pluggable device. Voltage distrubances on the V_{CC} pin are handled by the power-on reset circuit, allowing proper operation during hot plug-in applications.

Serial Interface

Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. The X96011 operates as a slave in all applications.

Serial Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes while SCL is HIGH are reserved for indicating START and STOP conditions. See Figure 10. On power-up of the X96011, the SDA pin is in the input mode.

Serial Start Condition

All commands are preceded by the START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met. See Figure 9.

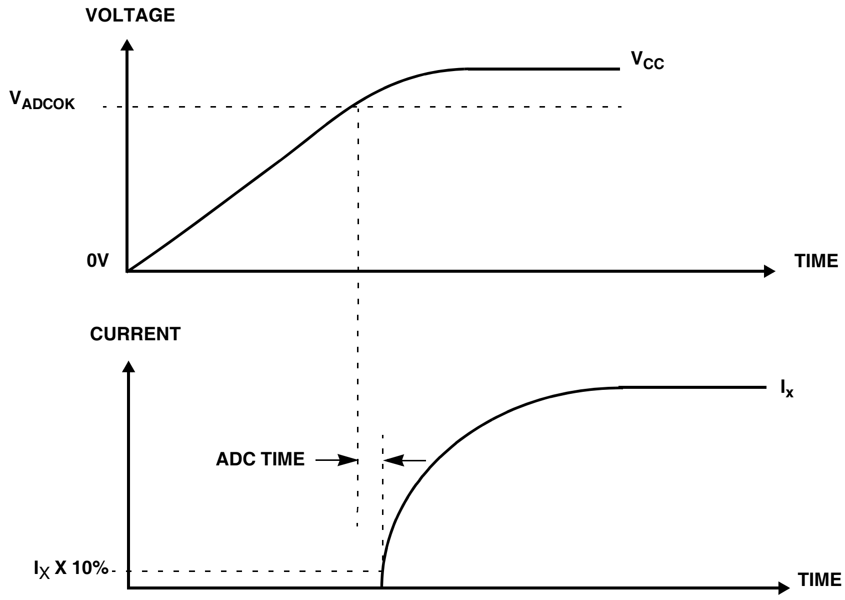


FIGURE 8. CONVERTER POWER-ON RESET RESPONSE

Serial Stop Condition

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a read sequence. A STOP condition can only be issued after the transmitting device has released the bus. See Figure 9.

Serial Acknowledge

An ACK (Acknowledge), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. See Figure 11.

The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte. A valid Slave Address byte must contain the Device Type Identifier 1010, and the Device Address bits matching the logic state of pins A2, A1, and A0. See Figure 13.

If a write operation is selected, the device responds with an ACK after the receipt of each subsequent eight-bit word.

In the read mode, the device transmits eight bits of data, releases the SDA line, and then monitors the line for an ACK. The device continues transmitting data if an ACK is detected. The device terminates further data transmissions if an ACK is not detected. The master must then issue a STOP condition to place the device into a known state.

1. The X96011 acknowledges all incoming data and address bytes except: 1) The “Slave Address Byte” when the “Device Identifier” or “Device Address” are wrong; 2) All “Data Bytes” when the “WEL” bit is “0”, with the exception of a “Data Byte” addresses to location 86h; 3) “Data Bytes” following a “Data Byte” addressed to locations 80h, 85h, or 86h.

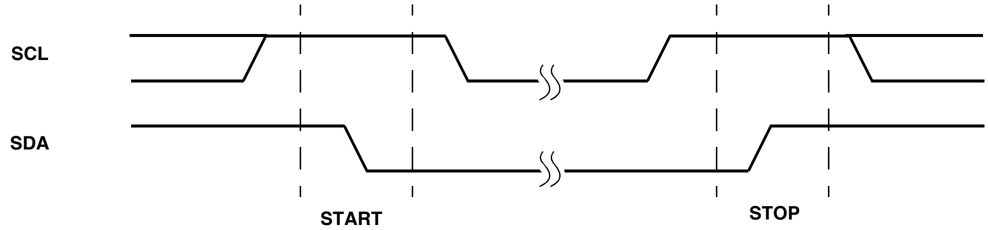


FIGURE 9. VALID START AND STOP CONDITIONS

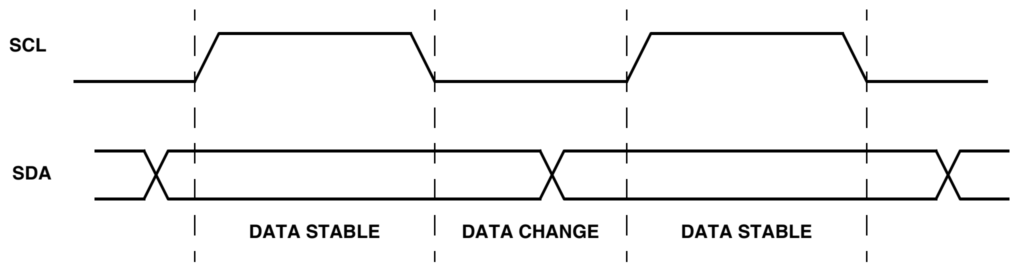


FIGURE 10. VALID DATA CHANGES ON THE BUS

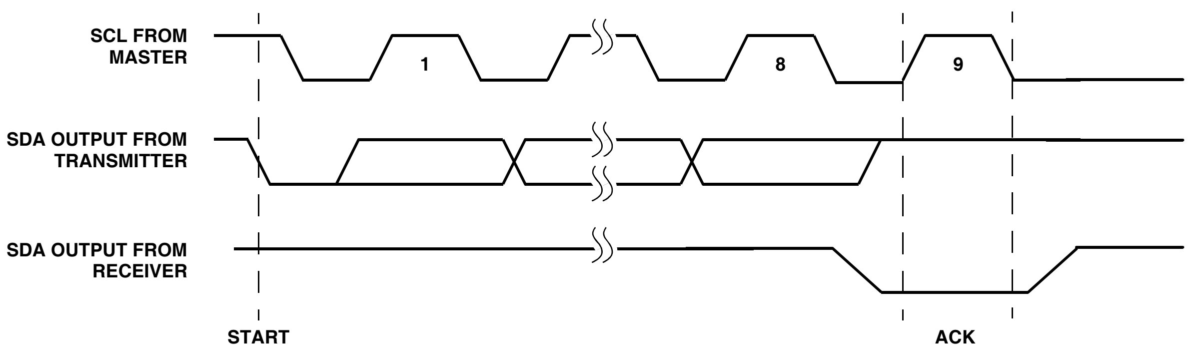


FIGURE 11. ACKNOWLEDGE RESPONSE FROM RECEIVER

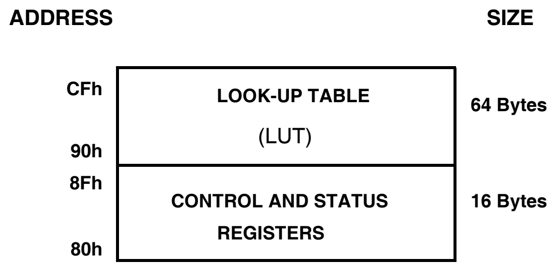


FIGURE 12. X96011 MEMORY MAP

X96011 Memory Map

The X96011 contains a 80 byte array of mixed volatile and nonvolatile memory. This array is split up into two distinct parts, namely: (Refer to Figure 12).

- Look-up Table (LUT)
- Control and Status Registers

The Control and Status registers of the X96011 are used in the test and setup of the device in a system. These registers are realized as a combination of both volatile and nonvolatile memory. These registers reside in the memory locations 80h through 8Fh. The reserved bits within registers 80h through 86h, must be written as “0” if writing to them, and should be ignored when reading. Register bits shown as 0 or 1, in Figure 4, must be written with the indicated value if writing to them. The reserved registers, 82h, 84h, and from 88h through 8Fh, must not be written, and their content should be ignored.

The LUT is realized as nonvolatile EEPROM, and extend from memory locations 90h–CFh. This LUT is dedicated to storing data solely for the purpose of setting the outputs of Current Generators I_{OUT}.

All bits in the LUT are preprogrammed to “0” at the factory.

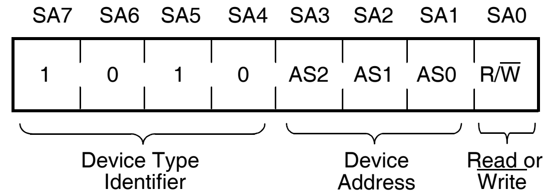
Addressing Protocol Overview

All Serial Interface operations must begin with a START, followed by a Slave Address Byte. The Slave address selects the X96011, and specifies if a Read or Write operation is to be performed.

It should be noted that the Write Enable Latch (WEL) bit must first be set in order to perform a Write operation to any other bit. See “WEL: Write Enable Latch (Volatile)” on page 9. Also, all communication to the X96011 over the 2-wire serial bus is conducted by sending the MSB of each byte of data first.

The memory is physically realized as one contiguous array, organized as 5 pages of 16 bytes each.

The X96011 2-wire protocol provides one address byte. The next few sections explain how to access the different areas for reading and writing.



SLAVE ADDRESS BIT(s)	DESCRIPTION
SA7 - SA4	Device Type Identifier
SA3 - SA1	Device Address

FIGURE 13. SLAVE ADDRESS (SA) FORMAT

Slave Address Byte

Following a START condition, the master must output a Slave Address Byte (Refer to Figure 13). This byte includes three parts:

- The four MSBs (SA7 - SA4) are the Device Type Identifier, which must always be set to 1010 in order to select the X96011.
- The next three bits (SA3 - SA1) are the Device Address bits (AS2 - AS0). To access any part of the X96011’s memory, the value of bits AS2, AS1, and AS0 must correspond to the logic levels at pins A2, A1, and A0 respectively.
- The LSB (SA0) is the $R/\overline{W}$ bit. This bit defines the operation to be performed on the device being addressed. When the $R/\overline{W}$ bit is “1”, then a Read operation is selected. A “0” selects a Write operation (Refer to Figure 13)

Nonvolatile Write Acknowledge Polling

After a nonvolatile write command sequence is correctly issued (including the final STOP condition), the X96011 initiates an internal high voltage write cycle. This cycle typically requires 5ms. During this time, any Read or Write command is ignored by the X96011. Write Acknowledge Polling is used to determine whether a high voltage write cycle is completed.

During acknowledge polling, the master first issues a START condition followed by a Slave Address Byte. The Slave Address Byte contains the X96011’s Device Type Identifier and Device Address. The LSB of the Slave Address ($R/\overline{W}$) can be set to either 1 or 0 in this case. If the device is busy within the high voltage cycle, then no ACK is returned. If the high voltage cycle is completed, an ACK is returned and the master can then proceed with a new Read or Write operation. (Refer to Figure 14)

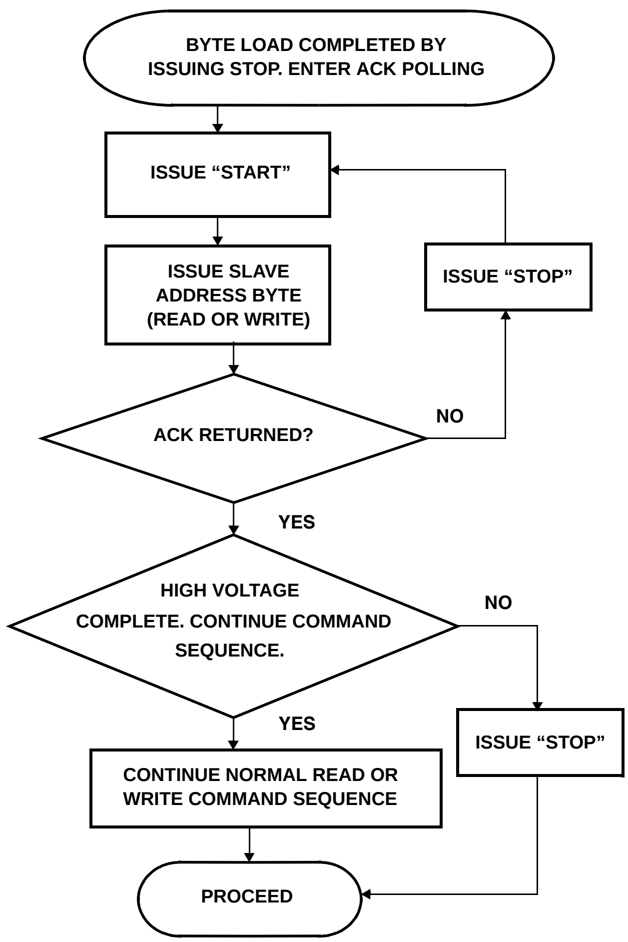


FIGURE 14. ACKNOWLEDGE POLLING SEQUENCE

Byte Write Operation

In order to perform a Byte Write operation to the memory array, the Write Enable Latch (WEL) bit of the Control 6 Register must first be set to “1”. See “WEL: Write Enable Latch (Volatile)” on page 9.

For any Byte Write operation, the X96011 requires the Slave Address Byte, an Address Byte, and a Data Byte (See Figure 15). After each of them, the X96011 responds with an ACK. The master then terminates the transfer by generating a STOP condition. At this time, if all data bits are volatile, the X96011 is ready for the next read or write operation. If some bits are nonvolatile, the X96011 begins the internal write cycle to the nonvolatile memory. During the internal nonvolatile write cycle, the X96011 does not respond to any requests from the master. The SDA output is at high impedance.

Writing to Control bytes which are located at byte addresses 80h through 8Fh is a special case described in the section “Writing to Control Registers” .

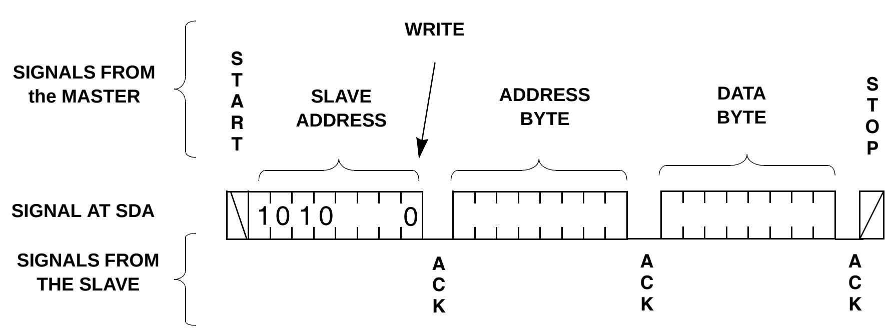


FIGURE 15. BYTE WRITE SEQUENCE

Page Write Operation

The 80-byte memory array is physically realized as one contiguous array, organized as 5 pages of 16 bytes each. A "Page Write" operation can be performed to any of the four LUT pages. In order to perform a Page Write operation, the Write Enable Latch (WEL) bit in Control register 6 must first be set (See "WEL: Write Enable Latch (Volatile)" on page 9.)

A Page Write operation is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 16 bytes (See Figure 16). After the receipt of each byte, the X96011 responds with an ACK, and the internal byte address counter is incremented by one. The page address remains constant. When the counter reaches the end of the page, it "rolls over" and goes back to the first byte of the same page.

For example, if the master writes 12 bytes to a 16-byte page starting at location 11 (decimal), the first 5 bytes are written to locations 11 through 15, while the last 7 bytes are written to locations 0 through 6 within that page. Afterwards, the address counter would point to location 7. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time.
(See Figure 17).

The master terminates the loading of Data Bytes by issuing a STOP condition, which initiates the nonvolatile write cycle. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle.

A Page Write operation cannot be performed on the page at locations 80h through 8Fh. The next section describes the special cases within that page.

Writing to Control Registers

The bytes at locations 80h, 81h, 83h, 85h, and 86h are written using Byte Write operations. They cannot be written using a Page Write operation.

Registers Control 1 and 3 have a nonvolatile and a volatile cell for each bit. At power-up, the content of the nonvolatile cells is automatically recalled and written to the volatile cells. The content of the volatile cells controls the X96011's functionality. If bit NV13 in the Control 0 register is set to "1", a Write operation to these registers writes to both the volatile and nonvolatile cells. If bit NV13 in the Control 0 register is set to "0", a Write operation to these registers only writes to the volatile cells. In both cases the newly written values effectively control the X96011, but in the second case, those values are lost when the part is powered down.

If bit NV13 is set to "0", a Byte Write operation to Control registers 0 or 5 causes the value in the nonvolatile cells of Control registers 1 and 3 to be recalled into their corresponding volatile cells, as during power-up. This doesn't happen when the $\overline{\text{WP}}$ pin is LOW, because Write Protection is enabled. It is generally recommended to configure Control registers 0 and 5 before writing to Control registers 1 or 3.

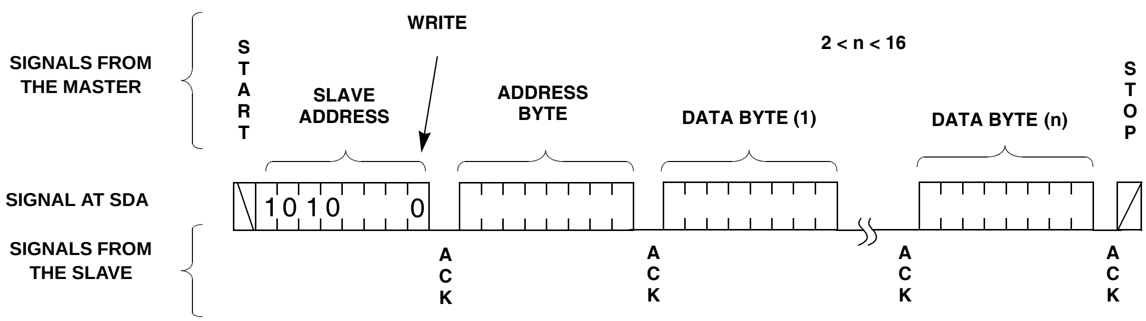


FIGURE 16. PAGE WRITE OPERATION

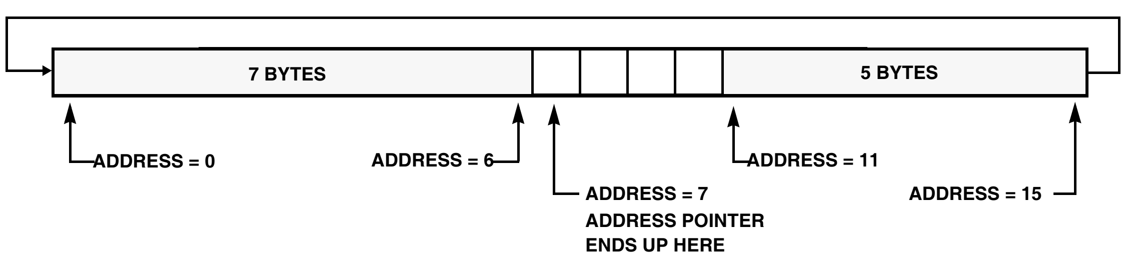


FIGURE 17. EXAMPLE: WRITING 12 BYTES TO A 16-BYTE PAGE STARTING AT LOCATION 11.

A “Byte Write” operation to Control register 1 or 3, causes the value in the nonvolatile cells of the other to be recalled into the corresponding volatile cells, as during power-up.

When reading either of the control registers 1 or 3, the Data Bytes are always the content of the corresponding nonvolatile cells, even if bit NV13 is “0” (Figure 5).

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Slave Address byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Slave Address byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the X96011 responds with an ACK. Then the X96011 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eigth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (Figure 18).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location CFh a stop should be issued. If the read operation continues the output bytes are unpredictable. If the byte address is set between 00h and 7Fh, or higher than CFh, the output bytes are unpredictable.

A Read operation internal pointer can start at any memory location from 80h through CFh, when the Address Byte is 80h through CFh respectively.

When reading any of the control registers 1, 2, 3, or 4, the Data Bytes are always the content of the corresponding nonvolatile cells, even if bit NV13 is "0". See “IDS: Current Generator Direction Select Bit (Non-volatile)”. See Figure 5.

Data Protection

There are three levels of data protection designed into the X96011: 1- Any Write to the device first requires setting of the WEL bit in Control 6 register; 2- The Write Protection pin disables any writing to the X96011; 3- The proper clock count, data bit sequence, and STOP condition is required in order to start a nonvolatile write cycle, otherwise the X96011 ignores the Write operation.

$\overline{WP}$: Write Protection Pin

When the Write Protection ($\overline{WP}$) pin is active (LOW), any Write operations to the X96011 is disabled, except the writing of the WEL bit. See

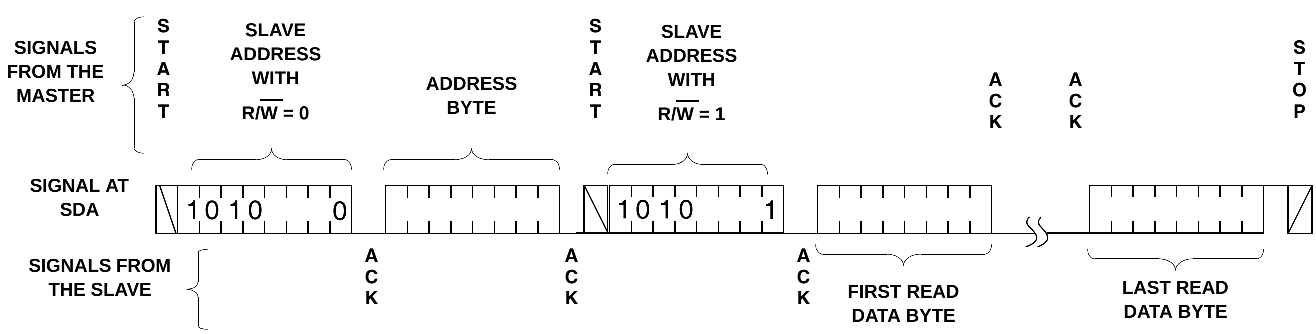
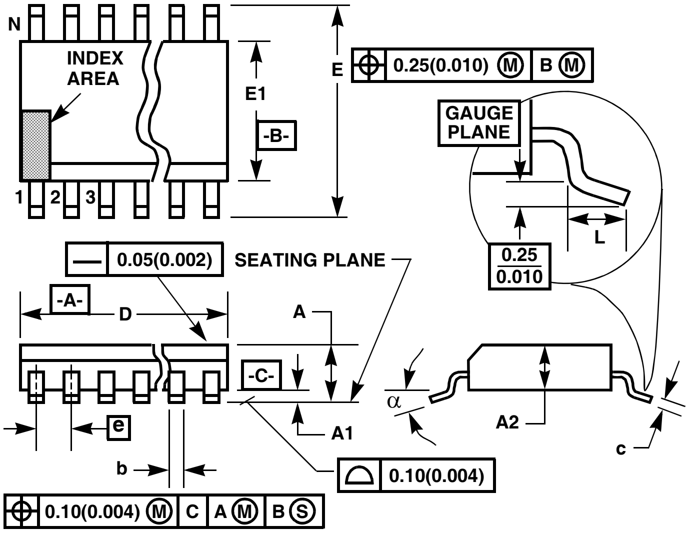


FIGURE 18. READ SEQUENCE

Thin Shrink Small Outline Plastic Packages (TSSOP)



M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 2 4/06

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)