Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

IDT73200
IDT73201

FEATURES:

- IDT73200: Eight 16-bit high-speed pipeline registers
- IDT73201: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 12ns to 20ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Read/Write buffer for 32-bit RISC/CISC microprocessors
- Applications as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT73200 and IDT73201 are mutilevel pipeline registers. With IDT's high-performance CEMOS™ technology, the IDT73200 and IDT73201 have access times of 12ns.

The IDT73200 contains eight 16-bit registers which can be configured as one 8-level, two 4-level , four 2-level or eight 1-level pipeline registers.

The IDT73201 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT73201. Three input control pins (SEL_0–SEL_2) select which of the multiplexer inputs are directed to the output (Y_0–Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations such as those in digital signal processing (DSP). The IDT73200 and IDT73201 can also be used as quick access scratch pad registers for general purpose computing.

The two pipeline registers are packaged in 48-pin plastic and ceramic DIPs for through–hole designs as well as 52-pin PLCC and LCC for surface mount designs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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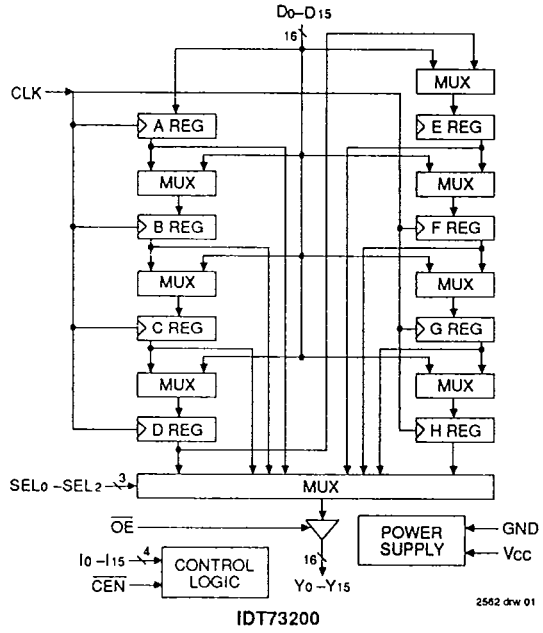
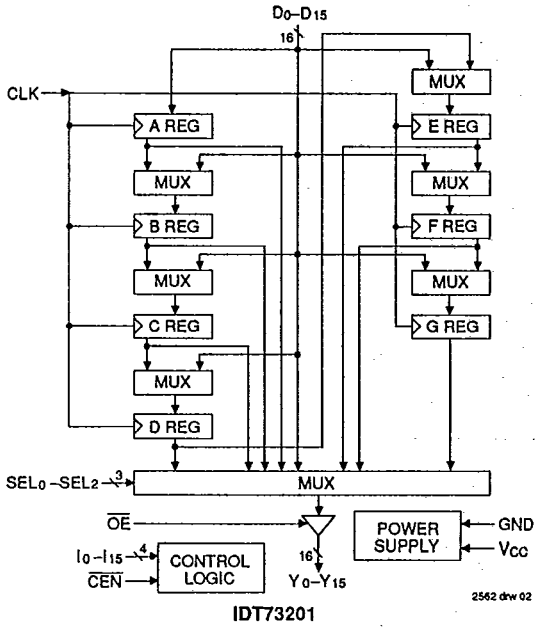
FUNCTIONAL BLOCK DIAGRAMS



IDT73200



IDT73201

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PIN CONFIGURATIONS

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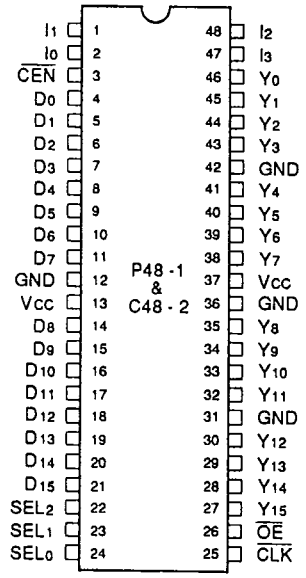
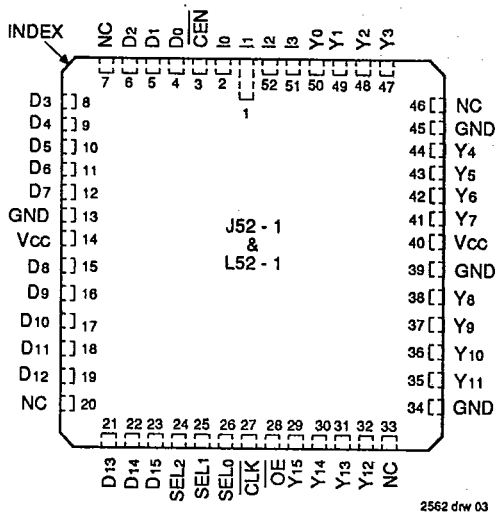


DIP
TOP VIEW



2562 drw 03

PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction I_0–I_3 is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port Y is in a high impedance state. When low, the output port Y is active.
Vcc		Power supply pin, 5V.
GND		Ground pins, 0V.

2562 tbl 01

IDT73200 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$H \rightarrow Y_0 - Y_{15}$

2562 tbl 02

IDT73201 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

2562 tbl 03

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IDT73200 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	—

2562 tbl 04

IDT73201 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	—
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	—

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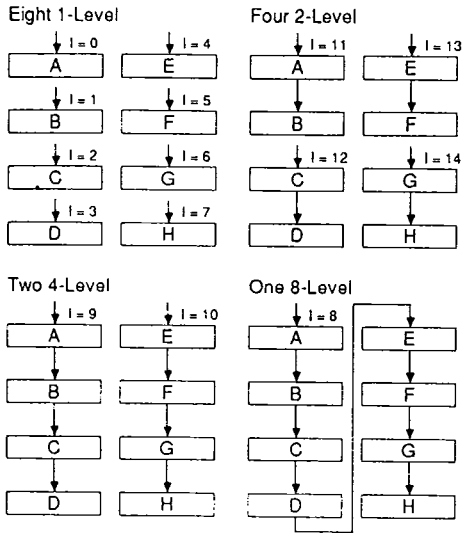
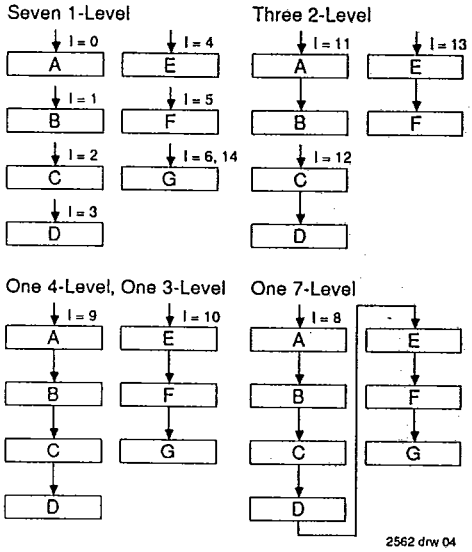
IDT73200 PIPELINE CONFIGURATIONS



IDT73201 PIPELINE CONFIGURATIONS



2562 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
VTERM	Terminal Voltage with Respect to GND	−0.5 to VCC + 0.5	−0.5 to VCC + 0.5	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2562 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2562 tbl 07

1. This parameter is sampled at initial characterization and is not 100% tested.

TEST CIRCUIT

Test	Switch
tPLZ	Closed
tPZL	Closed
Open Drain	Closed
All Other Tests	Open

DEFINITIONS: 2562 tbl 10

CL = Load capacitance includes jig and probe capacitance.
RT = Termination should be equal to ZOUT of the pulse generator. (Typically 50Ω)
VIN = 0V to 3.0V
INPUT: tr = tf = 2.5ns (10% to 90%) unless otherwise specified

DC ELECTRICAL CHARACTERISTICS

T-46-09-27

Commercial: 0°C to +70°C, 5V ± 5%; Military: −55°C to +125°C, 5V ± 10%

Symbol	Parameter	Test Condition		Min.	Max	Unit
V_{IH}	High-Level Input Voltage	—		2.0	—	V
V_{IL}	Low-Level Input Voltage	—		—	0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max.	$V_I = V_{CC}$	—	10	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max.	V_I = GND	—	−10	µA
V_{OH}	High-Level Output Voltage	V_{CC} = Min., I_{OH} = -8mA(COM'L.), −6mA(MIL.)		2.4	—	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA(COM'L.), 12mA(MIL.)		—	0.4	V
V_{IK}	Input Clamp Voltage	I_I = −18mA		—	−1.2	V
I_{OS}	Short Circuit Output Current[2]	V_{CC} = Max., V_O = GND, V_I = V_{CC} or GND		−20	—	mA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	$V_I = V_{CC}$	—	20	µA
I_{OZL}	Low Impedance Output Current	V_{CC} = Max.	V_I = GND	—	−20	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value based on temperature range.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 milliseconds.

2562 tbl 08

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max., $V_I = V_{LC}$ or V_{HC}		—	2	10	mA
I_{CCQT}[3]	Quiescent Power Supply Current Inputs HIGH	V_{CC} = Max., V_I = 3.4V		—	15	45	mA
I_{CCD1}[4]	Dynamic Power Supply Current	V_{CC} = Max., Outputs Disabled, $\overline{OE}$ = HIGH, f_{CP} = 10MHz, 50% Duty Cycle, $V_I \leq V_{HC}$, $V_I \geq V_{LC}$	COM'L.	—	10	30	mA
			MIL.	—	10	40	
I_{CCD1}[4]	Dynamic Power Supply Current	V_{CC} = Max., Outputs Disabled, $\overline{OE}$ = HIGH, f_{CP} = 40MHz, 50% Duty Cycle, $V_I \leq V_{HC}$, $V_I \geq V_{LC}$	COM'L.	—	10	60	mA
			MIL.	—	10	80	

NOTES:
1. For conditions shown as Min. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + (I_{CCQT} \times D_H \times N_T) + I_{CCD}$
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for each TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Charge moved by an input transition pair (HLH or LHL)
   All currents are in milliamps and all frequencies are in megahertz.

2562 tbl 09

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AC ELECTRICAL CHARACTERISTICS

T-46-09-27

Commerical: T_A = 0°C to +70°C, V_{CC} = 5V ±5%; Military: T_A = −55°C to +125°C, V_{CC} = 5V ±10%

Parameter	Commercial				Milltary				Unit
	73200L12 73201L12		73200L15 73201L15		73200L15 73201L15		73200L20 73201L20		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CLK to Y_0–Y_{15} Propagation Delay	—	12	—	15	—	15	—	20	ns
SEL_0–SEL_2 to Y_0–Y_{15} Propagation Delay	—	12	—	15	—	15	—	20	ns
D_0–D_{15} to CLK Set-up Time	3	—	4	—	4	—	5	—	ns
D_0–D_{15} to CLK Hold Time	1	—	2	—	2	—	3	—	ns
I_0–I_3 to CLK Set-up Time	4	—	5	—	5	—	6	—	ns
I_0–I_3 to CLK Hold Time	2	—	2	—	2	—	3	—	ns
CEN to CLK Set-up Time	4	—	5	—	5	—	6	—	ns
CEN to CLK Hold Time	2	—	2	—	2	—	3	—	ns
$\overline{OE}$ Enable Time[1]	—	9	—	10	—	10	—	13	ns
$\overline{OE}$ Disable Time[1]	—	8	—	9	—	9	—	13	ns
CLK Pulse Width HIGH	5	—	5	—	5	—	6	—	ns
CLK Pulse Width LOW	5	—	5	—	5	—	6	—	ns
CLK Period	—	12	—	15	—	15	—	20	ns
Data In to Data Out Flowthrough[2]	—	12	—	15	—	-15	—	20	ns

2562 tbl 11

NOTES:
1. Output Enable and Disable times measured to 500mV change of output voltage level.
2. 73201 only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 4.0V
Input Rise/Fall Times	4ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2562 tbl 12

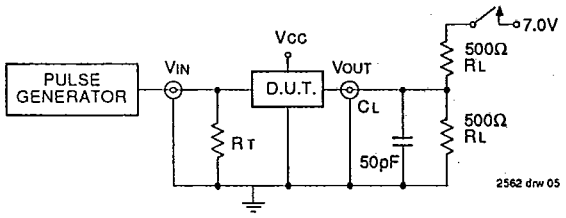

Figure 1. AC Output Test Circuit

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscilliate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

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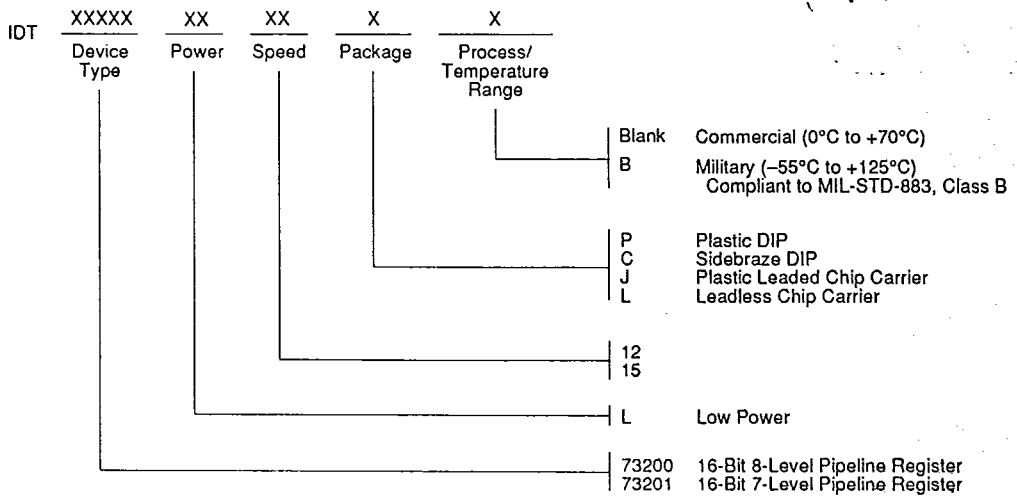
ORDERING INFORMATION



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