

# TS823/824/825 Series

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

SOT-25



### General Description

The TS823/824/825 family allows the user to customize the CPU monitoring function without any external components. The user has a large choice of reset voltage thresholds and output driver configurations, all of which are present at the factory. Each wafer is trimmed to the customer's specifications.

These circuits will ignore fast negative going transients on V<sub>dd</sub>. The state of the reset output is guaranteed to be correct down to 1V. After V<sub>dd</sub> crosses above a factory present threshold, the TS823/824/825 assert a reset signal. After a predetermined time (the "reset" interval) the reset is deasserted. If V<sub>dd</sub> ever drops below the threshold voltage a reset is asserted immediately. In addition to a supply monitoring function the TS823/824/825 also monitor transitions at the watchdog (WDI) input. If a logic transition does not occur at the WDI pin within a certain time interval (the "watchdog" interval) then a reset is asserted. The reset deasserts after the reset interval, as explained earlier.

The TS823/824/825 can both assert a reset manually by pulling the MR input to ground, and the micro-power quiescent current make this family a natural for portable battery powered equipment.

### Features

- Precision monitoring of +3V, +3.3V and +5V power supply voltage
- Tight voltage threshold tolerance +/-1.5%
- Fully specified over temperature
- 210mS min. power-on reset pulse width
- 3uA(typ) supply current
- Guaranteed reset valid to V<sub>dd</sub> = +1V
- Power supply transient immunity
- No external components

### Applications

- Computers and Controllers
- Embedded Controllers
- Intelligent instruments
- Critical uP monitoring
- Portable / Battery powered equipment
- Automotive Systems

### Ordering Information

Part No.	Package	Packing
TS823CX5 <sub>x</sub> RF	SOT-25	3Kpcs / 7" Reel
TS824CX5 <sub>x</sub> RF	SOT-25	3Kpcs / 7" Reel
TS825CX5 <sub>x</sub> RF	SOT-25	3Kpcs / 7" Reel

Note: **x** is the threshold voltage type, option as

**A** : 4.63V   **B** : 4.38V   **D** : 3.08V   **E** : 2.93V

**F** : 2.63V   **G** : 2.32V   **H** : 2.19V

Contact factory for additional voltage option

### Pin Descriptions

Function	TS823	TS824	TS825
RESET (Active-Low)	1	1	1
Ground	2	2	2
Manual Reset	3	-	4
(RESET) (Active-High)	-	3	3
Watchdog Input	4	4	-
Supply Voltage (V <sub>dd</sub> )	5	5	5

### Absolute Maximum Rating

Parameter	Symbol	Maximum	Unit
Supply Voltage	V <sub>dd</sub>	6.0	V
Supply Voltage - Recommended	V <sub>dd</sub>	0.9 ~ 5	V
Operating Junction Temperature Range	T <sub>OP</sub>	-40 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C
Thermal Resistance	θ <sub>JC</sub>	256	°C/W
Maximum Lead Temperature (260°C)	T <sub>LEAD</sub>	10	S

Notes: Stress above the listed absolute rating may cause permanent damage to the device.

# TS823/824/825 Series

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

### Electrical Specifications (Ta = 25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input Supply Voltage		Vdd	1.0	--	5.5	V
Supply Current	WDI and MRB unconnected	Idd	--	3	10	uA
Reset Threshold	TS823/824/825CX5A	V <sub>TH</sub>	4.56	4.63	4.7	V
	TS823/824/825CX5B		4.31	4.38	4.45	
	TS823/824/825CX5D		3.03	3.08	3.13	
	TS823/824/825CX5E		2.89	2.93	2.97	
	TS823/824/825CX5F		2.59	2.63	2.67	
	TS823/824/825CX5G		2.28	2.32	2.36	
	TS823/824/825CX5H		2.15	2.19	2.23	
RESET Output Voltage Low	Vdd < V <sub>TH(MIN)</sub> , I <sub>SINK</sub> = 1.2mA,	V <sub>OL</sub>	--	--	0.5	V
(RESET) Output Voltage High	Vdd > V <sub>TH(MAX)</sub> , I <sub>SOURCE</sub> = 0.5mA	V <sub>OH</sub>	0.8 Vdd	--	--	V
Vdd to Reset Delay	Vdd = V <sub>TH</sub> - 100mV	T <sub>D1</sub>	--	40	--	uS
Reset Active Timeout Period	Ta = -40°C ~ +85°C	T <sub>D2</sub>	140	210	280	mS
Watchdog Timeout Period		T <sub>WD</sub>	1120	1760	2400	mS
WDI Pulse Width		T <sub>WDI</sub>	50	--	--	nS
WDI Input Threshold	Vdd = V <sub>TH</sub> × 1.2	W <sub>DIHL</sub>	--	--	0.7	V
		W <sub>DIH</sub>	0.8 Vdd	--	--	V
WDI Input Current	W <sub>DI</sub> = 0V	I <sub>IL</sub>	-15	-8	0.7	uA
	W <sub>DI</sub> = Vdd = 5V	I <sub>IH</sub>	--	8	15	uA
MR Input Threshold	Vdd = V <sub>TH</sub> × 1.2	M <sub>RIL</sub>	--	--	0.7	V
		M <sub>RIH</sub>	0.8 Vdd	--	--	V
MR Pulse Width		T <sub>WMR</sub>	1	--	--	uS
MR Noise Immunity	Pulse width with no reset		--	100	--	nS
MR to Reset Delay	Vdd = V <sub>TH</sub> - 100mV	T <sub>DMR</sub>	--	500	--	nS
MR Pull Up Resistance			80	--	120	KΩ
Input Supply Voltage	Ta = -40°C ~ +85°C	V <sub>CC</sub>	1.0	--	5.5	V

### Detail Description

#### Pin Function

Pin Name	Pin Description
Reset	Active Low
GND	Ground
(Reset)	Active High
MR	This pin is active low. Pulling this pin low to forces a reset. After a low to high transition reset remains asserted for exactly one reset timeout period. This pin is internally pulled high. If this function is unused then float this pin or tie it to Vdd.
WDI	Watch Dog Input. Any transition on this pin will reset the Watch Dog timer. If this pin remains high or low for longer than the Watch Dog interval then a reset is asserted. Float or tri-state this pin to disable the Watch Dog feature.
Vdd	Positive power supply. A reset is asserted after this voltage drops below a predetermined level. After Vdd rises above that level reset remains asserted until the end of the reset timeout period.

# TS823/824/825 Series

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

### **Application Information**

The TS823/824/825 are designed to interface with the reset input of a microprocessor and to prevent CPU execution errors due to power up, power down, and other power supply errors. The TS823/824 also monitor the CPU health by checking for signal transitions from the CPU at the WDI input.

#### **Reset Output**

Active low reset outputs are denoted as RESET, Active high reset output are denoted as (RESET),

A reset will be asserted if any of three things happen:

1. Vdd drops below the threshold ( $V_{th}$ )
2. The MR pin is pulled low.
3. The WDI pin does not detect a transition within the Watch Dog interval (TWD)

The reset will remain asserted for the prescribed reset interval after:

1. Vdd rises above the threshold ( $V_{th}$ )
2. MR goes high
3. The Watch Dog timer have timed out causing the reset to assert.

#### **Manual Reset Input**

The TS823 and TS825 feature a manual reset feature (MR). A logic low on the MR pin asserts a reset. The reset remains asserted as long as the MR pin remains low. After the MR pin transitions to a high state the reset remains asserted for the prescribed reset interval (TD2). The MR pin is internally pulled up to Vdd by a 100K $\Omega$  resistor. It is internally de-bounced to reject switching transients.

The MR pin is ESD protected by diodes connected to Vdd and Gnd. So the MR pin should never be driven higher than Vdd or lower than Gnd.

#### **Watchdog Input**

The TS823 and TS824 are equipped with a watchdog input (WDI). If the microprocessor does not produce a valid logic edge at the watchdog input (WDI) within the prescribed watchdog interval (TWD) then a reset asserts. The reset remains asserted for the required reset interval (TD2). At the end of the reset interval the reset is deasserted and the watchdog interval timer starts again from zero.

If the watchdog input is left unconnected or is connected to a tri-stated buffer the watchdog function is disabled. As soon as the WDI input is driven either low or high the watchdog function resumes with the watchdog timer set to zero.

#### **Watchdog Input Current**

The watchdog input pin (WDI) typically sources/sinks 8 $\mu$ A when driven high or low. So from a power dissipation point of view the duty cycle of the waveform at WDI is unimportant. When the WDI pin is floating or tri-stated the power supply current fall to less than 3 $\mu$ A.

#### **Glitch Rejection**

The TS823/824/825 family will reject negative going transients on the Vdd line to some extent. The smaller the duration of the transient the larger its amplitude may be without triggering a reset. The "Glitch Rejection" chart in the graphs section of this datasheet shows the relation between glitch amplitude and allowable glitch duration to avoid unintended resets.

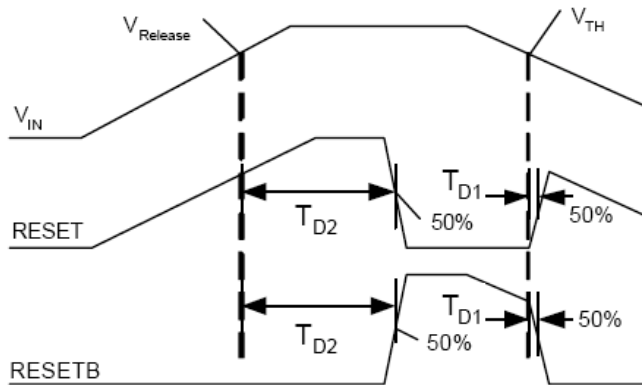
#### **Accurate Output State at Low Vdd**

With Vdd voltage on the order of the MOS transistor threshold (<1V) the outputs of the TS823/824/825 may become undefined. For parts with active low output RESET a resistor placed between RESET and Gnd on the order of 100K $\Omega$  will ensure that the RESET output stays low when Vdd is lower than the threshold voltage of the part. In a like manner a resistor on the order of 100K $\Omega$  when placed between (RESET) and Vdd will ensure parts with active high output (RESET) will remain high when Vdd is lower than the threshold voltage of the parts.

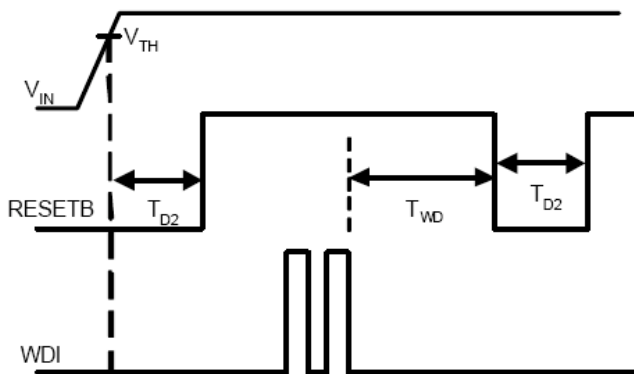
# TS823/824/825 Series

Microprocessor Supervisory Circuit  
with Watchdog Timer & Manual Reset

**Reset Timing Diagram**



**Reset Timing Diagram**



# TS823/824/825 Series

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

### Electrical Characteristics Curve

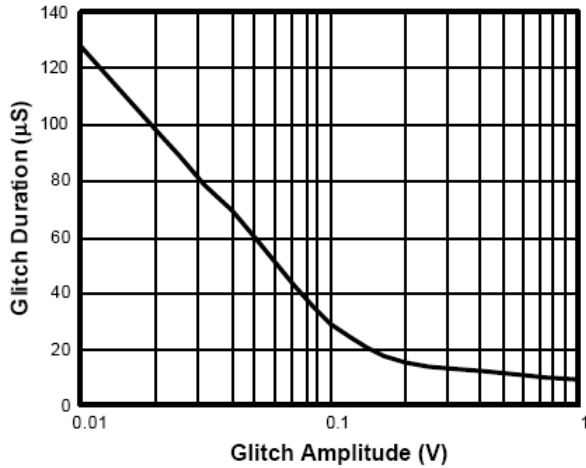


Figure 1. Glitch Rejection

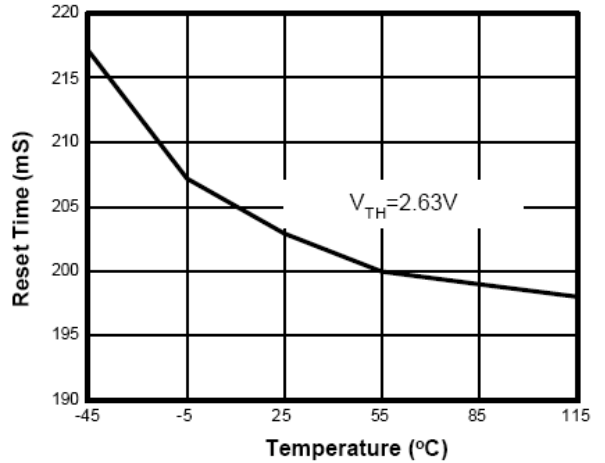


Figure 2. Reset Time vs. Temperature

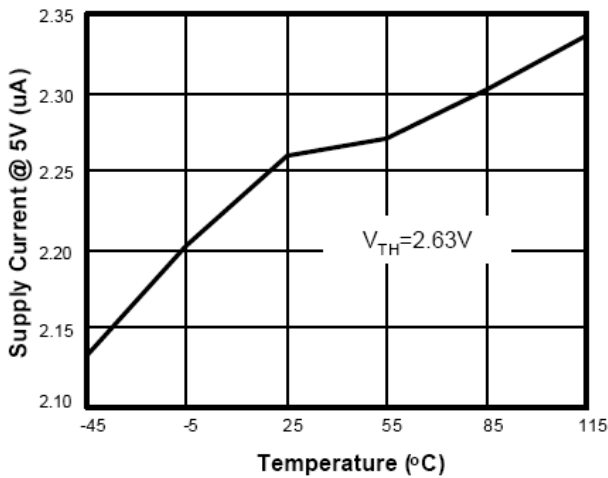


Figure 3. Iin vs. Temperature

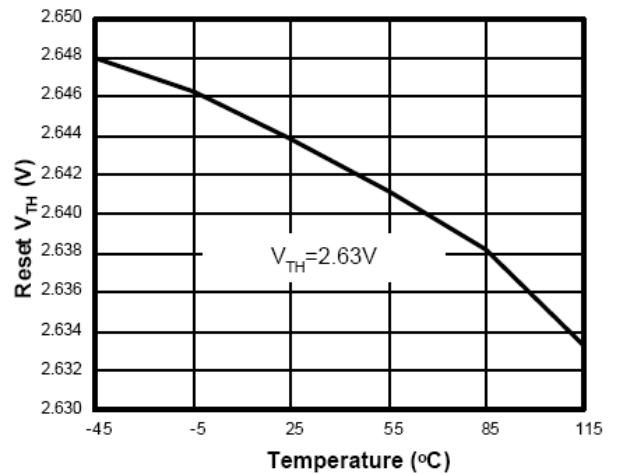


Figure 4. Reset  $V_{TH}$  vs. Temperature

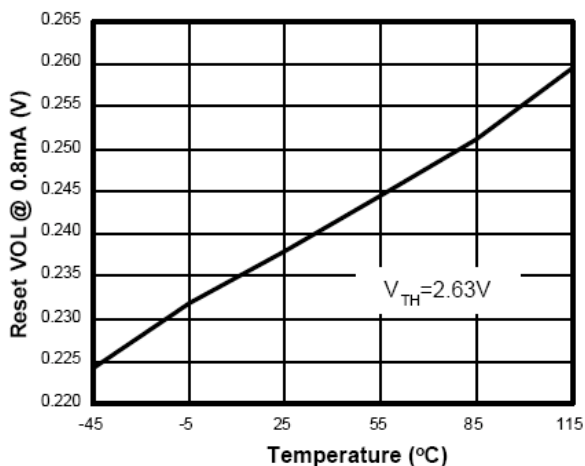
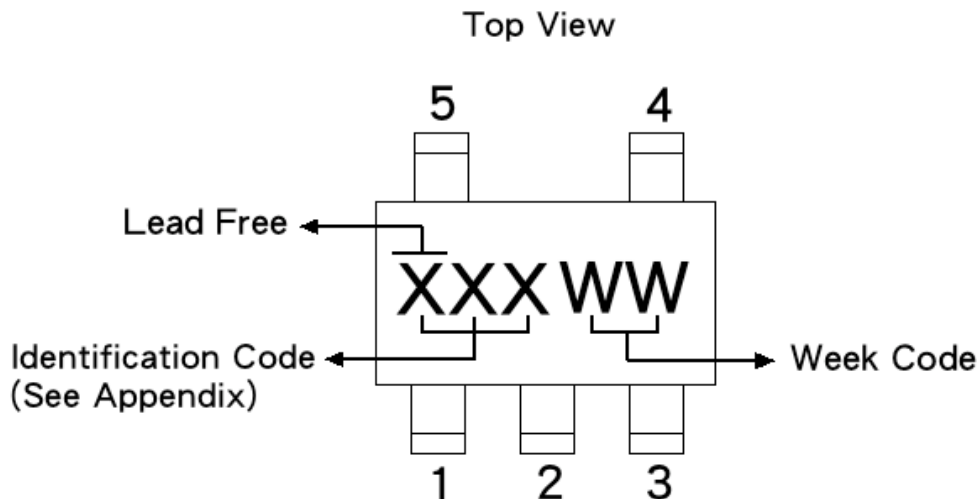


Figure 5. Reset VOL vs. Temperature

# TS823/824/825 Series

Microprocessor Supervisory Circuit  
with Watchdog Timer & Manual Reset

## Marking Information



Part No.	Identification Code	Part No.	Identification Code	Part No.	Identification Code
TS823CX5A	BAC	TS824CX5A	BAD	TS825CX5A	BAE
TS823CX5B	-	TS824CX5B	ATW	TS825CX5B	--
TS823CX5D	ASM	TS824CX5D	ATL	TS825CX5D	ATN
TS823CX5E	ATX	TS824CX5E	ATV	TS825CX5E	AUS
TS823CX5F	ATG	TS824CX5F	ATC	TS825CX5F	AWW
TS823CX5G	BCW	TS824CX5G	--	TS825CX5G	--
TS823CX5B	AWY	TS824CX5B	AWS	TS825CX5B	--

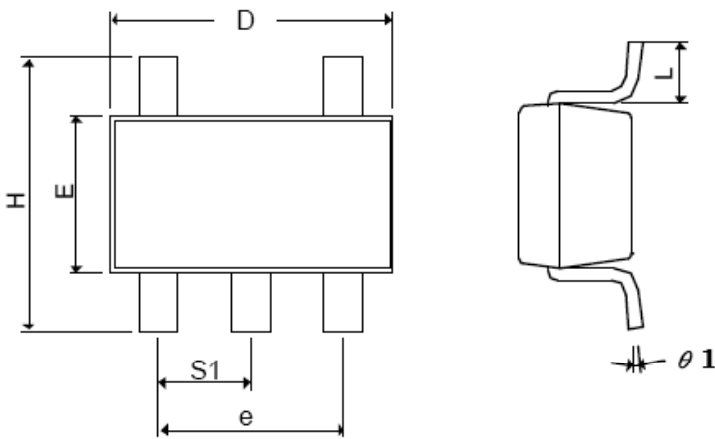
### Year Code definition

Identification Code			Week Code		Year
X	X	X	W	W	xxx0
X	X	X	W	<b>W</b>	xxx1
X	X	X	<b>W</b>	W	xxx2
X	X	X	<b>W</b>	<b>W</b>	xxx3
X	X	<b>X</b>	W	W	xxx4
X	X	<b>X</b>	W	<b>W</b>	xxx5
X	X	<b>X</b>	<b>W</b>	W	xxx6
X	X	<b>X</b>	<b>W</b>	<b>W</b>	xxx7
X	<b>X</b>	X	W	W	xxx8
X	<b>X</b>	X	W	<b>W</b>	xxx9

# TS823/824/825 Series

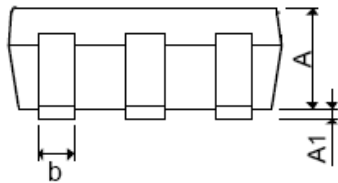
Microprocessor Supervisory Circuit  
with Watchdog Timer & Manual Reset

## SOT-25 Mechanical Drawing



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A+A1	0.09	1.25	0.0354	0.0492
B	0.30	0.50	0.0118	0.0197
C	0.09	0.25	0.0035	0.0098
D	2.70	3.10	0.1063	0.1220
E	1.40	1.80	0.0551	0.0709
E	1.90 BSC		0.0748 BSC	
H	2.40	3.00	0.09449	0.1181
L	0.35 BSC		0.0138 BSC	
$\theta 1$	0°	10°	0°	10°
S1	0.95 BSC		0.0374 BSC	

Front View





# **TS823/824/825 Series**

## Microprocessor Supervisory Circuit with Watchdog Timer & Manual Reset

### **Notice**

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.