ANALOG DEVICES

Quad-Channel Digital Isolators

ADuM1410/ADuM1411/ADuM1412

FEATURES

Low power operation
- **5 V operation**
  - **1.3 mA per channel max @ 0 Mbps to 2 Mbps**
  - **4.0 mA per channel max @ 10 Mbps**
- **3 V operation**
  - **0.8 mA per channel max @ 0 Mbps to 2 Mbps**
  - **1.8 mA per channel max @ 10 Mbps**

Bidirectional communication
3 V/5 V level translation
High temperature operation: 105°C
Up to 10 Mbps data rate (NRZ)
Programmable default output state
High common-mode transient immunity: >25 kV/μs
16-lead, Pb-free, SOIC wide body package
Safety and regulatory approvals
- **UL recognition: 2500 V rms for 1 minute per UL 1577**
- **CSA component acceptance notice #5A**
- **VDE certificate of conformity (pending)**
  - **DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01**
  - **DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000**
  - **V_{IORM} = 560 V peak**

APPLICATIONS

General-purpose multichannel isolation
SPI® interface/data converter isolation
RS-232/RS-422/RS-485 transceiver
Industrial field bus isolation

FUNCTIONAL BLOCK DIAGRAMS

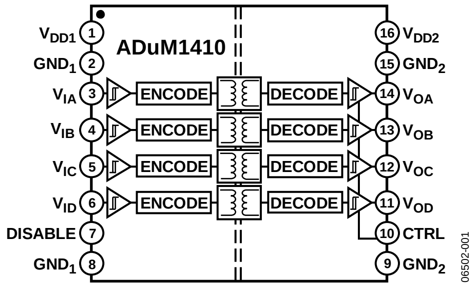


Figure 1. ADuM1410 Functional Block Diagram

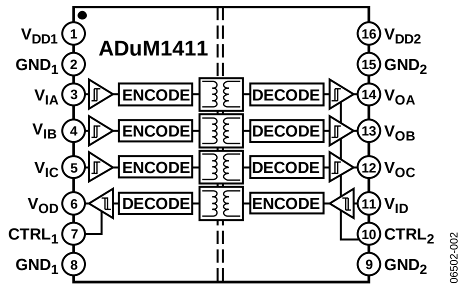


Figure 2. ADuM1411 Functional Block Diagram

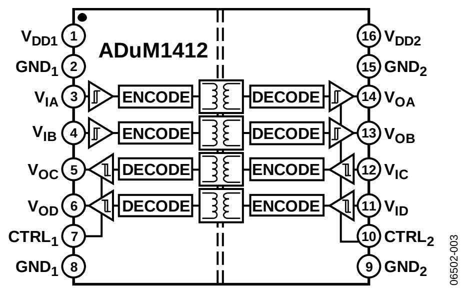


Figure 3. ADuM1412 Functional Block Diagram

GENERAL DESCRIPTION

The ADuM141x[1] are four-channel digital isolators based on Analog Devices, Inc. *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technologies, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The usual concerns that arise with optocouplers, such as uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products.

Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM141x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide) up to 10 Mbps. All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. All products also have a default output control pin. This allows the user to define the logic state the outputs are to adopt in the absence of the input power. Unlike other optocoupler alternatives, the ADuM141x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

[1] Protected by U.S. Patents 5,952,849, 6,873,065 and 7,075,329. Other patents pending.

Rev. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/06—Rev. D to Rev. E

3/06—Rev. C to Rev. D

11/05—Rev. SpB to Rev. C: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. [1]

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.73	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.38	0.53	mA	
ADuM1410, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.4	3.2	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.6	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		8.8	12	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.8	4.0	mA	5 MHz logic signal frequency
ADuM1411, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		5.4	7.6	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		3.8	5.3	mA	5 MHz logic signal frequency
ADuM1412, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		2.0	2.6	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		4.6	6.5	mA	5 MHz logic signal frequency
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{CTRL1}, I_{CTRL2}, $I_{DISABLE}$	−10	+0.01	+10	µA	0 ≤ V_{IA},V_{IB}, V_{IC},V_{ID} ≤ V_{DD1} or V_{DD2}, 0 ≤ V_{CTRL1},V_{CTRL2} ≤ V_{DD1} or V_{DD2}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}, V_{DD2} − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}, V_{DD2} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1411ARW and ADuM1412ARW						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} − t_{PHL}\|$[5]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM141xBRW						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	30	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			5	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			30	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			5	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Enable Time[9]	t_{ENABLE}			2.0	µs	V_{IA}, V_{IB}, V_{IC}, V_{ID}, = 0 or V_{DD1}
Input Disable Time[9]	$t_{DISABLE}$			5.0	µs	V_{IA}, V_{IB}, V_{IC}, V_{ID}, = 0 or V_{DD1}
Input Dynamic Supply Current per Channel[10]	$I_{DDI\,(D)}$		0.12		mA/Mbps	
Output Dynamic Supply Current per Channel[10]	$I_{DDO\,(D)}$		0.04		mA/Mbps	

1 All voltages are relative to their respective ground.

2 The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

3 The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

4 The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

5 t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

6 t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

7 Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

8 CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

9 Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (See Table 10).

10 Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V. [1]

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.25	0.38	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.33	mA	
ADuM1410, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.6	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.8	1.0	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	1.8	mA	5 MHz logic signal frequency
ADuM1411, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.9	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.7	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.1	4.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.1	3.0	mA	5 MHz logic signal frequency
ADuM1412, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		1.0	1.8	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		2.6	3.8	mA	5 MHz logic signal frequency
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{CTRL1}, I_{CTRL2}, $I_{DISABLE}$	−10	+0.01	+10	µA	0 ≤ V_{IA},V_{IB}, V_{IC},V_{ID} ≤ V_{DD1} or V_{DD2}, 0 ≤ V_{CTRL1},V_{CTRL2} ≤ V_{DD1} or V_{DD2}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	1.6			V	
Logic Low Input Threshold	V_{IL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}, V_{DD2} – 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}, V_{DD2} – 0.4	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM1411ARW and ADuM1412ARW						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	75	100	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL}\rvert$[5]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
ADuM141xBRW						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	40	60	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			5	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			30	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			5	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate			1.1		Mbps	
Input Enable Time[9]	t_{ENABLE}		2.0		µs	V_{IA}, V_{IB}, V_{IC}, V_{ID} = 0 or V_{DD1}
Input Disable Time[9]	$t_{DISABLE}$		5.0		µs	V_{IA}, V_{IB}, V_{IC}, V_{ID} = 0 or V_{DD1}
Input Dynamic Supply Current per Channel[10]	$I_{DDI (D)}$		0.07		mA/Mbps	
Output Dynamic Supply Current per Channel[10]	$I_{DDO (D)}$		0.02		mA/Mbps	

[1] All voltages are relative to their respective ground.

[2] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

[3] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

[4] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[6] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[7] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

[9] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (See Table 10).

[10] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

5 V/3 V operation[1]: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			0.50	0.73	mA	
3 V/5 V Operation			0.25	0.38	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.19	0.33	mA	
3 V/5 V Operation			0.38	0.53	mA	
ADuM1410, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			2.4	3.2	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			1.2	1.6	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.8	1.0	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			1.2	1.6	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			8.6	11	mA	5 MHz logic signal frequency
3 V/5 V Operation			3.4	6.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			1.4	1.8	mA	5 MHz logic signal frequency
3 V/5 V Operation			2.6	3.0	mA	5 MHz logic signal frequency
ADuM1411, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			1.0	1.9	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.9	1.7	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			1.7	2.4	mA	DC to 1 MHz logic signal frequency
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			5.4	7.6	mA	5 MHz logic signal frequency
3 V/5 V Operation			3.1	4.5	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			2.1	3.0	mA	5 MHz logic signal frequency
3 V/5 V Operation			3.8	5.3	mA	5 MHz logic signal frequency
ADuM1412, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			2.0	2.6	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			1.0	1.8	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			1.0	1.8	mA	DC to 1 MHz logic signal frequency
3 V/5 V Operation			2.0	2.6	mA	DC to 1 MHz logic signal frequency

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
10 Mbps (BRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1\ (10)}$					
5 V/3 V Operation			4.6	6.5	mA	5 MHz logic signal frequency
3 V/5 V Operation			2.6	3.8	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2\ (10)}$					
5 V/3 V Operation			2.6	3.8	mA	5 MHz logic signal frequency
3 V/5 V Operation			4.6	6.5	mA	5 MHz logic signal frequency
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{CTRL1}, I_{CTRL2}, $I_{DISABLE}$	−10	+0.01	+10	µA	$0 \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or V_{DD2}, $0 \leq V_{CTRL1}, V_{CTRL2} \leq V_{DD1}$ or V_{DD2}, $V_{DISABLE} \leq V_{DD1}$
Logic High Input Threshold	V_{IH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	$V_{DD1}, V_{DD2} - 0.1$	V_{DD1}, V_{DD2}		V	$I_{Ox} = -20$ µA, $V_{Ix} = V_{IxH}$
		$V_{DD1}, V_{DD2} - 0.4$	$V_{DD1}, V_{DD} - 0.2$		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	$I_{Ox} = 20$ µA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400$ µA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM1411ARW and ADuM1412ARW						
Minimum Pulse Width[3]	PW			1000	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	25	70	100	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL}\rvert$[5]	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	$C_L = 15$ pF, CMOS signal levels
ADuM141xBRW						
Minimum Pulse Width[3]	PW			100	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	25	35	60	ns	$C_L = 15$ pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL}\rvert$[5]	PWD			5	ns	$C_L = 15$ pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			30	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			5	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	$C_L = 15$ pF, CMOS signal levels
For All Models						
Output Rise/Fall Time (10% to 90%)	t_R/t_f					$C_L = 15$ pF, CMOS signal levels
5 V/3 V Operation			2.5		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[8]	$\lvert CM_H\rvert$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, $V_{CM} = 1000$ V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\lvert CM_L\rvert$	25	35		kV/µs	$V_{Ix} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Enable Time[9]	t_{ENABLE}		2.0		µs	V_{IA}, V_{IB}, V_{IC}, $V_{ID} = 0$ or V_{DD1}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Disable Time[9]	$t_{DISABLE}$		5.0		µs	V_{IA}, V_{IB}, V_{IC}, V_{ID} = 0 or V_{DD1}
Input Dynamic Supply Current per Channel[10]	$I_{DDI (D)}$					
5 V Operation			0.12		mA/Mbps	
3 V Operation			0.07		mA/Mbps	
Output Dynamic Supply Current per Channel[10]	$I_{DDI (D)}$					
5 V Operation			0.04		mA/Mbps	
3 V Operation			0.02		mA/Mbps	

[1] All voltages are relative to their respective ground.
[2] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.
[3] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[5] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[7] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[9] Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL logic state (See Table 10).
[10] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		28		°C/W	

[1] The ADuM141x device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM141x have been approved by the organizations listed in Table 5.

Table 5.

UL[1]	CSA	VDE[2] (ADuM1411 and ADuM1412 pending)
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01[2]

[1] In accordance with UL1577, each ADuM141x is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
[2] In accordance with DIN EN 60747-5-2, each ADuM141x is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN 60747-5-2 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

These isolators are suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN EN 60747-5-2 approval.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV[1]	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, Partial Discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 7			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

[1] See DIN VDE 0110 for definition of Classification 1 through Classification IV listed in the Characteristic column.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature (T_A) = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages[1] (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages[1, 2] (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages[1, 2] (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2 (I_{O2})	−22 mA to +22 mA
Common-Mode Transients[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 7 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

Table 9.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages	V_{DD1}, V_{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Truth Table (Positive Logic)

V_{IX} Input[1]	CTRL Input[2]	$V_{DISABLE}$ State[3]	V_{DDI} State[4]	V_{DDO} State[5]	V_{OX} Output[1]	Notes
H	X	L or NC	Powered	Powered	H	Normal operation, data is high.
L	X	L or NC	Powered	Powered	L	Normal operation, data is low.
X	H or NC	H	X	Powered	H	Inputs disabled. Outputs are in the default state as determined by CTRL.
X	L	H	X	Powered	L	Inputs disabled. Outputs are in the default state as determined by CTRL.
X	H or NC	X	Unpowered	Powered	H	Input unpowered. Outputs are in the default state as determined by CTRL. Outputs return to input state within 1 µs of V_{DDI} power restoration. See the Pin Configurations and Function Descriptions section for more details.
X	L	X	Unpowered	Powered	L	Input unpowered. Outputs are in the default state as determined by CTRL. Outputs return to input state within 1 µs of V_{DDI} power restoration. See the Pin Configurations and Function Descriptions section for more details.
X	X	X	Powered	Unpowered	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 µs of V_{DDO} power restoration. See the Pin Configurations and Function Descriptions section for more details.

[1] V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D).
[2] CTRL refers to the CTRL signal on the input side of a given channel (A, B, C, or D).
[3] Available only on ADuM1410.
[4] V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).
[5] V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

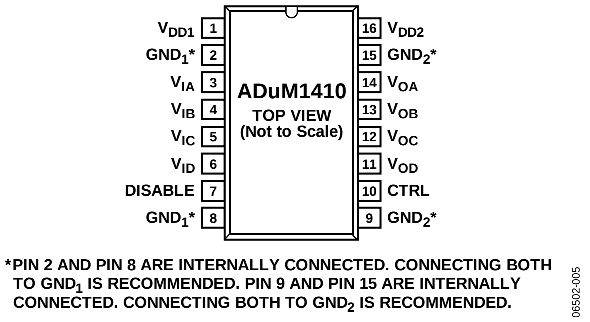
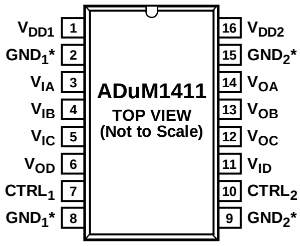


Figure 4. ADuM1410 Pin Configuration

Table 11. ADuM1410 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	DISABLE	Input Disable. Disables the isolator inputs and halts the dc refresh circuits. Outputs take on the logic state determined by CTRL.
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	CTRL	Default Output Control. Controls the logic state the outputs assume when the input power is off. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are high when CTRL is high or disconnected and V_{DD1} is off. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are low when CTRL is low and V_{DD1} is off. When V_{DD1} power is on, this pin has no effect.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND_2 IS RECOMMENDED.

06502-006

Figure 5. ADuM1411 Pin Configuration

Table 12. ADuM1411 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	$CTRL_1$	Default Output Control. Controls the logic state the outputs assume when the input power is off. V_{OD} output is high when $CTRL_1$ is high or disconnected and V_{DD2} is off. V_{OD} output is low when $CTRL_1$ is low and V_{DD2} is off. When V_{DD2} power is on, this pin has no effect.
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	$CTRL_2$	Default Output Control. Controls the logic state the outputs assume when the input power is off. V_{OA}, V_{OB}, and V_{OC} outputs are high when $CTRL_2$ is high or disconnected and V_{DD1} is off. V_{OA}, V_{OB}, and V_{OC} outputs are low when $CTRL_2$ is low and V_{DD1} is off. When V_{DD1} power is on, this pin has no effect.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

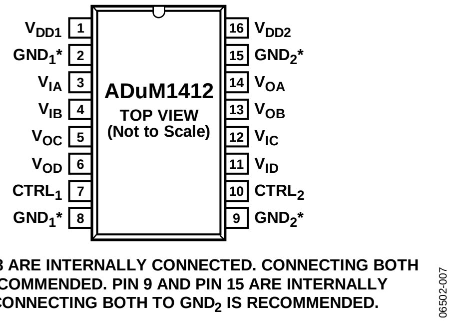


Figure 6. ADuM1412 Pin Configuration

Table 13. ADuM1412 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	$CTRL_1$	Default Output Control. Controls the logic state the outputs assume when the input power is off. V_{OC} and V_{OD} outputs are high when $CTRL_1$ is high or disconnected and V_{DD2} is off. V_{OC} and V_{OD} outputs are low when $CTRL_1$ is low and V_{DD2} is off. When V_{DD2} power is on, this pin has no effect.
8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
9	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	$CTRL_2$	Default Output Control. Controls the logic state the outputs assume when the input power is off. V_{OA} and V_{OB} outputs are high when $CTRL_2$ is high or disconnected and V_{DD1} is off. V_{OA} and V_{OB} outputs are low when $CTRL_2$ is low and V_{DD1} is off. When V_{DD1} power is on, this pin has no effect.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

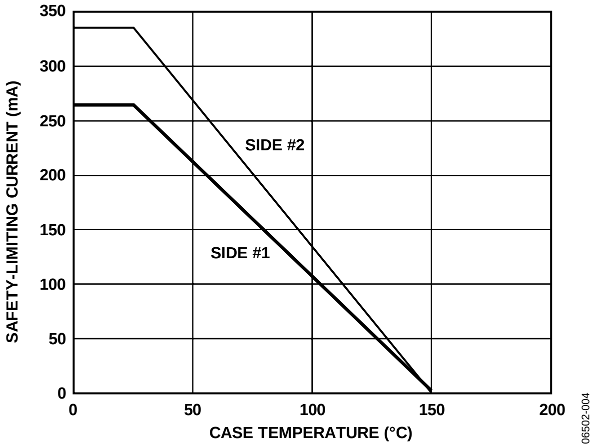


Figure 7. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN 60747-5-2

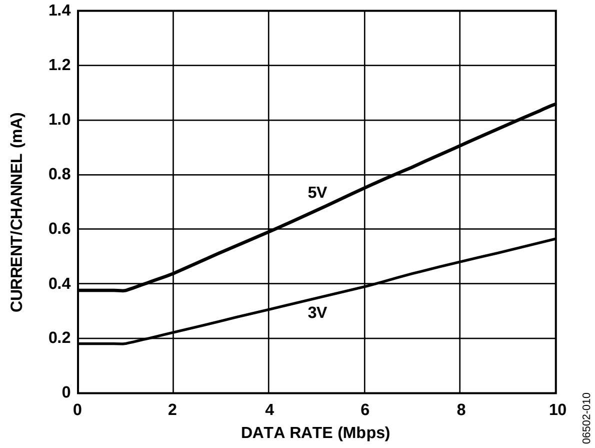


Figure 10. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

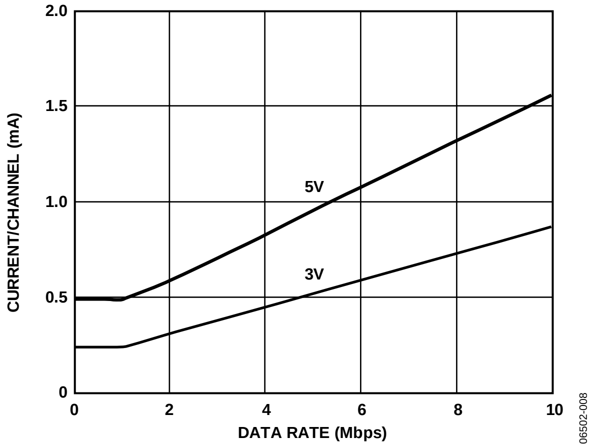


Figure 8. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

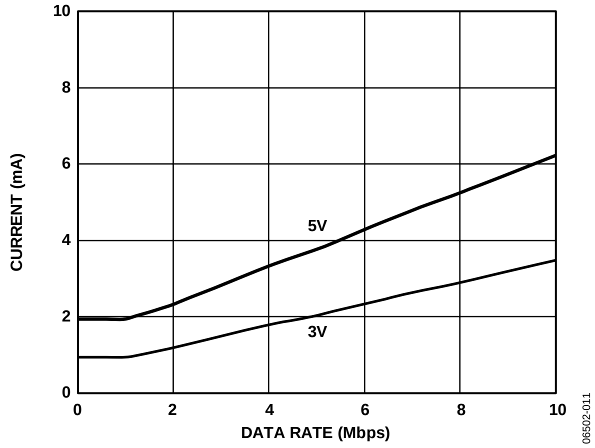


Figure 11. Typical ADuM1410 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

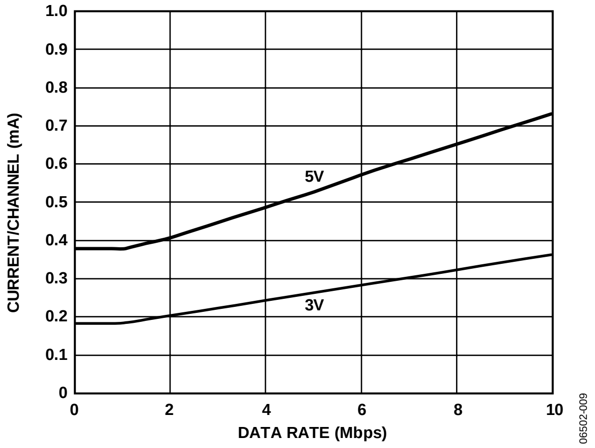


Figure 9. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

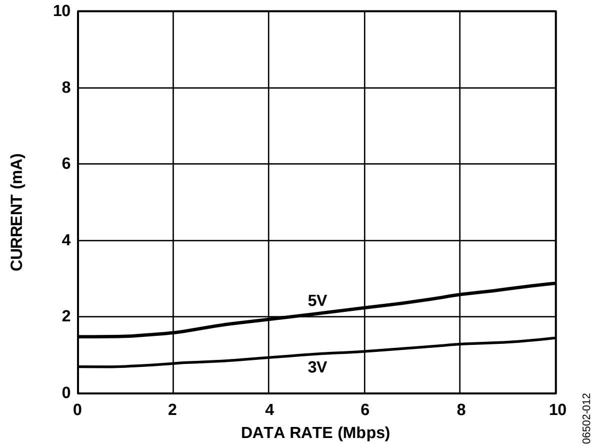


Figure 12. Typical ADuM1410 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

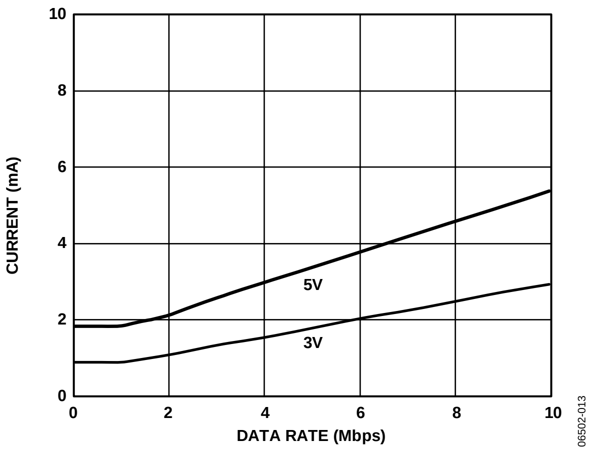


Figure 13. Typical ADuM1411 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

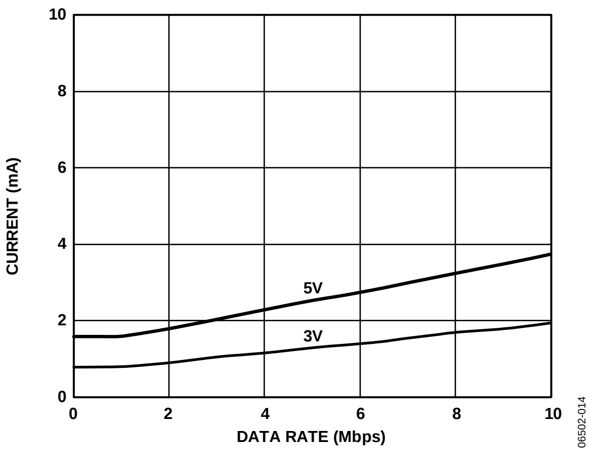


Figure 14. Typical ADuM1411 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

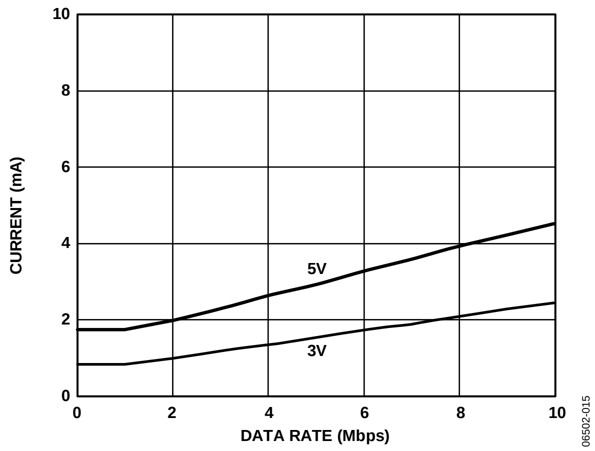


Figure 15. Typical ADuM1412 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM141x digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 16). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1}, and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

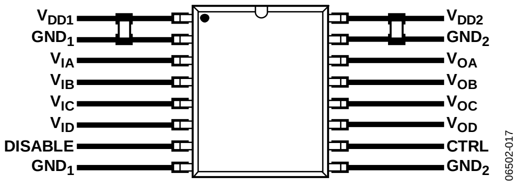


Figure 16. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input to output propagation delay time for a high to low transition may differ from the propagation delay time of a low to high transition.

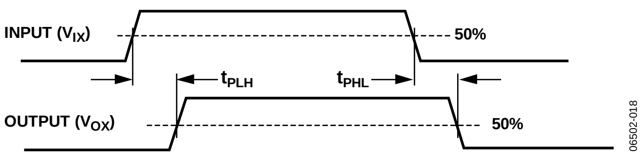


Figure 17. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values, and it is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM141x component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM141x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 2 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The magnetic field immunity of the ADuM141x is determined by the changing magnetic field which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM141x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^th turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM141x and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 18.

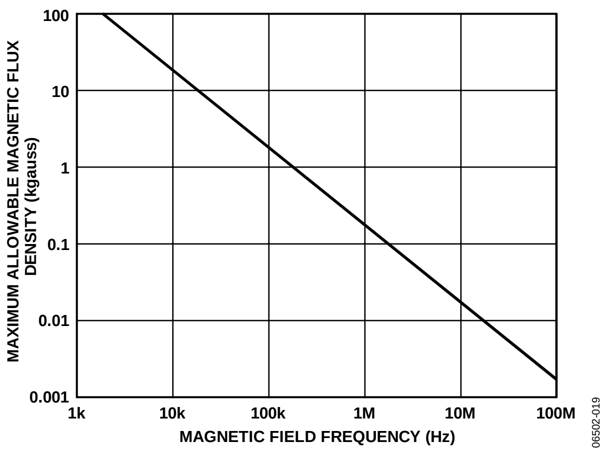


Figure 18. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and was of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM141x transformers. Figure 19 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM141x is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current needed to be placed 5 mm away from the ADuM141x to affect the operation of the component.

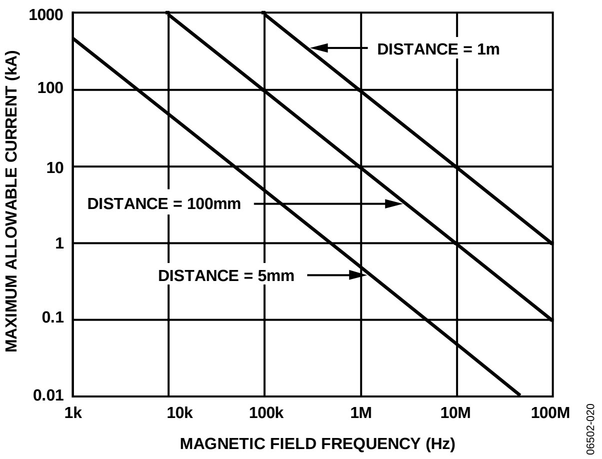


Figure 19. Maximum Allowable Current for Various Current-to-ADuM141x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM141x isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5\,f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5\,f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\,f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz); it is half of the input data rate expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 8 and Figure 9 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1410/ADuM1411/ADuM1412 channel configurations.

OUTLINE DIMENSIONS

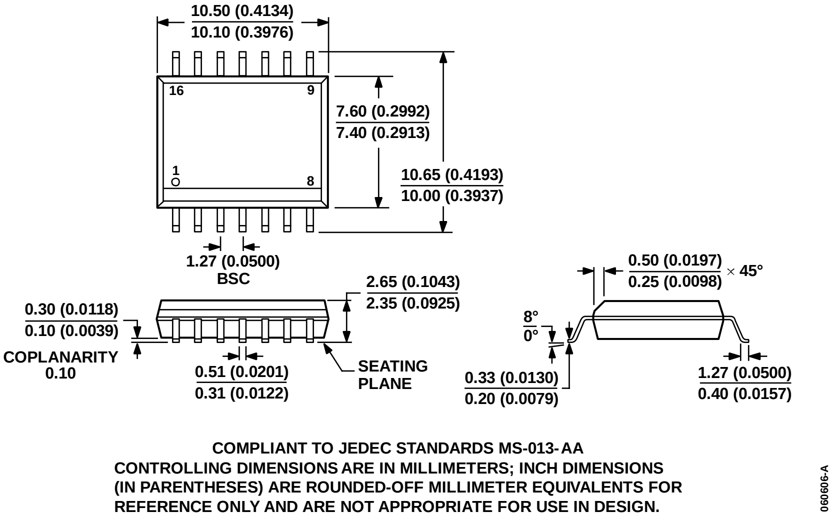


Figure 20. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate	Maximum Propagation Delay, 5 V	Maximum Pulse Width Distortion	Temperature Range	Package Description	Package Option
ADuM1410BRWZ[1]	4	0	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body	RW-16
ADuM1410BRWZ-RL[1]	4	0	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body, 13″ Reel	RW-16
ADuM1411ARWZ[1]	3	1	1 Mbps	100 ns	40 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body	RW-16
ADuM1411ARWZ-RL[1]	3	1	1 Mbps	100 ns	40 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body, 13″ Reel	RW-16
ADuM1411BRWZ[1]	3	1	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body	RW-16
ADuM1411BRWZ-RL[1]	3	1	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body, 13″ Reel	RW-16
ADuM1412ARWZ[1]	2	2	1 Mbps	100 ns	40 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body	RW-16
ADuM1412ARWZ-RL[1]	2	2	1 Mbps	100 ns	40 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body, 13″ Reel	RW-16
ADuM1412BRWZ[1]	2	2	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body	RW-16
ADuM1412BRWZ-RL[1]	2	2	10 Mbps	50 ns	5 ns	−40°C to +105°C	16-Lead SOIC_W, Wide Body, 13″ Reel	RW-16

[1] Z = Pb-free part.

D06502-0-10/06(E)